An Efficient Substrate Noise Coupling Analysis by Blocked Structure-Model-Reduction and Partition

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***Abstract*— *An efficient yet accurate substrate coupling-noise versification procedure has been developed for the lightly doped CMOS process. A novel block-structured model reduction is used to improve the model reduction efficiency. Furthermore, the verification of coupling-noise voltage at each contact is reformulated as an optimization procedure under user-supplied current constraints. One by-product during the verification can be further used to guide the placement of analog victims from the digital aggressors. The procedure is validated by a design of LNA and ring oscillator in 0.18um TSMC CMOS process.*

I. Introduction

Substrate coupling in mixed-signal/RF CMOS ICs prevents the integration of sensitive analog/RF circuits with noisy digital circuits if it is not well characterized. The substrate models can be obtained by finite difference methods [**?**], stabilized multi-layer Green's function [], and scalable curve fitting [**?**] or surface potential method [**?**]. These methods are either expensive to use, difficult to be realized as macro-model, or takes tremendous time to build. Moreover, there is no efficient procedure to produce the profile for the coupling noise for large number of contacts.

In this paper, the focus is on the accurate macro-model for the substrate noise coupling and an efficient linear programming verification procedure to present the noise figure at each contact. The model is applicable

The rest of the paper is organized as follows. In Section II, we first present the preliminary of substrate RC mesh extraction, where we discuss the regularity of the extracted G, C matrices. In Section III, we discuss a novel block-structure model reduction based on regularity structure of G, C matrices. A MIMO realization is also presented. In Section IV, with the realized MIMO macro-model, we reformulate the verification of voltage profile at each contact as a linear programming program. In Section V, to improve the efficiency during verification, we further discuss a structured partition for the realized MIMO model. The experiment results are presented in Section VI, and we concludes the paper with discussion in Section VII.

II. Regularity of Substrate Mesh Network

The substrate outside of active/contact areas can be treated as uniformly doped layer, where a quasi-static Maxwell's equation is:

$$\epsilon\frac{\partial}{\partial t}(\nabla\cdot E)+\frac{1}{\rho}(\nabla\cdot E)=0 \tag{1}$$

where the displacement current term is ignored as we assume the substrate is lightly doped, where the conduction current is dominated. The circuit equation in matrix form can be obtained:

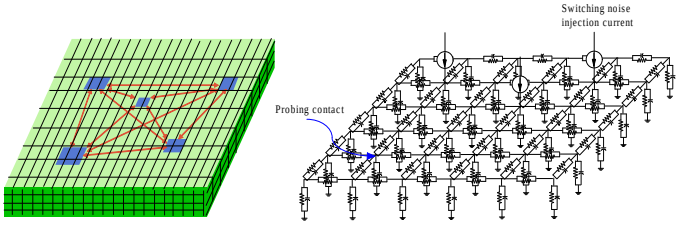

Fig. 1. The regularity of structured substrate RC mesh network.

$$\sum_j[\frac{V_i-V_j}{R_{ij}}+C_{ij}(\frac{\partial V_i}{\partial t}-\frac{\partial V_j}{\partial t})]=0 \tag{2}$$

Clearly, the model has a regular mesh topology. Then discuss the injection current noise (by switching), and the contact placements for victim circuits. Therefore, it brings challenges: i) the obviously large size of model needs more efficient model reduction; ii) the large number of ports (mostly are observation ports) needs explore the regularity. Note that the correlation between partitioned system can not be ignored.

III. Block-structured Model Reduction

The results in [**?**] can be naturally extensible to partitions other than 2-by-2. Consider a linear system in frequency domain:

$$\begin{aligned} Gx(s)+sCx(s)&=Bv_p\\ i_p&=B^Tx(s)\end{aligned} \tag{3}$$

where G, C the are conductance and capacitance matrices $(n\times n)$, $x(s)$ is the state variable, B is the incidence matrix at ports (n_p ports), and i_p, u_p are the port current/voltage variables. Suppose we have the following partitions:

$$B=\begin{bmatrix} B_{1(n_p\times n_1)}\\ B_{2(n_p\times n_2)}\\ \vdots\\ B_{d(n_p\times n_d)}\end{bmatrix},\quad G=\begin{bmatrix} G_{11} & G_{12} & \dots & G_{1d}\\ G_{21} & G_{22} & \dots & G_{2d}\\ \vdots & \vdots & \ddots & \vdots\\ G_{d1} & G_{d2} & \vdots & G_{dd}\end{bmatrix} \tag{4}$$

and similarly for A, C, and L, where $\sum_{n_i}=n$. By applying PRIMA we obtain the qth-order of basis matrix V_q. We further partition V_q according to the block size of G:

$$V_d^{(q)}=\begin{bmatrix} V_{1(n_p\times n_1)}\\ V_{2(n_p\times n_2)}\\ \vdots\\ V_{d(n_p\times n_d)}\end{bmatrix} \tag{5}$$

and reconstruct it to

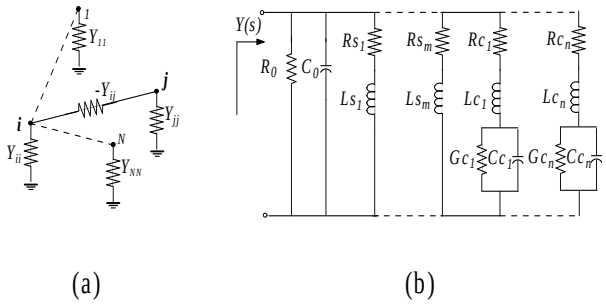

Fig. 2. (a) The MIMO realization of reduced model by modified Foster's synthesis; (b) The realized RLCG circuit of one branch admittance.

$$\widetilde{V}_d^{(q)} = \begin{bmatrix} V_{1(n_p \times n_1)} & 0 & \cdots & 0 \\ 0 & V_{2(n_p \times n_2)} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & V_{d(n_p \times n_d)} \end{bmatrix} \tag{6}$$

and we can obtain the order reduced state matrices by projecting $\widetilde{V}_d$:

$$\widetilde{G}_d = \widetilde{V}_d^{(q)\,T} G \widetilde{V}_d^{(q)}, \qquad \widetilde{C}_d = \widetilde{V}_d^{(q)\,T} C \widetilde{V}, \qquad \widetilde{B}_d = \widetilde{V}_d^{(q)\,T} B. \tag{7}$$

We can obtain a reduced model that can match at least twice poles as PRIMA such that the reduction efficiency is improved. Furthermore, this structured model reduction can preserve the block structure of the original system.

The transfer function of the reduced system is:

$$Y'(s) = \begin{bmatrix} Y'_{1,1} & \cdots & Y'_{1,n_p} \\ \vdots & \vdots & \vdots \\ Y'_{n_p,1} & \cdots & Y'_{n_p,n_p} \end{bmatrix} \tag{8}$$

where

$$Y'_{i,j} = c^{i,j} + \sum_{m=1}^{q} \frac{k_i^{i,j}}{s - p_m}, \tag{9}$$

q is the number of poles (model order) for the approximation, k_i and p_i are the residues and poles. It can be realized according to Fig. **??**, where

$$Y_{ii} = \sum_{j=1}^{n_p} Y'_{ij}, \qquad Y_{ij} = -Y'_{ij} \tag{10}$$

Experiments compare the waveform accuracy of different structure sized circuits.

IV. Correlation-considered Partition

Unfortunately the efficiency of the reduced model degrades as the number of external ports to the circuits increases. Partition is a technique which divides a circuit into parts, obtains solutions for the parts and combines these partial solutions to find a global solution. It converts a large problem into a number of smaller problems which can be solved separately.

Assume the original system is divided into K subdivisions. Usually for if the original matrix is structured, there will be $K-1$ to be identical sub-matrices ($\mathbf{Y}_k$) but the last one is always different as it is the *global connection circuit* ($\mathbf{Y}_0$) as the common interconnection. For the kth partitioned block, we have following nodal equation

$$\mathbf{Y}_k V_k = I_k + \widetilde{I}_k \tag{11}$$

where V_k, I_k are nodal voltage and current vector at ports of kth partition, and $\widetilde{I}_k$ is the correlation current from the other partitioned block through the interconnection block. We also have following branch equation at interconnection network

$$\mathbf{Y}_0 V_0 = I_0 \tag{12}$$

where $\mathbf{Y}_0$ is the impedance of branches at interconnection network, and V_c and I_c are branch voltage and current vectors.Note that the nodal voltage/ current vectors V_k /I_k of partitioned block are related to the branch voltage voltage /current vectors V_c/I_c of interconnection block:

$$\widetilde{I}_k = C_{k0} I_0, \qquad V_0 = -\sum_{k=1}^{K} C_{k0}^T V_k \tag{13}$$

Therefore, we have following hybrid matrix equation

$$\begin{bmatrix} \mathbf{Y}_1 & 0 & \cdots & 0 & -C_{10} \\ 0 & \mathbf{Y}_2 & \cdots & 0 & -C_{20} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 0 & \mathbf{Y}_K & -C_{K0} \\ C_{10}^T & C_{20}^T & \cdots & C_{K0}^T & \mathbf{Y}_0^{-1} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_K \\ I_0 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_K \\ 0 \end{bmatrix} \tag{14}$$

The block current I_k then can be solved

$$I_k = \sum_{l=1}^{K} \mathcal{Y}_{kl} V_l = \mathcal{Y}_k V \tag{15}$$

where the impedance of interconnection block and each partitioned block is modified

$$\mathcal{Y}_{kk} = \mathbf{Y}_k + C_{k0} \mathbf{Y}_0 C_{k0}^T \tag{16}$$

$$\mathcal{Y}_{kl} = C_{k0} \mathbf{Y}_0 C_{l0}^T \tag{17}$$

V. Robustness Verification

The frequency domain response at the ports of kth partitioned block is:

$$(\frac{V(s)}{V_{DD}})\mathcal{Y}_k(s) = \frac{I_k(s)}{V_{DD}} = \frac{P_k(s)}{V_{DD}^2} \tag{18}$$

where $I(s)$, $P(s)$ are ports' voltage, current responses and power densities (total power distributed by block area), and V_{DD} is the supply voltage. Usually, the power density can be specified/estimated by the designers during the pre-design stages. Therefore, we can give a upper bound as the peak current constraints such that: $I_k(s) \le I_{k0}, s_{min} \le s \le s_{max}$, or $P_k(s) \le P_{k0}, s_{min} \le s \le s_{max}$. Note that

$$(\frac{V(s)}{V_{DD}})\mathcal{Y}_k(s) \le |(\frac{V(s)}{V_{DD}})||\mathcal{Y}_k(s)| \tag{19}$$

Therefore, if we define

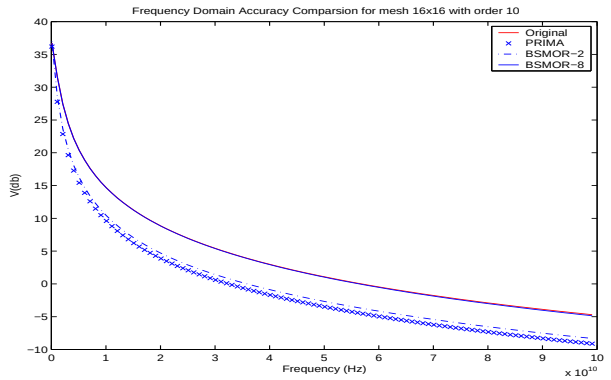

Fig. 3. Frequency response of structured model reduction, Prima, and original model at one port of a 16x16 RC-mesh

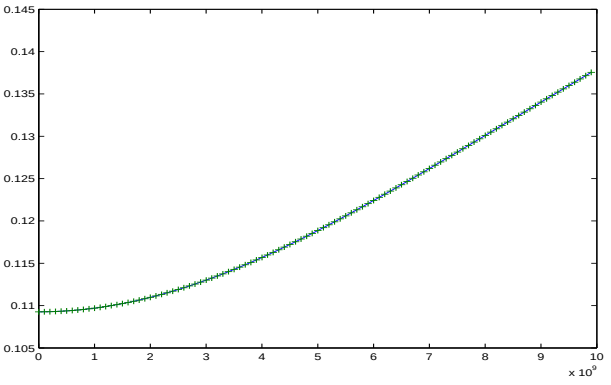

Fig. 4. Frequency response of partitioned and flatten model response at one port of 16x16 RC-mesh

$$x = |(\frac{V(s)}{V_{DD}})|, \qquad M = |\mathcal{Y}_k(s)|, \qquad b = \frac{I_{k0}}{V_{DD}} = \frac{P_{k0}}{V_{DD}^2} \tag{20}$$

then we can formulate the following equivalent problem to verify the robustness of the design of power ground plane: *Check if* $x \leq 1$ *is satisfied for all vectors* x *that satisfies* $Mx < b, x \geq 0$.

As these constraints are linear, we can construct the following linear programing (LP) to check the robustness at each block.

Experiments show partitions without/with consideration of the correlation of different partitioned systems.

VI. Experiment

A. Substrate Noise

1) Substrate Noise: Geometry:
Technology (material):
FastHenry mesh extraction:

2) Switching Circuit: ISCAS-logic (C432):
Maximum current evaluation:

3) Analog Block: LC-Oscillator, or VCO. Place VCO at different grid locations to see the magnitude of the noise. (1) frequency domain verification; (2) time domain effect.

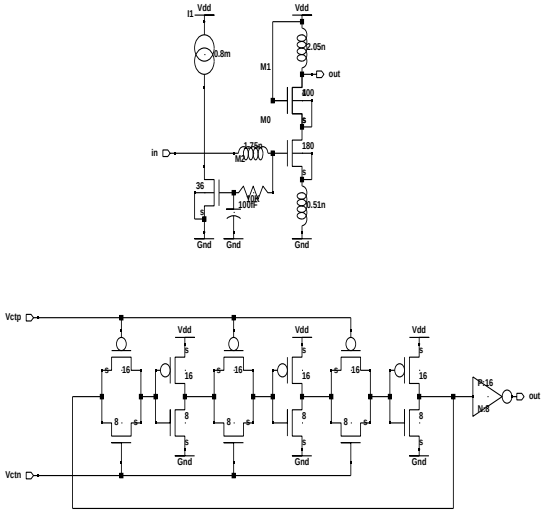

Fig. 5. (a) a low noise amplifier as victim; (b) ring oscillator as noise injection source

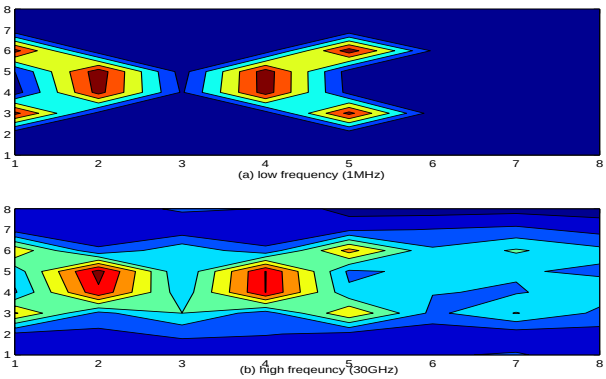

Fig. 6. A noise map of 16x16 mesh with 8x8 contacts array

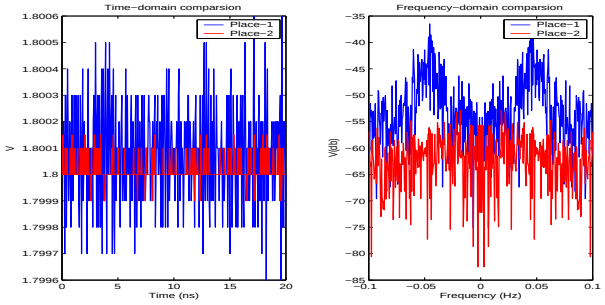

Fig. 7. The frequency/time-domain responses of LNA output when placed at two different locations