An Efficient Substrate Coupling Noise Verification with Blocked Structure-Model-Reduction and Partition

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Abstract*— *An efficient yet accurate substrate coupling-noise versification procedure has been developed. A novel block-structured model reduction is used to improve the model reduction efficiency. The reduced macro-model is then partitioned with the consideration of correlation among each port. Furthermore, the verification of coupling-noise voltage at each probing contact (for placing sensitive modules) is reformulated as a linear optimization procedure under user-supplied local and global current constraints. One by-product during the verification can be further used to guide the placement of analog victims from the digital aggressors. The procedure is validated by a design of LNA and ring oscillator in 0.18um TSMC CMOS process.

I. Introduction

Substrate coupling in mixed-signal/RF CMOS ICs prevents the integration of sensitive analog/RF circuits with noisy digital circuits if it is not well characterized. The substrate models can be obtained by finite difference methods [1], stabilized multi-layer Green's function [2], and scalable curve fitting [3], [4]. These methods are either expensive to use due to the large model size, difficult to be analyzed for arbitrary geometries, or takes tremendous time to build. Moreover, there is no efficient procedure to produce a profile of the coupling noise to guide the placement of sensitive analog/RF modules as there could exist a large number of possible contact locations.

To reduce the complexity of a passive network, Krylov-subspace projection based model reduction is usually applied [5] by implicit moment matching for dominant poles. However, this method loses its advantage when handling structured network like the substrate plane or Power/Ground grid, where i) the produced model is not compact as the order is usually observed "too high"; and ii) the reduction process is not efficient when there exists large number of ports. An alternate model reduction by truncated balanced realization (TBR) is proposed in [6]. This approach applies SVD decomposition to truncate less dominant states and achieve a more compact model. The drawback of this approach is the computation may become expensive as several expensive numerical techniques needs to be applied to diagonalize the overall state matrix, and guarantee the passivity. Recently, a structured model reduction is proposed by Freund in [7], where the regularity of the model structure is exploited to improve the moment-matching efficiency. This approach only discusses a 2×2 partition of the state matrix, i.e., the natural decomposition of conductance, capacitance, inductance, and adjacent matrices. The regularity of structured system is not yet sufficiently exploited during the moment matching.

In this paper, we present an efficient substrate noise verification procedure to guide the placement of sensitive analog module with the switching noisy digital module. An $n \times n$ structured model reduction to further improve the model reduction efficiency, and apply the macro-model during a linear programming based verification of the substrate coupling noise. To alleviate the complexity introduced by large number of ports during the verification, the macro-model is further partitioned with consideration of the correlation between each coupled partition. The produced the coupling noise profile is applied to guide the placement of a LNA (low noise amplifier) together with a switching block of ring oscillators.

The rest of the paper is organized as follows. In Section II, we first present the preliminary of substrate RC mesh extraction, where we discuss the regularity of the extracted G, C matrices. In Section III, we discuss a novel block-structure model reduction based on regularity structure of G, C matrices. A MIMO realization is also presented. In Section IV, we present a correlation considered circuit partition of the resulting macro-model to accelerate the following LP verification procedure. With a partitioned and reduced macro-model, in Section V, we reformulate the verification of voltage profile at each contact port as a linear programming program at each block. We present the experiment results in Section VI, and concludes the paper with discussion in Section VII.

II. Regularity of Substrate Mesh Network

The substrate outside of active/contact areas can be treated as uniformly doped layer, where a quasi-static Maxwell's equation is:

$$\epsilon \frac{\partial}{\partial t}(\nabla \cdot E) + \frac{1}{\rho}(\nabla \cdot E) = 0 \tag{1}$$

The Eddy current term (the primary cause of substrate loss) is ignored as we assume the substrate is highly doped, where the conduction current is dominant. It is sufficient for analyzing the problem of substrate coupling noise under this assumption [1], [2]. Note that (1) can be discretized on the substrate volume in differential form using finite difference or integral form using BEM boundary element methods. Because the BEM method needs find a numerical stable multi-layer Green's function [2], it is difficult in general when the layout geometry is arbitrary. In this paper, the finite difference based discretization is used to generate the model. The circuit equation in matrix form can be obtained:

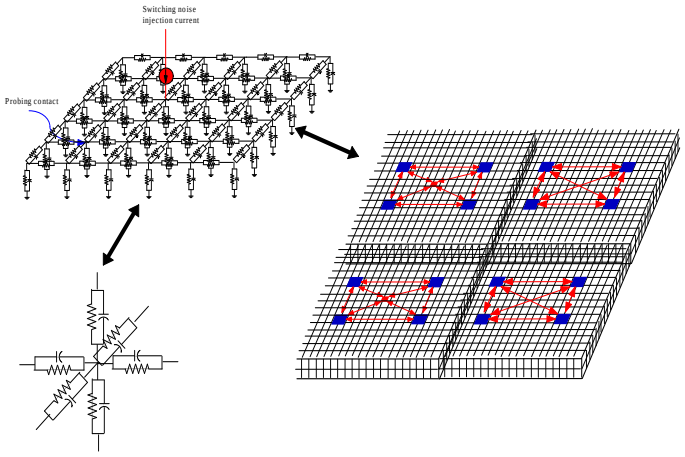

Fig. 1. The regularity of structured substrate RC mesh network.

$$\sum_j [\frac{V_i - V_j}{R_{ij}} + C_{ij}(\frac{\partial V_i}{\partial t} - \frac{\partial V_j}{\partial t})] = 0 \tag{2}$$

Clearly as shown in Fig.1, this model results in a regular RC-mesh topology, i.e., there are large number of repeatable RC sub-network. Since the size of the resulting RC mesh network is large, we apply the model reduction technique with consideration of the regularity from the original model as discussed below.

III. Block-structured Model Reduction

Consider a linear system in frequency domain:

$$\begin{aligned} Gx(s) + sCx(s) &= Bv_p \\ i_p &= B^T x(s) \end{aligned} \tag{3}$$

where G, C the are conductance and capacitance matrices ($N \times N$), $x(s)$ is the state variable, B is the incidence matrix at ports (n_p ports), and i_p, u_p are the port current/voltage variables. Suppose we have the following partition according to the regularity of the RC network (See Fig. 1):

$$B = \begin{bmatrix} B_{1(n_p \times n_1)} \\ B_{2(n_p \times n_2)} \\ \vdots \\ B_{d(n_p \times n_d)} \end{bmatrix}, \quad G = \begin{bmatrix} G_{11} & G_{12} & \dots & G_{1d} \\ G_{21} & G_{22} & \dots & G_{2d} \\ \vdots & \vdots & \ddots & \vdots \\ G_{d1} & G_{d2} & \vdots & G_{dd} \end{bmatrix} \tag{4}$$

and similarly for A, C, and L, where $\sum n_i = N$. By applying PRIMA we obtain the qth-order of basis matrix V_q. We further partition V_q according to the block size of G:

$$V_d^{(q)} = \begin{bmatrix} V_{1(n_p \times n_1)} \\ V_{2(n_p \times n_2)} \\ \vdots \\ V_{d(n_p \times n_d)} \end{bmatrix} \tag{5}$$

and reconstruct it to

$$\widetilde{V}_d^{(q)} = \begin{bmatrix} V_{1(N_p \times n_1)} & 0 & \dots & 0 \\ 0 & V_{2(n_p \times n_2)} & \dots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \dots & V_{d(n_p \times n_d)} \end{bmatrix} \tag{6}$$

We can obtain the order reduced state matrices by projecting $\widetilde{V}_d$:

$$\widetilde{G}_d = \widetilde{V}_d^{(q)T} G \widetilde{V}_d^{(q)}, \qquad \widetilde{C}_d = \widetilde{V}_d^{(q)T} C \widetilde{V}, \qquad \widetilde{B}_d = \widetilde{V}_d^{(q)T} B. \tag{7}$$

Using such a matrix $\widetilde{V}_d$, we define a reduced-order model with following transfer function:

$$Y'(s) = \widetilde{B}_d^T (\widetilde{G}_d + s\widetilde{C}_d)\widetilde{B}_d \tag{8}$$

and we have following Theorem:

THEOREM.1 Let $\widetilde{V}_d$ be a matrix composed from (6), and $K_q(G^{-1}C, G^{-1}B)$ be the qth block Krylov subspace. If $K_q(G^{-1}C, G^{-1}B) \subseteq span(\widetilde{V}_d)$, then the first q moments in the expansion of Y and the projected Y' about s_0 are identical.

It is shown in [7] that the reduced model of passive network obtained by Krylov-subspace projection preserves passivity. Therefore, Y' projected by $\widetilde{V}_d$ is passive. Furthermore, as shown by experiment, with the partition of structured state matrices, a reduced model that can match at least twice poles as PRIMA, i.e., the reduction efficiency is improved. Note that this structured model reduction preserves the block structure of the original system such that it enables us to further apply an additional port-partition to the resulting macro-model.

The transfer function of the reduced system can be expanded in pole-residue form:

$$Y'(s) = \begin{bmatrix} Y'_{1,1} & \dots & Y'_{1,n_p} \\ \vdots & \vdots & \vdots \\ Y'_{n_p,1} & \dots & Y'_{n_p,n_p} \end{bmatrix} \tag{9}$$

with

$$Y'_{i,j} = c^{i,j} + \sum_{m=1}^{q} \frac{k_i^{i,j}}{s - p_m}, \tag{10}$$

where q is the number of poles (model order) for the approximation, k_i and p_i are the residues and poles. For the SPICE compatible time-domain simulation, we use a modified Foster's synthesis method illustrated in Fig. 2, where the admittance form is first changed into branch-admittance form:

$$Y_{ii} = \sum_{j=1}^{n_p} Y'_{ij}, \qquad Y_{ij} = -Y'_{ij} \tag{11}$$

We find that each branch-admittance can be realized as follows. Firstly, we rewrite Y_{ij} in the Foster's canonical form:

$$Y_{ij} = sY_{ij}^{(\infty)} + Y_{ij}^{(0)} + \sum_{m=1}^{M} \frac{a_m}{s - p_m} + \sum_{n=1}^{N} (\frac{a_n}{s - p_n} + \frac{a_n^*}{s - p_n^*}) \tag{12}$$

where we expand the rational function into the partial fraction form with N conjugate-poles p_n and M real-poles p_m. The admittance function in Foster's canonical-form can be then synthesized by an equivalent circuit in Fig. 2 with the following relations to determine R, L, C, G elements:

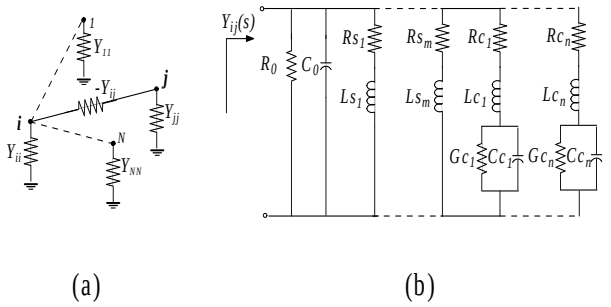

Fig. 2. (a) The MIMO realization of reduced model by modifi ed Foster's synthesis; (b) The realized RLCG circuit of one branch admittance.

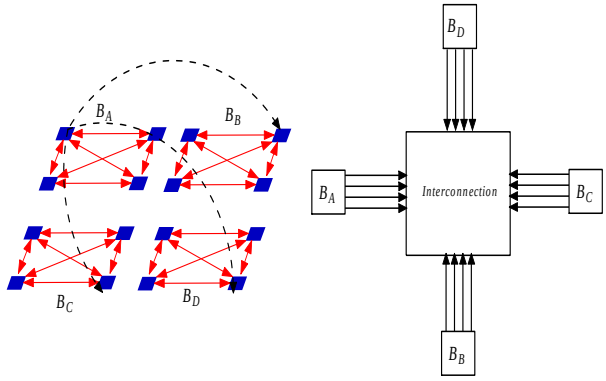

Fig. 3. Partition the coupled macro-model into sub-network blocks with a central interconnection block.

$$G_0 = Y_{ij}^{(0)}, \qquad C_0 = Y_{ij}^{(\infty)};$$
$$Rs_m = \tfrac{1}{a_m}, \qquad Ls_m = -\tfrac{p_m}{a_m};$$
$$Lc_n = \tfrac{1}{2Re\{a_n\}}, \qquad Lc_n Cc_n |p_n|^2 = Rc_n Gc_n + 1,$$
$$\tfrac{Gc_n}{Cc_n} = -\tfrac{Re\{a_n p_n^*\}}{Re\{a_n\}}, \qquad \tfrac{Rc_n}{Lc_n} = \tfrac{Re\{a_n p_n^*\}}{Re\{a_n\}} - 2Re\{p_n\} \quad (13)$$

IV. Correlation-considered Partition

To generate the order reduced macro-model, we need to first specify the interested ports. Usually, we specify i) the invoking ports: external voltage/current sources, and ii) the probing ports: interested observation points. When given digital switching module (the input ports), the possible locations, i.e., the observation ports to place the To place the sensitive analog module can be large. Unfortunately, the efficiency of the reduced model degrades as the number of external ports to the circuits increases. Partition is a technique which divides a circuit into parts, obtains solutions for the parts and combines these partial solutions to find a global solution. It converts a large problem into a number of smaller problems which can be solved separately.

As shown in Fig. 3, we assume the original system is divided into K subdivisions. Generally, if the original matrix is structured, there will be $K-1$ to be identical sub-matrices ($\mathbf{Y}^k$) but the last one is always different as it is the *global connection circuit* ($\mathbf{Y}^0$) for the common interconnection. For the kth partitioned block, we have following nodal equation

$$\mathbf{Y}^k v^k = i^k + \widetilde{i}^k \quad (14)$$

where v^k, i^k are nodal voltage and current vector at ports of kth partition, and $\widetilde{i}^k$ is the correlation current from the other partitioned block through the interconnection block. $\mathbf{Y}^k$ is a $n_k \times n_k$ branch-impedance matrix of the kth block.

Moreover, we also have following branch equation at interconnection network

$$\mathbf{Y}^0 v^0 = i^0 \quad (15)$$

where $\mathbf{Y}^0$ is the impedance of branches at interconnection network and it is a diagonal matrix. v^0 and i^0 are branch voltage and current vectors. Furthermore, the nodal voltage/ current vectors v^k /i^k of partitioned block are related to the branch voltage voltage /current vectors v^0/i^0 of interconnection block:

$$\widetilde{i}^k = C^{k0} i^0, \qquad v^0 = -\sum_{k=1}^{K} (C^{k0})^T v^k \quad (16)$$

where C^{k0} is the connection matrix composed by $\{0, 1, -1\}$ to indicate the direction of branch currents between kth partitioned block and the interconnection block. It is a sparse matrix in general. Therefore, we have following hybrid matrix equation

$$\begin{bmatrix} \mathbf{Y}^1 & 0 & \cdots & 0 & -C^{10} \\ 0 & \mathbf{Y}^2 & \cdots & 0 & -C^{20} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 0 & \mathbf{Y}^K & -C^{K0} \\ (C^{10})^T & (C^{20})^T & \cdots & (C^{K0})^T & \mathbf{Y}^{0-1} \end{bmatrix} \begin{bmatrix} v^1 \\ v^2 \\ \vdots \\ v^K \\ i^0 \end{bmatrix} = \begin{bmatrix} i^1 \\ i^2 \\ \vdots \\ i^K \\ 0 \end{bmatrix} \quad (17)$$

The block current I^k then can be solved

$$i^k = \sum_{l=1}^{K} \mathcal{Y}^{kl} v^l = \mathcal{Y}^k v \quad (18)$$

where $\mathcal{Y}^k$ is a newly constructed impedance matrix that is much sparser than the original densely coupled port matrix Y. Note that the impedance of interconnection block and each partitioned block are modified

$$\mathcal{Y}^{kk} = \mathbf{Y}^k + C^{k0} \mathbf{Y}^0 (C^{k0})^T \quad (19)$$
$$\mathcal{Y}^{kl} = C^{k0} \mathbf{Y}^0 (C^{l0})^T \quad (20)$$

Because $\mathbf{Y}^0$ is a diagonal matrix, and C^{k0} is sparse in general, the computation of (20) is observed not expensive. With the partitioned block I-V relation (18), we further formulate a linear programming program as discussed below to calculate the maximum voltage bounce at each probing port when the maximum currents are specified for each partitioned block.

V. Robustness Verification

For the current sources in each partitioned block with size n_k, we can specify a fixed current envelope I_j^k for the jth current source $i_j^k(s)$ such that $i_j^k(s) \leq I_j^k (s_{min} \leq s \leq s_{max})$. Note that such a upper-bound envelope current can be

obtained from the prior simulation by the event-driven based characterization [8] of the switching currents in each block.

Furthermore, we can observe the following *monotonicity* for a RC network:

PROPOSITION.1 When the G, C matrices are symmetric and positive definite (s.p.d.), then the substrate RC-network obeys:

$$\begin{aligned} if \quad & i_1(s) \geq i_2(s), \forall s \geq 0, \\ then \quad & v_1(s) \geq v_2(s), \forall s \geq 0 \end{aligned} \tag{21}$$

i.e., the substrate RC-network is monotone.

Based on this monotonicity, it is obvious to obtain the maximum voltage bounce under a specified maximum current envelope for each current source. However, with only such a "local constraints" the result can be very pessimistic as it seldom happens that the substrate network simultaneously draws all the maximum switching currents. Therefore, it needs further specify a "global" constant for each partitioned block:

$$U^k i^k(s) \leq Ig^k \tag{22}$$

where U^k is a unit-one vector with size n_k. Note that such a block current Ig^k can be simply calculated from the power density (the power divided by the block area), or statistically estimated [9] by the designers during the pre-design stage.

With the use of the monotonicity, we have the following combined static unequal constrains:

$$\begin{bmatrix} \mathcal{G}^k_{11} & \cdots & \mathcal{G}^k_{1N} \\ \vdots & \ddots & \vdots \\ \mathcal{G}^k_{N1} & \cdots & \mathcal{G}^k_{NN} \\ \sum_j \mathcal{G}^k_{j1} & \cdots & \sum_j \mathcal{G}^k_{j1} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} I^k_1 \\ \vdots \\ I^k_{n_k} \\ Ig^k \end{bmatrix} \tag{23}$$

where $\mathcal{G}^k = Re\{\mathcal{Y}^k\}$ is the *dc* conductance matrix. By a normalization procedure,

$$\begin{aligned} x^k &= \frac{V^k}{V_{target}}, \qquad M^k = r\mathcal{G}^k \\ b^k &= \frac{I^k}{I_{max}}, \qquad r = \frac{V_{target}}{I_{max}} \end{aligned} \tag{24}$$

we can formulate a robustness verification as below:

DEFINITION.1 A substrate RC-network is robust by checking if $x \leq 1$ is satisfied for all vectors x that satisfies $Mx < b, x \geq 0$, i.e., all the maximum voltage bounce are below the user specified target voltage V_{target}.

As these constraints are linear, we can construct the following linear programing (LP) to check the robustness at each block, i.e.,

$$\begin{aligned} max \quad & x^k_i \\ s.b.t. \quad & M^k x^k \leq b^k \\ & x^k \geq 0 \end{aligned} \tag{25}$$

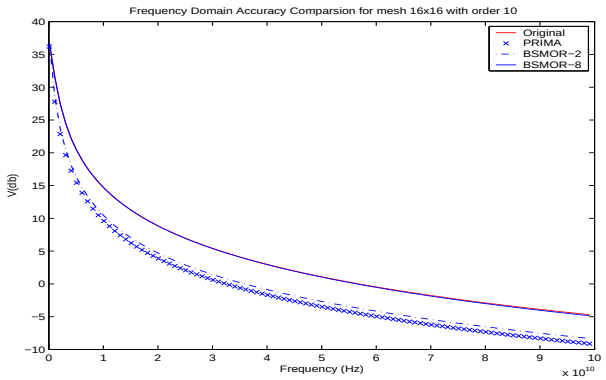

Fig. 4. Frequency response of structured model reduction, Prima, and original model at one port of a 16x16 RC-mesh.

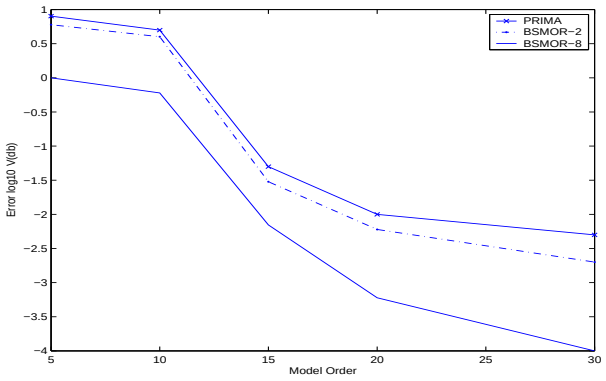

Fig. 5. Error of frequency response of structured model reduction and Prima for increasing order models on the 16x16 RC-mesh.

As proved in [10], it is a sufficient condition for the substrate network to be robust when it passes the above verification.

VI. Experiment

In this part, we first present the performance of the $n \times n$ blocked structure-model-reduction, correlation-considered partition, and LP verification procedure. Then, we present an application of this verification flow to a placement of LNA with switching ring oscillators.

For a 16×16 RC-mesh (10K circuit elements), Fig. 4 shows the accuracy comparison of frequency response at one port among the original one (10K circuit elements), and reduced models by PRIMA, 2×2 structured-reduction (SPRIM), and an 8×8 structured-reduction. All the reduced models are in the same order of 10, and realized by Fig. 2. Clearly, with 10th iteration the 8×8 structured-reduction converges with the original circuit response but PRIMA and 2×2 structured-reduction are still not converged.

We further compare the accuracy of the verification procedure by the flatten, the partitioned macro-model without consideration of the correlation, the partitioned macro-model with consideration of the correlation up to nearest neighbor, and the partitioned macro-model with consideration of all the correlation in (20). As shown in Fig. 6, the verification without consideration of correlation at all can leads to nonnegotiable error, and the verification with consideration of all correlation

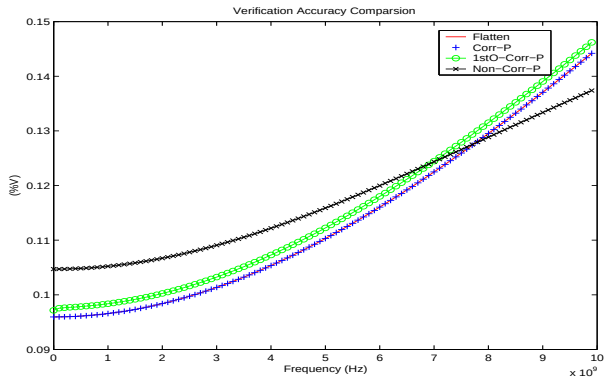

Fig. 6. LP-verification of substrate coupling noise of the partitioned and flatten model response on the 16x16 RC-mesh.

has the identical results as the flatten verification. However, because the constraint matrix (see (25)) size is much reduced by partition, the partitioned verification achieves 10X times (8.32s vs 81.12s) verification speedup compared to the flatten one. Note that the verification process by considering the nearest neighbor correlation has less than 3% waveform difference, but it can saves the partition time by 2 times (1.24s vs 0.63s).

Table I and II further studies the runtime scalability of the reduced model for verification, and the effect of choosing the partition size. Discuss more with more data ...

We then apply the partitioned verification result to guide the placement a sensitive LNA with two frequency-varying ring oscillation as shown in Fig. 7. Note that the frequency of the ring oscillator can be changed by varying the controlling voltage Vctn(p). The substrate considered here is a $3mm \times 3mm$ plane with $10um$ thick epi-layer ($10Ohm - cm$) and $200um$ thick p-type substrate ($0.01Ohm - cm$).

Fig. 8 shows the noise (voltage bounce magnitude) map of the substrate with 8×8 possible locations for placing the contact for the LNA. The two ring oscillator are located bat (2,4) and (4,4). By controlling their voltage Vctn(p) we obtain different switching current injecting at at 100MHz and 10GHz respectively. The maximum currents are characterized in time domain and then FFT is used to obtain the current envelope in frequency domain. With the detailed information of the noise distribution, we place the LNA at two locations: (7,2) and (5,2). According the noise map, the noise (7,2) at both frequency points are much smaller than the cases for (5,2). This observation is confirmed by the direct SPICE simulation results. As shown in Fig. 10, we observed the substrate noise at (7,2) is about 20db lower when placing the LNA at location of (5,2).

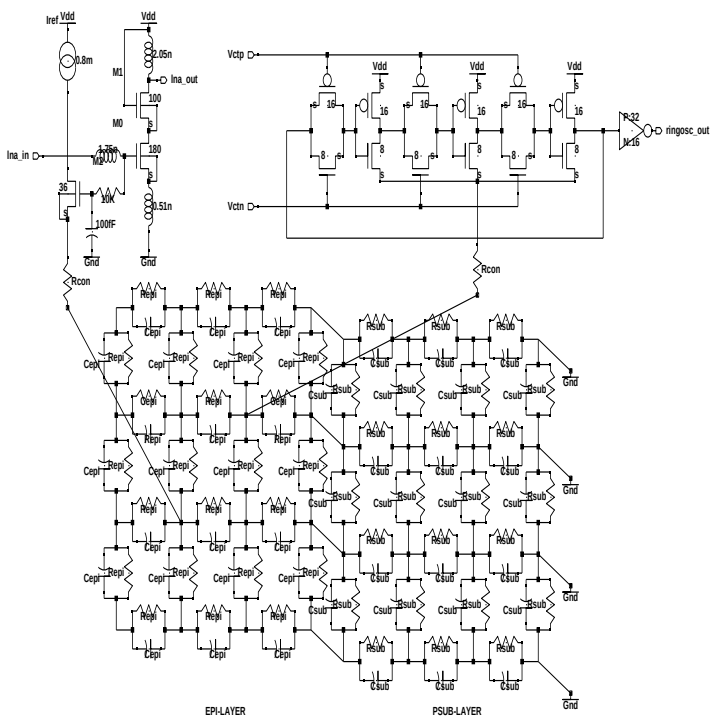

Fig. 7. (a) a low noise amplifier as victim; (b) frequency-variant ring oscillator as noise injection source.

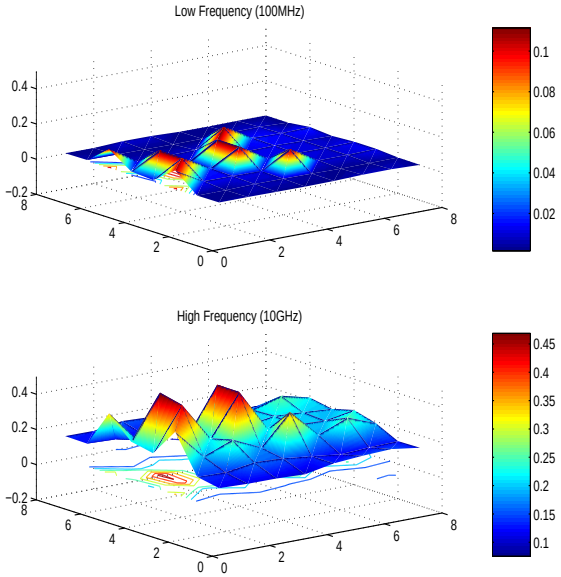

Fig. 8. A noise map with 8x8 contacts array injected by two frequency-controllable ring oscillators at low and high frequency.

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TABLE I

VERIFICATION EFFICIENCY COMPARISON BETWEEN FLATTEN AND PARTITIONED MODELS.

Ckts	Verify w reduction+partition						Brute-force Verify	
	Redu-port#	Redu-time	Parti-sz	Parti-time	Vfy-time	Vfy-vio-#	Vfy-time	Vfy-vio-#
ckt#1(10K)	16	8.32s	4	1.24s	0.81s	3	81.12s	3
ckt#1(20K)	32	24.88s	8	2.11s	1.32s	8	276.45s	7
ckt#1(80K)	64	87.89s	16	10.19s	12.92s	19	1925.87s	21

TABLE II

VERIFICATION EFFICIENCY COMPARISON BY VARYING THE PARTITIONED BLOCK SIZE.

Ckts	Part Size											
	$\frac{1}{16}N$			$\frac{1}{8}N$			$\frac{1}{4}N$			No Part		
	Parti-time	Vfy-time	Vio #	Parti-time	Vfy-time	Vio #	Parti-time	Vfy-time	Vio #	Part time	Vfy time	Vio #
ckt#1(20K to 32p)	6.89s	0.34s	7	4.28s	0.82s	8	2.11s	1.32s	8	NA	16.98s	7
ckt#1(80K to 64p)	20.80s	3.14s	21	14.26s	8.86s	20	10.19s	12.92s	19	NA	528.57s	21

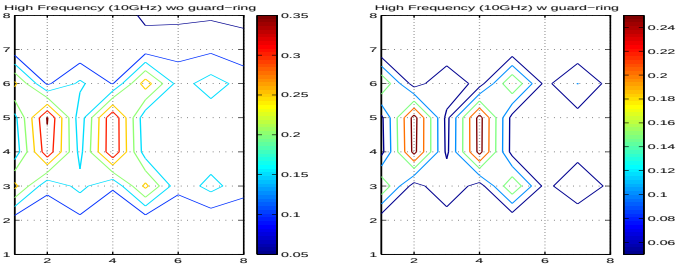

Fig. 9. Contour of above noise map at high frequency with/without guard rings.

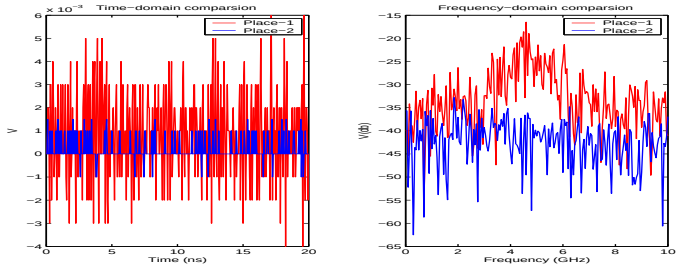

Fig. 10. The frequency/time-domain responses of LNA output when placed at two different locations (5,2) and (7,2).

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