

Micro architecture-level power estimation and cycle accurate simulation:

Below is the summary of what we have discussed:

$$P_{total} = \sum_{i \in MODUAL} \int R_i(l) \left(\frac{P}{l} \right) (\alpha_i, Vdd_i, Vth_i, f_i) dl + \sum_{j \in BUS} \left(\frac{P}{l} \right) (\alpha_j, Vdd_j, Vth_j, f_j) L_j$$

where R is the Rent's rule wire length distribution function;

$\left(\frac{P}{l} \right)$ is the unit length power function and it is a function of the switching activity,

Vdd , Vth , and delay slack, which depends on the target delay and the wire-length;

α is the switching activity;

f is the % delay slack.

In Weiping's paper, three tiers of wires are considered whereas in the ISLPED paper, only one type of wire is assumed. I will assume there is only one type of wire for simplicity in the first place and pls let me know if adjustments need to be made to fix this. Weiping has three types of models for repeater insertion and based on his conclusion, the hybrid model is the best, which is also confirmed in one of the book that Weiping referred me to check out. This could be considered later when the integration of the two parts is completed. Weiping has checked in his program so I will start looking into it.