Weekly Report Cynthia

The code for the full chip interconnect power from the ISLPED paper is modified so that it now computes interconnect power for each module and buses, weight them with the respective number of accesses and switches, and then sum them up. The total access and total switch of the modules and buses are obtained from using Weiping's gcc benchmark.

One issue occurred from breaking down into modules is that the majority of the wire-length is too short to be considered. One of the reasons is that the lmin we assume currently is the delay optimal insertion length, which is quite large. The current interconnect power for all modules is almost zero and the bus power is less than one watt. This is quite different from Weiping's result which is on the order of 10 Watts. This is because we ignored the power from the interconnects that does not require buffers. Please let me know if I should modify the current setting for lmin.