This week driver sizing with and without buffer load is studied. Below is the summary of the derivation so far.

Case I. Cascaded driver for wire without buffers

Driver design variables: n - number of stage
u– stage ratio

Size of first stage, s_1, is assumed to be 4x.
The number of stages range from 1 to 5 and for each number of stages, the corresponding stage ratio, u, that satisfies the delay target, D_{target} is solved. Then n and u are plugged into the power equations to obtain the power.

The equations for delay and power are given below.

$$nr_s c_p + (n-1)ur_s c_o + \frac{r_s}{s_1 u^{n-1}}cL + \frac{1}{2}cL^2 = D_{t\,arg\,et}$$

$$P_{tot} = P_{dyn} + P_{lkg} + P_{sc}$$

$$P_{dyn} = aV_{dd}^2 f_{clk}(s_1 c_p + (c_o + c_p)\sum_{k=2}^{n} u^{k-1}s_1 + Lc)$$

$$P_{lkg} = \frac{1}{2}V_{dd}I_{off}\sum_{k=1}^{n} u^{k-1}s_1$$

$$P_{sc} = a\ln(3)V_{dd}W_{min}^{nmos}I_{sc}f_{clk}(\sum_{k=1}^{n} u^{k-1}s_1 \tau_k)$$

Case II. Cascaded drivers for wire with buffers

Assuming the target delay for a wire (D_{target}), the total wire length (L), the buffer size (s), the buffer insertion length (l), and the power optimal unit length delay (t_per_length) are given, we can solve for the distance between the driver and the first buffer (l') as well as the delay from the driver to the first buffer (D_1) in the following way.
l'=L-floor(L/l)*l
D_1=t_per_length*floor(L/l)*l
The reason of using floor is to have integer number of buffers. The delay and power equations for this case is very similar to that of the case I except D_{target} is replaced by D_1 and L is replaced by l' and there is an additional capacitive loading of c_os from the input capacitance of the first buffer.

Both of the cases have been implemented in Matlab and at this point, I am working on integrating case I and case II into the computation for full chip interconnect power.