Escape Routing Design to Reduce the Number of Layers in Area Array Packaging

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***Abstract*—High density multilayer substrate technologies are indispensable to accommodate high inputs/outputs (I/Os) fine pitch area array integrated circuits (ICs), chip scale packages/ball grid arrays (CSP/BGAs) in the coming packaging generation. They must provide not only a high wiring density, but also an acceptable low cost, short turn around time (TAT) and reliability. Reduction of the number of layers is expected to be a reasonable solution for the conflicting demands. General approaches to reduce the layer count have been to decrease the size of the routing line width and spacing. However, they need changes in the manufacturing processes and materials, causing an increased cost.**

From escape routing design viewpoint, effects of routing manner on the layer count has been studied. A preferential routing creates specific pad geometry resulting in a high wiring efficiency. This effect can be estimated with an increase in the number of lines per layer routable as a contribution of "the hybrid channel," depending on capture pad pitch-pad diameter-line width-interline space relationship. It is one of remarkable case recognized that, within one line per channel rule, the preferential routing can effect almost equivalent to that by two lines per channel on the wireability. Its better effect on cost and TAT can also be expected compared with the two thinner sized lines per channel rule, since nothing changed in both manufacturing processes and materials is needed. This method is applicable immediately and lightly to packages and boards for assembly of the high I/O flip chips, CSPs, and BGAs.

***Index Terms*—Area array, BGA, CSP, escape routing, flip chip, high density substrates, layer count, multilayer, packaging, preferential, the hybrid channel.**

I. Introduction

WITH THE insatiable market demand for higher performance electronic devices, the number of chip/package inputs/outputs (I/Os) has continuously been growing. To accommodate the higher I/Os, area array type interconnection between chip to package, chip to board, chip scale packaging (CSP) to board, or ball grid array (BGA) to board, is needed and tends practically to increase. In the circumstances, various sorts of multilayer high density substrates have been proposed. The higher I/O counts also requires an increase in their number of escape routing layers, resulting in a higher manufacturing cost of substrates used as a package or a board. Nevertheless, the market will never accept the higher cost caused by the increase in I/O counts. Additionally, an adequate reliability and short turn around time (TAT) should simultaneously be satisfied.

Reduction of the layer count will become an effective solution for the complicated requirements. Reducing the layer count is affected by wireability and the total wireability of a substrate is calculated as a product of the number of lines per channel, the number of channels per cm, and the number of signal planes [1]. Here, the channel represents a space between the adjoining pads. Generally, the number of channels per cm is previously determined by bump location on chip or footprint of package, and an increase in the number of lines per channel enables the number of layers to decrease.

In the conventional geometry of pad and line [2], the increasing the number of lines per channel can only be realized by a decrease in the size of the line, the space between the lines, and the line to capture pad space. These dimensional changes exposes the substrate to cost, yield and reliability issues, because some process modification toward unstable condition is needed. With substrates manufactured with one line per channel rule that their pad pith, capture pad diameter, line width and space are, respectively, 250 μm, 130 μm, 40 μm, 40 μm for flip chip connection, or 800 μm, 500 μm, 100 μm, 100 μm for CSP/BGA connection, for instance, the line width and space should become 24 μm, 24 μm for the former, and 60 μm, 60 μm for the latter for two line per channel rule when their pith and capture pad diameter are unaltered. In these cases, some new materials and new equipment, or new process technology will be necessary as well. Guinn *et al.* [3] have shown the trends in required area for packaging various devices depending on their number of I/Os, and pointed out that the progress in feature dimensional reduction technology of PWB (printed wiring board) is too slow compared with that of ICs.

An alternative method to reduce the layer counts without making any change in the manufacturing process is accordingly desired. This corresponds to considering an improvement in the escape routing design. Hirt *et al.* [4] analyzed the escape routing with multilayer structure according to the conventional procedure from a concentrated I/Os of area flip chip and BGA. Key issue here for the escaping is the restriction by "lines per channel" rule. Also in the rerouting structure from periphery I/Os to area I/Os shown by Darnauer *et al.*, limitation in the escape routing by the "lines per channel" rule has been emphasized. Reported approaches to reduce the layer count from the standpoint of the routing design, however, are very few. Gasparini *et al.* [6] have shown that the specific location of bumps on a silicon chip contributes to the routability. By incorporating their design method into the placement of the signal I/O, Andrews *et al.* [7] have succeeded to reduce the number of layers of an organic substrate for flip chip packaging without any change in line width and spaces. Their results suggest some improvement in the routing design may contribute to reducing the layer counts. Their method, however, requires

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some changes in pad allocation, not only on the substrate, but also on the corresponding IC. To realize an universality of a method applicable covering package to board interconnection, in which footprint is generally standardized, it is necessary to achieve the reduction of the layer counts with no change in the pad allocation on the interface. That would also be preferable from its total cost and TAT standpoint.

This paper describes the routing manner effective on reducing the layer counts in packages or boards for a given area array pad matrix on ICs, CSPs, or BGAs.

II. Approach

In the conventional escape routing manner for a typical square grid pad matrix, pads on an outermost row are routed out first, and then the pads on the next inner row are routed out through the channel. Thus the routing is performed in order from outer side row and the number of rows routable on a layer is determined by the number of lines per channel plus one, as shown in Fig. 1.

Compared with this, in the present study, effects of some change in the routing order on the wireability and the number of routing layers has been investigated. First of all, the routing priority is given to the inner pads on the specific vertical rows (marked with arrows in Figs. 4, 5 and 8) parallel to the routing out direction, followed by a preferential routing along the vertical rows with a given number of lines per channel. Here, a conception "hybrid channel" has been newly applied. While the conventional channel is made up by a pair of the pads adjacent to each other, the hybrid channel consists of a pair of the pads that the coordinate of the first land is (x, y) and the another pad is placed at the coordinate $(x + p(n-1), y)$ when the pad pith is p, as shown in Fig. 4. Here, n is determined to be a natural number larger than two. Effect of the preferential routing has been evaluated in comparison with the conventional routing manner; how many routing lines can be placed additionally per the hybrid channel compared with the conventional channel, depending on n, for various relations among pad pitch, pad diameter, line width and spacing. Subsequently, number of the layers needed has been estimated.

III. Model and Case Studies

A. Lines Per Channel

1) Effect of the Hybrid Channel: In the regular pad matrix as partially shown in Fig. 1, total number of the lines routable per channels formed with n pads and from pads surrounded by them, l, is given by (1). On the other hand, number of the lines routable per the hybrid channel, m, is given by (2)

$$l = \alpha(n-1) + (n-2) \tag{1}$$

$$m = (p(n-1) - d - s)/(w+s) \tag{2}$$

where

- p pad pitch;
- d diameter of the pad;
- w width of the line;
- s minimum space between the line and the pad, and is generally equal to minimum inter line space;

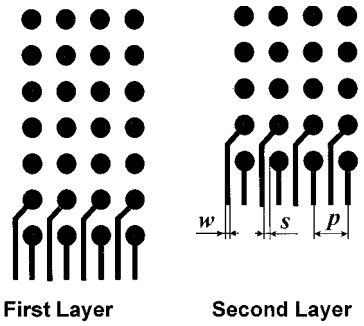

Fig. 1. Typical conventional routing structure on first and second layers.

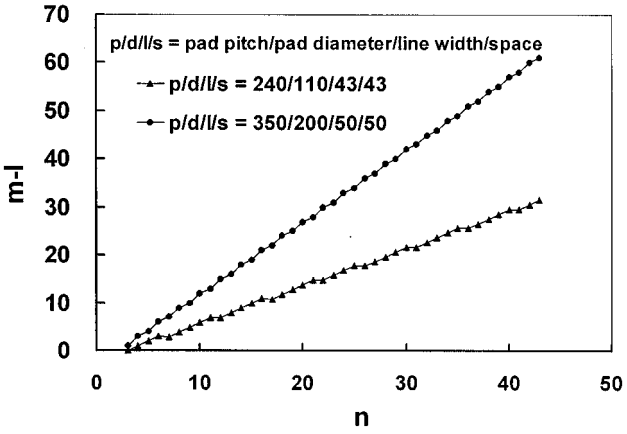

Fig. 2. Gain, $m - l$, per the hybrid channel as a function of n.

- n number of serial pads chosen;
- $n-1$ represents number of channels in serial n pads;
- $n-2$ represents number of pads inside the hybrid channel;
- α number of lines per channel;

given by

$$\alpha = (p - d - s)/(w + s).$$

In Fig. 1, a case of $n = 4$ is shown, in which l becomes five from three channels and two pads surrounded by the channels. When n chosen satisfies the relation $m \geq l + 1$, the hybrid channel effects on wireability. As n increase, gain, $m - l$, can be increased as shown in Fig. 2. This efficiency is, however, estimated merely for a restriction by pads in the first row.

2) Number of Lines Supplied to the Hybrid Channel: Since α is fixed, diagonal inter-pad space (diagonal channel) is only a source of the additional lines that are supplied toward the first row. The number of lines routable per the diagonal channel, D, is given by

$$D = (\sqrt{2}p - d - s)/(w + s). \tag{3}$$

In many cases with typical design rule of current wiring processes for one line per channel, D becomes 2 and, as the result, one additional line is obtainable per the channel.

When eliminated pads make rectangular space as shown in Fig. 3, only two diagonal channels are obtainable. Hence, the gain per the hybrid channel is limited into $2(D - \alpha)$, regardless of n and $m - l$. Number of the diagonal channels included in the hybrid channel need accordingly to be increased for the proper effect. The hybrid channels shaped an isosceles triangle,

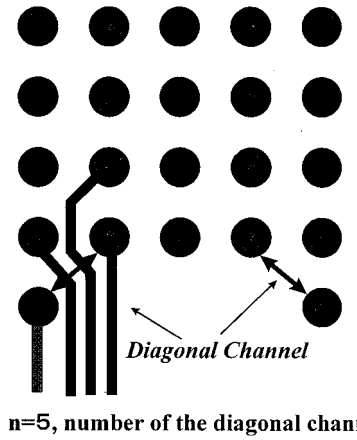

Fig. 3. Example of the channel in which eliminated pads make a rectangular space.

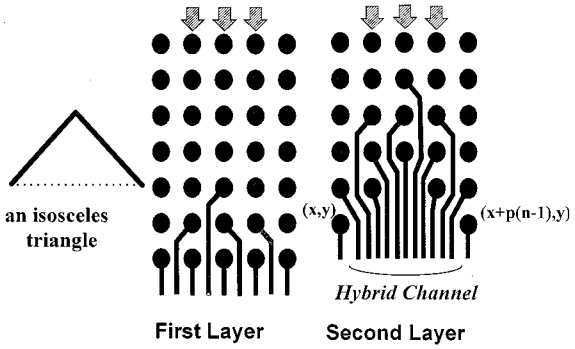

Fig. 4. Example of the preferential routing structure with the hybrid channel $(n = 5)$ shaped an isosceles triangle and a pad geometry obtained on the following layer.

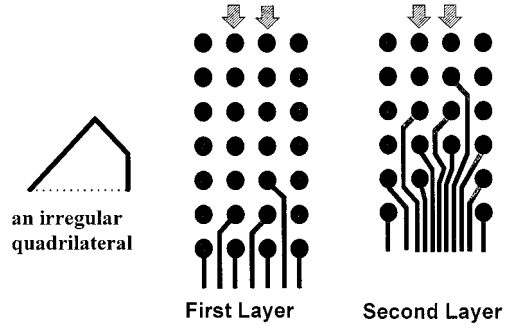

Fig. 5. Example of the preferential routing structure with the hybrid channel $(n = 4)$ shaped an irregular quadrilateral and a pad geometry obtained on the following layer.

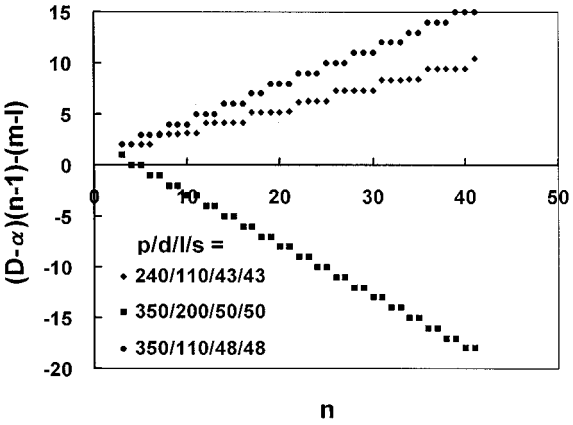

Fig. 6. Comparison between gain, $m-l$, and lines supplied, $(D-\alpha)(n-1)$, depending on n for pad pitch / pad diameter / line width / interline space combinations; 240/110/43/43, 350/200/50/50 ($\alpha = 1$), and 350/110/48/48 ($\alpha = 2$).

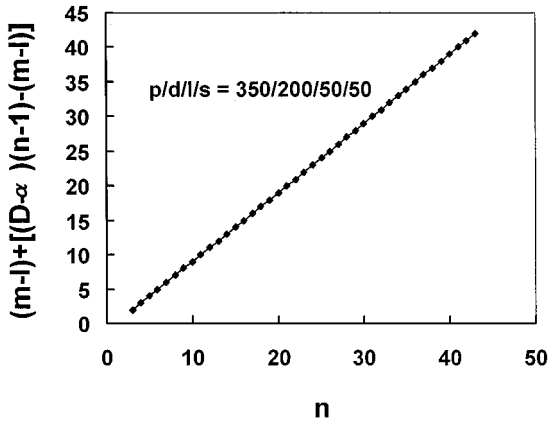

Fig. 7. Practical gain per the hybrid channel for pad pitch / pad diameter / line width / interline space = 350/200/50/50 as a function of n.

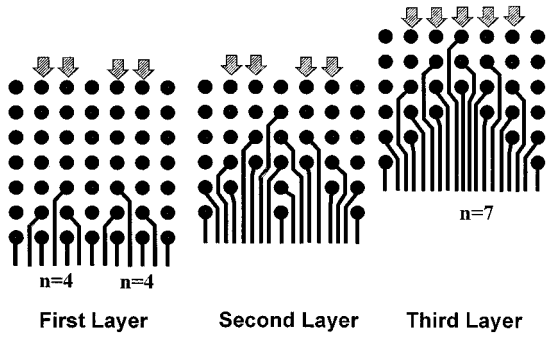

Fig. 8. An embodiment of how to arrange the hybrid channel with $n = 7$.

as shown in Fig. 4, include maximum number of the diagonal channels for a given odd n, and where number of the diagonal channels available is $n-1$. For an even n, the shape of the hybrid channels becomes an irregular quadrilateral with a number of the diagonal channels as $n-1$, as shown in Fig. 5.

Fig. 6 compares $m-l$ and $(D-\alpha)(n-1)$ depending on n for pad pitch of 240 μm, 350 μm and 350 μm with line width/space of 43 μm/43 μm, 50 μm/50 μm and 48 μm/48 μm, pad diameter of 110 μm, 200 μm and 110 μm, respectively. When $(D-\alpha)(n-1)-(m-l) \geq 0$, supplied lines will be adequate or excessive, so that the effective gain per hybrid channel, g, becomes $m-l$. On the contrary, the supplied lines will be deficient when $(D-\alpha)(n-1)-(m-l) < 0$, so that g becomes $(m-l)+[(D-\alpha)(n-1)-(m-l)]$. Fig. 7 estimates the gain per the hybrid channel taking account of this deficiency for pad pitch of 350 μm with line width/space of 50 μm/50 μm and pad diameter of 200 μm.

To achieve the efficiency of the hybrid channel for all routing layers, n and shape of the hybrid channel should be reproducible. This can be realized when $(n-1) \geq (m-l)$. Nevertheless, the shapes with a large n is generally difficult to maintain the reproducibility, caused by an increase of number

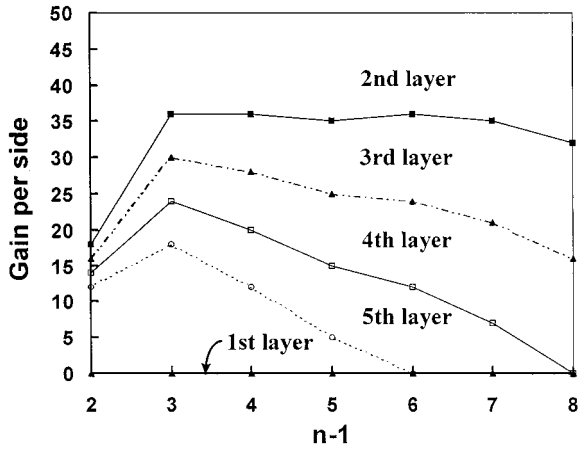

Fig. 9. Dependence of the gain per side on $(n-1)$ for the layers from 1st to 5th, with pad matrix $= 40 \times 40$, for pad pitch / pad diameter / line width / space $= 350/200/50/50$.

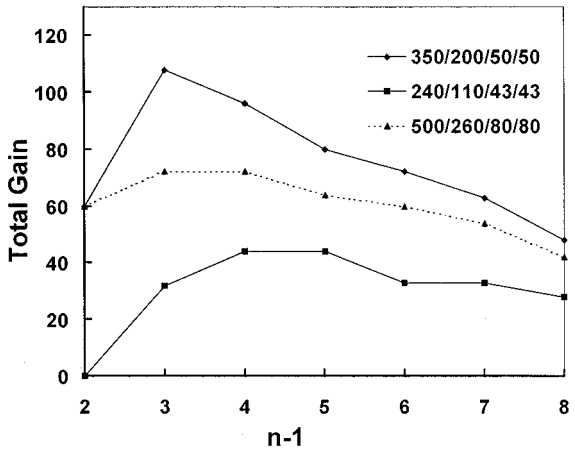

Fig. 10. Total gain summed from 1st to 5th layers depending on $(n-1)$, with pad matrix $= 40 \times 40$, for pad pitch / pad diameter / line width / space $= 350/200/50/50$, $240/110/43/43$, and 500/260/80/80.

of pads involved in the hybrid channel space. For $\alpha = 1$, when n is from 3 to 5, the reproducible channels can be arranged with two layers. Figs. 4, 5, 8 demonstrate how to arrange the hybrid channels for $n = 5, 4, 7$, respectively. With $n = 7$, three layers would be needed for the hybrid channel to be ready. For $n \geq 6$, the arrangement is initiated with combined triangles of a smaller n, as an example shown in Fig. 8.

B. Lines Per Side, Per Layer

With the triangle type hybrid channel, a gain per the channel can be increased as increase in n, as Fig. 7 suggests. On the other hand, number of the hybrid channels, Nh, per a side of the pad matrix decrease with increase of n, as

$$Nh = (Ns - 2(1+\alpha))/(n-1) \tag{4}$$

where Ns is number of the pads included on a side of the pad matrix and $(n-1)$ is a repetition unit of the hybrid channel for a maximum Nh. Thus a number of the lines additionally routable becomes the product of the gain per the channel and Nh. As the pad matrix size diminishes, Nh decrease by ranging from zero to two on the following layer. Fig. 9 estimates dependence of the gain per side on $(n-1)$ for the layers from first to fifth in the case of which Ns is 40 and pad pitch, line width, space, and pad diameter are respectively 350 μm, 50 μm, 50 μm, 200 μm (210 μm, 30 μm, 30 μm, 120 μm and 500 μm, 71 μm, 71 μm, 285 μm, likely used in flip chip and CSP, are also equivalent), and where the decrease in Nh is assumed constantly as two per layer (This is a special assumption to simplify the model. Practically, the decrease in Nh vary depending on n and the matrix size). Since there is no hybrid channel on the first layer, the gain is always zero on the first layer. Although a larger gain can be expected with a larger $(n-1)$ on the second layer, they notably decline on the following layers. Hence, the gain should be evaluated with a sum of all of the effective layers. Fig. 10 compares the total gain summed from first to fifth layers for the $(n-1)$ ranging from 2–8, in three dimensional cases that are respectively corresponding with flip chip to package/substrate $(p/d/l/s = 350/200/50/50$ and $240/110/43/43)$ and CSP to board $(p/d/l/s = 500/260/80/80)$. Maximum total gain is, in general, obtained when $(n-1)$ is from three to five, as shown in Fig. 10.

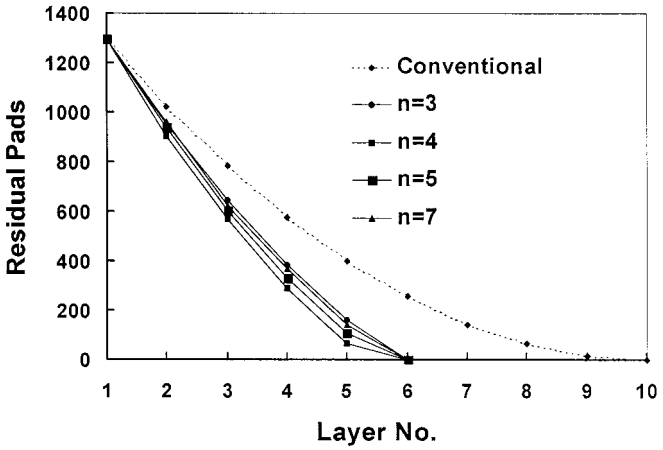

Fig. 11. The number of residual pads on the each layer routed with the preferential $(n = 3, 4, 5, 7)$ and the conventional procedures, with pad matrix $= 40 \times 40$, for pad pitch / pad diameter / line width / space $= 350/200/50/50$.

With the conventional routing out structure, lines per side on the first wiring layer is simply defined as $Ns + \alpha(Ns-1)$. For above mentioned preferential routing structure, the lines per side, ls, can accordingly be given as

$$ls = Ns + \alpha(Ns-1) + g \cdot Nh. \tag{5}$$

C. Number of the Layers Required

When outermost row and the next inner α row(s) are routed out on a wiring layer with the conventional procedure, the number of lines routable on the layer, Rt, is given by

$$Rt = \sum_{k=0}^{\alpha} 4\{Ns - 2[(\alpha+1)(L-1) - k] - 1\} \tag{6}$$

where L is a layer number. In practical cases, however, some lines additionally routable can be expected at the corner of the pad matrix. This corner effect arises from existing pads that are

TABLE I
COMPARISON IN REQUIRED FEATURE FOR ENTIRE ESCAPE ROUTING OF 40 × 40 PAD MATRIX WITHIN SEVEN LAYERS BETWEEN THE CONVENTIONAL AND THE PREFERENTIAL ROUTINGS

	Required feature size[μm]					lines routable	Layers for
	l	s	p	d	α	with n=5	escape routing
Preferential Routing	50	50	350	200	1	11	7
Conventional Routing	30	30	350	200	2	11	7

routable to two different directions perpendicular to one another. As the result, 2×4 additional pads can become routable for $\alpha = 1$, and $\alpha_2 \times 4$ pads can be expected for $\alpha = 2$ on the first layer. Although some empty channels exist on the outermost row, some critical channels, limiting the supply of lines, appear inside so that the additionally routable pads will be $2\alpha \times 4$ for $\alpha \geq 3$, in many cases. Since the matrix shape deforms from the square, an accurate estimation of the corner effect is difficult for the following layers. To avoid a complication, the corner effect has not been taken account in the model.

With the preferential routing, the number of routable lines on the layer, Rpt, is given by

$$Rpt = Rt + 4gNh. \tag{7}$$

Using this equation, Fig. 11 estimates the number of residual pads on the each layer routed with $n = 3, 4, 5, 7$ and the conventional procedure maintaining the matrix shaping square, in the case of which line width, interline space, pad diameter, pad pitch are, respectively, 50 μm, 50 μm, 200 μm, 350 μm (30 μm, 30 μm, 120 μm, 210 μm and 71 μm, 71 μm, 285 μm, 500 μm are also equivalent) and matrix size is 40×40 pads. With $n = 3$ through 7, the minimum number of layers required for 40×40 pads matrix to be wholly routed out can be six. The difference in Rpt from the practical number of layers needed is caused by the following two factors, except for the corner effect; First, the gain per the hybrid channel decreases to $(m - l) - 1$ on the second layer, caused by a deficiency of the supplied lines where the adjacent hybrid channels share a pad on their boundary. On the layers hereafter, the gain returns to $(m - l)$. Second, difference in Nh decrease also effects on Rt. In the preferential routing, the number of decreasing rows is larger than two that is the typical number for one line per channel structure. This is also a factor effective on Rt. Under these influences, the minimum number of layers required for 40×40 pads matrix to be wholly routed out becomes seven.

With the conventional two lines per channel structure requires the same number of routing layers as seven. The similar comparison can be done using the equations (1) and (2) between two lines per channel ($\alpha = 2$) structure and the hybrid channel with $\alpha = 1$. For instance, the line width and space should be thinned to 30 μm and 30 μm for $\alpha = 2$ from 50 μm and 50 μm for $\alpha = 1$ when the pad pitch and diameter are identical for both, and (1) gives 11 for $\alpha = 2$, while (2) also gives 11 for $\alpha = 1$, with these w, s and $n = 5$, as summarized in Table I. This suggests that the preferential routing structure with one line per channel rule is equivalent to conventional routing structure with two lines per channel rule.

IV. DISCUSSION

In general, logic LSIs have I/Os for power and ground ranging from 25 to 35% of the bump matrix. For instance, the ratio of signal, power and ground in typical ASICs can be roughly approximated as 4 : 1 : 1. These bumps for power and ground are typically located in center of the bump matrix, and are, respectively, connected to some separated power and ground layers of a substrate/package. Since these pads for both of power and ground can, respectively, be united systematically into one or two routes, number of rows for signal pads is a major factor that influences on the required number of routing layers.

The build up substrates are, in most cases, made with a symmetric structure, in which an identical number of build up layer are formed on both side of the core, to avoid a warp caused by imbalance in shrinkage during the manufacturing process. Minimum pitch among the though holes in usual PCB core is larger than the pitch among flip chip bumps, so that all signal pads in the matrix need to be routed out within the build up layers on the chip mounting side. To realize the symmetry, some electrically less-important layers tend to be added, usually as power or ground layers, on the opposite side. Therefore when one signal layer is eliminated, one of these insignificant layers can easily be omitted as well.

It is profitable to increase the number of pads routed out per layer even if a number of routing out layers required can not be decreased. Fig. 11 explains this advantage on the fifth layer. As the diminution rate is clearly different depending on n, an adequate area is provided for ground (or power) to coexist on a final routing layer of signal with the effective n. When the number of signal lines is sufficiently small, the layer can be regarded as a ground (or power) layer, and as the result, signal routing layers can be diminished. With this manner, we could practically reduce tow build up layers from 1296 lands-grid array package for ASIC, in which 800 signal pads in 3828 pads-matrix for the flip chip connection are included.

On the other hand, first layer is generally a special layer on which a solder resist layer and larger lands compared with that of the inner layer are formed for the flip chip bump connection. When $p - d < w + 2s$, the first layer is only usable for the outermost row to be routed, and the case is common to both the preferential and conventional methods.

Since the relative position of the pads would be kept among the layers, this method can be expected as effective, not only for via-on-via (filled via, via in pad or stacked via) structure, but also for Dog-bone structure (microvias on escaped pads) that are extensively used in the connection between flip chip to substrate or package, package to board, etc. Furthermore, a larger effect can be realized if the hybrid channels are formed

previously in the bump geometry on ICs or package bottom, though the typical given fully populated square grid matrix has been supposed in the present study.

As the influences of reducing the layer count by the preferential routing method, a consumption of the materials can be minimized. The materials here include not only direct matters, such as some metal and resin layers that are built up, metal plated, but intermediate matters, such as exposure mask, etching resist, as well. The decrease in the number of layers permits the manufacturing process to be shorten, so that the time to market is also minimized. This shortening will, in many cases, be greater than a few days, not a few hours. Additionally, some improvement might be expected in the production yield, especially for the build up substrate made though sequential process. Yield of a sequential type build up substrate is predicted by

$$\text{Cumulative yield} = (\text{Layer yield})^{(\text{Number of layers})}.$$

When the layer yield is 93%, the reduction of two layers improves approximately 10% of the cumulative yield.

To reduce the number of layers, decrease of line width and space is of course effective, as previously mentioned. However, some decrease in the layer yield should be taken into account whenever the manufacturing process is changed toward finer line and space. To realize two lines per channel, for example, line width and space should be decreased to 18 μm and 18 μm from 30 μm and 30 μm with 210 μm pad pitch and 120 μm pad diameter corresponding to one line per channel. This 40% reduction in the line width and space must influence on the processing yield. In contrast, the layer yield would not be deteriorated with the reduction of the layer count by the preferential routing. An improved cumulative yield is, accordingly, expected to be directly led by the decrease in the number of layer. All of the foregoing effects will result in a distinctly curtailed cost.

The reduction of the layer count, furthermore, contributes to the reliability. Generally, majority of the failures in the typical environmental tests, such as temperature cycling, thermal shock, autoclave, are observed at the microvia-junctions or their vicinities. Since the number of the microvias can be decreased with the reduction of the layer count, it is predicted to become more reliable.

V. Conclusion

The layer counts can be decreased for a given identical area array pad matrix depending on a routing design. The preferential routing method provides an effect, almost equivalent to that by increase in the number of lines per channel, on reducing the layer count. The effect is estimated from line-space-pad diameter-pitch relationship and the matrix size. Nothing change in the manufacturing process is required with this procedure, so that cost and TAT can be minimized. Reliability is also expected to be improved for interlayer connection. This method is applicable for both packages and board that are used for chip to package or to board and package to board interconnections.

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