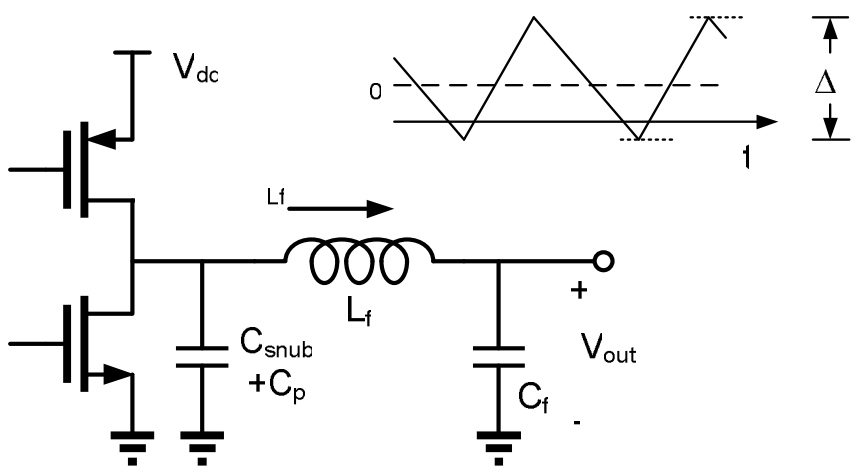
1. As mentioned last week, we want to find an optimized point between conduction loss(I^2R) and gate driving switching loss(CV^2f). With transistor size goes up, Ron will decrease but C_{gate} will increase. However, the simulation results only show limited improvement.



The reason is because we need to consider I_{rms} instead of I_{avg} to calculate the conduction loss. Noted that the L_fC_f product can be determined by the operation frequency (80MHz) and the required steady state output voltage ripple (2.5%). At first, after getting the L_fC_f product, I just chose the maximum available inductor (L_f) from the IBM 9sf library and then picked up the capacitance value accordingly. But for the schematic above, we know that in the steady state, V_{out} will almost be a constant value. So i_{Lf} will linearly increase or decrease according to the rectifier output voltage.

$$v = L\frac{di}{dt}, \qquad Vdd - vout = Vdd - D \cdot Vdd = L_f \cdot \frac{\Delta I}{Ts \cdot D}$$ (D: Duty ratio)

From above, ΔI is directly related to the inductor value. And the I_{rms} is then determined by both I_0 and ΔI, as showed in the figure below. If we want to have a optimized power efficiency, we need to consider the inductor size also.

2. I calculated all the circuit parameters from the stretch this week and tried to run simulation to verify it. But the ZVS loop not functioned as expected. The reason is that, as we want to decrease the conduction loss (I^2R), we choose larger transistor (reduce R) and larger inductor (reduce I_{rms}), in the cost of C_{gate}. But the parasitic capacitance C_p will also increase. And the sum of (C_p+C_{snub}) and the value of I_{rms} will impact the function of ZVS loop. With (C_p+C_{snub}) increase and I_{rms} decrease for the power efficiency, the High-to-low and Low-to-High transition will increase and cause the failure of ZVS loop. I run some simulation to confirm this and find out once we increase ΔI, the ZVS loop could come alive. But then, again, this will not generat the optimized power efficiency.