Weekly Report

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1. Find out the reason for the ZVS loop failure when decreasing the current ripple (ΔI) in order to increase the power efficiency. As mentioned before, to ensure the correct functionality, the inductor current (i_{Lf}) needs to be negative at leaset some time period to charge the capacitance ($C_{snub} + C_p$) to Vdd. The value of C_{snub} and ΔI can be calculated accordingly. But simulation results still show ZVS failure.

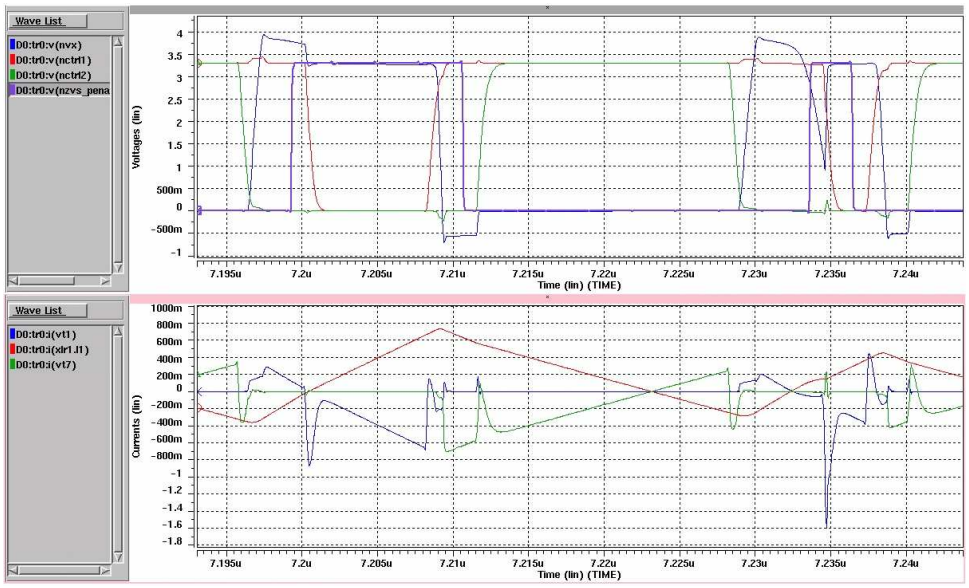

Figure 1: ZVS Loop Simulation Waveform

The detailed waveform can be found in Figure 1. The reason for the failure is beacuse the time delay of the comparator in ZVS loop. In Figure 1, the upper part is the voltage waveform and the lower part is the current waveform. Left hand side shows a successfully ZVS operation in one clock cycle and, on the opposite, is a failed ZVS operation.

The difference is the PMOS turn-on timing. If the PMOS's turn-on timing is delayed, which is after

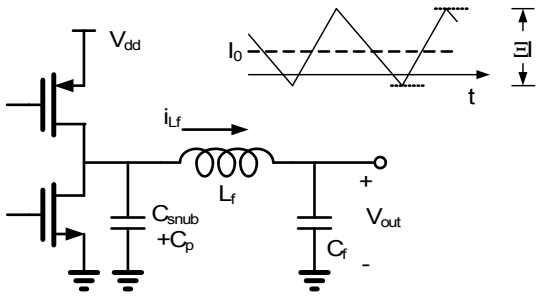

Figure 2: Simplified PWM circuit

inductor current changing it's direction, the voltage of rectifier output will drop. This cause the slope of the inductor current decreases and affects the overall transient behavior.

If I set the comparator threshold to a lower level, the ZVS loop could work despite of these transient malfunction. But the output voltage will be offseted due to the negative voltage of the overshoot. This overshoot cause the voltage comparator to response with a delay, with its negative value, will cause the average voltage goes down several mVolts.

2.