

Weekly Report

Wei Yao

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1. Check out the paper where over 80% efficiency is claimed. It turns out that the difference is due to the device/inductor model. Figure 1 and Figure 2 shows that, if we use the same formula but with the parameter provided in IBM 9sf process, the maximum efficiency will drop to around 70%. But the analysis provided in the paper is still valid, we still can optimize our design parameter according to these methods.

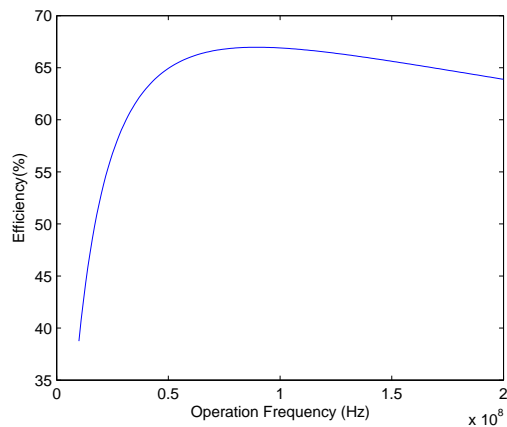


Figure 1: Operation Frequency vs Power Efficiency

2. Since the ZVS loop has some problems so that we can't clearly get the confirmed simulation results for each component's power consumption. Professor suggests to turn off the ZVS loop and check the power numbers. However, there will be a huge short circuit current if ZVS not working. To solve this, I use some skewed inverter to generate the delay for the control signal of PMOS and NMOS so that they will not turn-on at the same time. This is done manually and is only for analysis purpose. The skewed control signal can be seen in Figure 3. Simulation results is consistent with the analysis we made before.

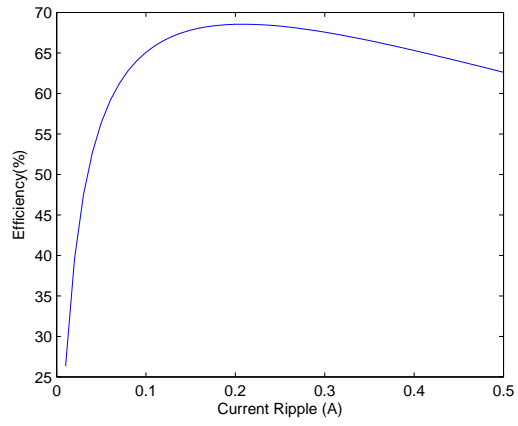


Figure 2: Current Ripple vs Power Efficiency

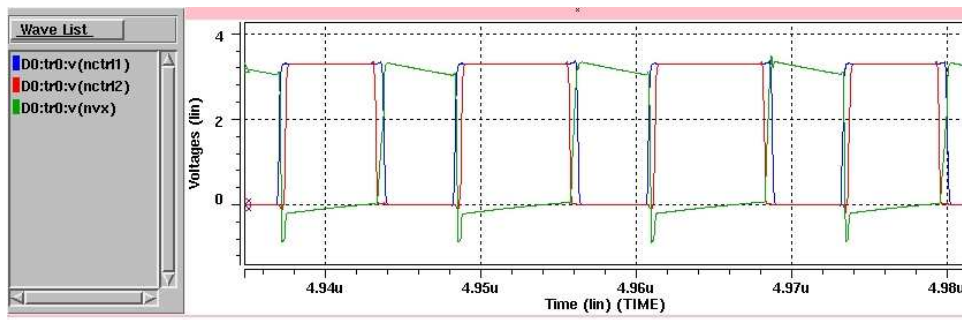


Figure 3: Simulation Results for the skewed control