Weekly Report

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1. Run the analysis to determine the max optimum efficiency available. As showed in Figure 1, the efficiency can only reach at around 65%. The bottleneck drops on the inductor loss. Figure 2 shows the same analysis, under same transistor parasitic setting, but with much better inductor available. (I use the same inductor setting as described in the paper.) The efficiency then goes up to 83%, similar to the paper.

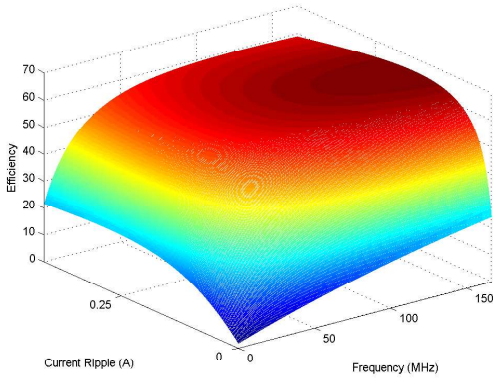

Figure 1: Optimum Power Efficiency vs frequency and Current Ripple

Here is the results and power breakdown of the analysis:

max efficiency: 66.950% inductor value: 10.60 nH

operation frequency: 180.58 MHz

current ripple: 199.52 mA

loading power: 240.000 mW

Inductor loss: 39.516 mW

PMOS switching loss: 25.819 mW

NMOS switching loss: 13.662 mW

PMOS conduction loss: 25.819 mW

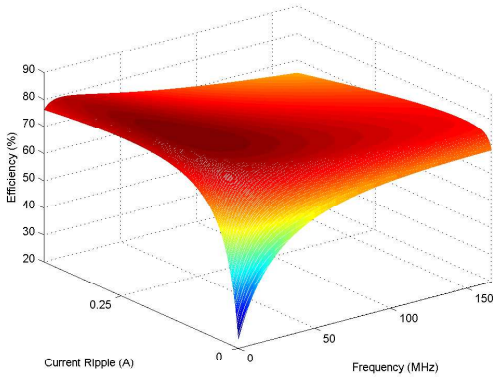

Figure 2: Optimum Power Efficiency vs frequency and Current Ripple with better inductor

NMOS conduction loss: 13.662 mW

2. Working on the ZVS loop. Mainly problem still occurred on the voltage comparator of the ZVS loop. Try some small fixing but still not function very well.