Model and Analysis for Combined Package and On-Chip Power Grid Simulation

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Abstract

We present new modeling and simulation techniques to improve the accuracy and efficiency of transient analysis of large power distribution grids. These include an accurate model for the inherent decoupling capacitance of non-switching devices, as well as a statistical switching current model for the switching devices. Moreover, three new simulation techniques are presented for problem size-reduction and speed-up. Results of application of these techniques on three PowerPC^{tm} microprocessors are also presented.

1. Introduction

Due to the increasing power consumption of microprocessors, power grid analysis has become a critical design task. An inadequate or poorly-designed power grid will result in excessive drops and fluctuations in the voltages supplied to devices, triggering performance degradation and signal integrity problems.

The voltage drop observed by a chip's devices is a combination of the voltage drop in the package and in the on-chip power grid. Package lead resistance is typically very low, hence the voltage drop across a package is predominantly due to package inductance, and is referred to as dI/dt *drop*. Conversely, the inductance of the on-chip power grid interconnect is small compared to its resistance. This is the dominant factor in on-chip voltage drop and is referred to as *IR-drop*.

Historically, much emphasis has been placed on analyzing the IR-drop of a power grid. Methods have been proposed for determining the worst case drop in a power grid[1][2][3], as well as for correcting *IR*-drop problems[4]. Since IR-drop analysis is often performed using DC analysis, the model of the power grid is fairly simple. It consists of resistances that model the power grid interconnect, and DC current sources that model the estimated peak current drain of circuit blocks or individual gates.

With the increasing power dissipation and operating frequency of the processors, the rate of current change (dI/dt) through the package and power distribution system has risen sharply causing significant concern for the dI/dt noise. Moreover, the package inductance combined with on-chip decoupling capacitance forms an RLC circuit that can resonate with certain instruction sequences and lead to noise build-up[5]. To ensure the robust operation of a processor, the impact of above effects on the power grid voltage must be analyzed. Such analysis, to be reliable, requires the power grid model to be complete with accurate models for the package and the on-chip power grid. A transient analysis of this combination can then be used to determine the voltage fluctuation at each of a chip's devices as well as the resonance behavior.

A combined package/on-chip power grid model requires that a number of circuit elements are extracted and modeled:
- RLC model of package leads, ball grid arrays, power planes
- RC model of on-chip power interconnect
- RC model of intrinsic decoupling capacitance of non-switching devices and n-well regions
- RC model of explicitly designed capacitance
- Model of AC currents of switching devices

Extensive research has been devoted to the extraction of accurate package models and power grid interconnect models, and a number of commercial tools are available for this purpose[6] [7]. However, much less work has focused on modeling the decoupling capacitance and the switching currents, which play a critical role in the transient and resonant behavior of the chip. In [8], simple models are presented for these parameters. However, they do not adequately represent the complex switching behavior on a chip, and can introduce significant error.

In this paper, we present a new model and extraction method for inherent device decoupling capacitance and device switching currents for the purpose of power grid analysis. We use a statistical model that can be applied both in the early stages of design and in pre-tape out, when the final layout is completed. The device decoupling capacitance methodology uses small-signal analysis of representative circuit blocks and is insensitive to errors in the switching activity estimation, which is a desirable property. The AC current model generates the desired total current profile using a statistical distribution of the switching current and the switching time of individual gates.

The simulation of a combined package/on-chip power grid suffers from several problems in terms of simulation efficiency. First, the modified nodal circuit formulation, which is typically used to solve for node voltages at each time step in a simulation, is no longer guaranteed to be positive definite when inductance is included in the power grid model. Hence, efficient matrix solution techniques for positive definite matrices, such as Cholesky factorization or the Conjugate Gradient methods, cannot be used. This results in a run-time increase of 2x or more. To overcome this problem, we present in this paper a method which separates inductance elements from RC elements and allows the use of efficient positive definite solution techniques for the RC portion. Since the RC elements greatly outnumber the inductances, this method has an efficiency similar to that of an IR-drop analysis, but without loss of accuracy.

Another efficiency issue arises from the fact that a combined package/on-chip power grid analysis requires the simultaneous analysis of both the Vdd and Gnd networks, since they are coupled to each other through mutual package inductance and on-chip decoupling capacitance. This doubles the circuit size as compared to a DC IR-drop analysis, in which the Vdd and Gnd grids are analyzed separately. Since the circuit model for a single power grid of a large microprocessor has few tens of millions of nodes, doubling the size of the model poses a serious problem. In this paper, we

propose a circuit transformation which exploits the near symmetry of most Vdd and Gnd power grids and allows a single power grid to be analyzed instead. This transformation is particularly effective for the analysis of power grids early in the design process, when the two grids are highly regular and symmetric.

Finally, combined package/on-chip power grid analysis requires the simulation of a large number of clock cycles before a steady-state behavior is obtained. This can lead to simulation times of multiple days for a large microprocessor. To reduce this run-time, we present a new method that uses a reduced circuit model to obtain an estimated steady-state circuit behavior. We then use this estimated steady-state as the starting point for the full power grid analysis to obtain quicker convergence. Using this method, the simulation time can be decreased by as much as 3 times.

The proposed power grid models and analysis techniques have been implemented in a power grid analysis tool called ElixIR, which has been used to analyze several generations of PowerPC[tm] processors. Results for 3 PowerPC[tm] processors are presented, and the effectiveness of the proposed methods is shown. The importance of improved decoupling capacitance and current models is also demonstrated.

The remainder of this paper is organized as follows: Section 2 presents the models and extraction methods for accurately representing a combined package/on-chip power distribution network. Section 3 discusses the simulation techniques for obtaining feasible run-times. Section 4 presents the results, and in Section 5 we draw our conclusions.

2. Power Grid Model

2.1 Model and Estimation of Decoupling Capacitor

While the explicit decoupling structures on a chip can be extracted using an extraction tool[6][7] and accurately modeled, the modeling and extraction of intrinsic decoupling capacitance of the devices and interconnect is complicated by the fact that the devices and interconnect play dual role - causing current to be drawn from the power rails when they switch, and providing decoupling when not switching. Traditionally[5][8], the amount of decoupling (non-switching) capacitance C_{decap} has been estimated from the average total power using the expression
$C_{decap} = \dfrac{P}{V^2 f}\dfrac{(1-SF)}{SF}$ where P is the average power, f is the switching frequency, V is the supply voltage, and SF is the average switching factor. Since (1 - SF) is much larger than SF, the error in this estimate is highly sensitive to any uncertainty in the estimated SF factor. For instance, when SF ranges from 0.1 to 0.3, as is the case in a typical design, the capacitance estimate varies by 285%. Since it is difficult to determine the exact SF for a large design, and also the SF varies widely in different parts of a chip, the above indirect estimation of total capacitance (switching + non-switching) from average power is highly error-prone. We overcome this difficulty by a direct estimation using SPICE simulations of several representative circuit blocks.

The procedure is shown in Figure 1. A representative circuit block is put in an arbitrary non-switching state by applying a DC operating voltage (V_{dc}) to the power terminals and 0's and 1's randomly to input signals. Then a small AC (sinusoidal) perturbation,

typically 5-15% of V_{dc} representing the supply noise, is applied to the power rails to determine the decoupling action of the circuit in that state. Figure 1(a) shows the simulation setup. Figure 1(b) depicts the equivalent RC circuit of the underlying decoupling circuit. Figure 1(c) shows the voltage and current at the power terminals in phasor notation. Since the device capacitances are voltage-dependent in the SPICE model, the resultant I_{ac} is not exactly sinusoidal, but the deviation is unnoticeably small due to the small change in voltages. The R_{eff} and C_{eff} elements are then calculated as shown in Figure 1. For this method, a small number of representative circuit blocks are chosen and are simulated along with all the interconnect parasitics. To account for the loss in decoupling action due to the switching of some devices, the C_{eff} as determined above is scaled down by the factor (1 - SF). This procedure is less sensitive to any error in the estimation of SF since SF is typically much smaller than 1. For a variation from 0.1 to 0.3 in SF, the estimated capacitance will vary by only 28%.
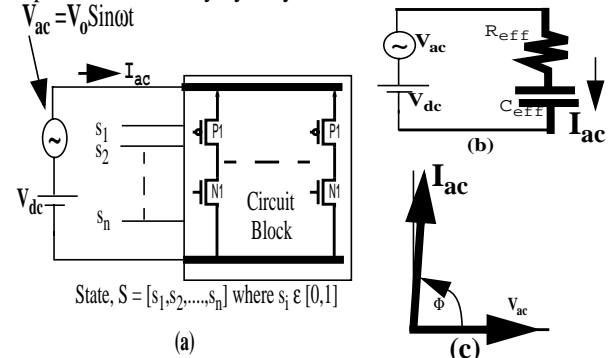
$$C_{eff} = (1/2\pi f)(V_{ac}/I_{ac}) \sin \Phi \qquad R_{eff} = (V_{ac}/I_{ac}) \cos \Phi$$

Figure 1. Intrinsic decoupling of devices and interconnect

Although the effective R and C are both frequency and voltage dependent, the simulations recorded relatively constant values in the frequency range of 0.2x - 2x the clock frequency and for a voltage fluctuation of 5 to 15% of Vdd. Moreover, they showed less than 3% variation across all input states for a circuit block of 240 transistors with 10 primary inputs. Thus, it would suffice to simulate the circuit in very few random states and take their average.

The C_{eff} and R_{eff} values determined for a block represent the combined decoupling action of the device capacitances and the extracted parasitic capacitances of the interconnects and can be translated to other circuit blocks based on the relative size (sum of transistor widths) of the blocks. An added advantage of this method is that decoupling capacitance can be individually modeled for blocks with different switching characteristics or topologies, allowing local variations in parts of a chip.

The intrinsic N-well capacitance is also modeled as a series RC whose time constant and capacitance per unit well area are characterized using a process simulator. The intrinsic as well as the explicit decoupling capacitances are distributed either according to the layout or, when a layout is not available (as during the early design stage), uniformly across the power rails.

2.2 Current Model

For a DC based IR-drop analysis, an estimated peak DC current is often used when the circuit design is still incomplete. In [8],

this simple DC peak current model is extended to an AC peak current model. Based on the estimated average chip current and an average/peak current factor, the current profile for a single clock cycle is constructed as shown in Figure 2(a). This current profile is then evenly distributed across all power grid connections by dividing the chip-level current by the number of power grid connections at each time point in the clock cycle. This method results in a low, wide current profile for each gate, and all gate currents are perfectly synchronized. In an actual circuit, however, each gate produces a much narrower and taller current pulse when switched, as shown in Figure 2(b). For a 500MHz design, a typical gate produces a current pulse 50ps wide, only a fraction of the 2ns pulse width that will be generated in the above approach. Also, gate currents are not synchronized, and switch at various times during the clock cycle. Decoupling capacitance is much more effective in supplying the needed charge for many short, asynchronous current spikes than for a set of slow, synchronized current pulses. Thus, this simplified current model can produce a significant error in power grid analysis.
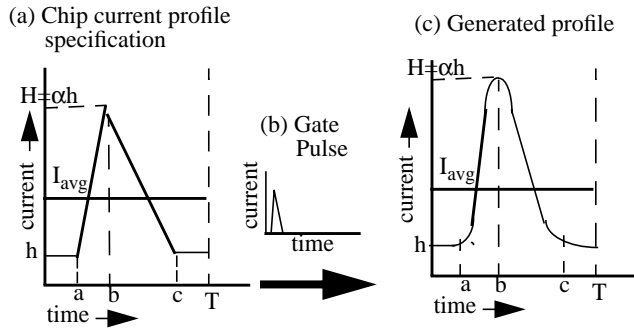

Figure 2. Generation of Mock Current Profile

An accurate model can be obtained by a fast transistor level simulation of the circuit blocks using chip-level vectors, monitoring the individual gate currents. Each gate can then be modeled by a current source matching its observed profile. However, this procedure is prohibitively expensive for very large processors. More importantly, most power grid design is performed before the circuit design is completed and transistor level simulation can be performed. Once all circuit designs are completed, only limited, small modifications can be made to the power grid. Hence, there is a critical need for a good early current model - a model that not only matches the total current profile at the chip-level, but matches also the gate-level current profiles and mimics their random switching behavior.

We propose therefore an enhanced current model in which each gate is assigned a short, sharp current spike as shown in Figure 2(b), as determined from SPICE simulations of typical gates. The user specifies the average current I_{avg}, the peak-to-base current ratio α, and the parameters a, b, and c, from which the chip-level current profile is constructed as shown in Figure 2(a). The switching times of individual gates are then assigned randomly such that they have a probability density function same as the specified current profile. Figure 2(c) shows the profile of total current thus generated. This model can be easily extended to obtain block-specific average current and peak-to-base current ratios.

Most commonly used random number generators have uniform distributions. The required non-uniform distribution of gate switching times can be generated through a uniformly distributed random number generator using a suitable transformation $f(x)$. Referring to Figure 3, if two random variables t and x with probability distributions $p(x)$ and $q(t)$ are related with a function $t=f(x)$ then their probability distributions obey the following differential equation [12]:

$$q(t) = p(x)\frac{dx}{dt} = p(f^{-1}(t))\frac{df^{-1}(t)}{dt}$$

Solving this equation for each continuity interval of the required function(0-a, a-b, b-c, c-1) and taking into account probability distribution normalization, one can compute the coordinates u, v, and w and obtain closed expressions for the transformation from x to t in the intervals 0-u, u-v, v-w, and w-1. The expressions are omitted here for brevity. Note that the generated profile matches well the specified profile when the gate pulses are sharper.
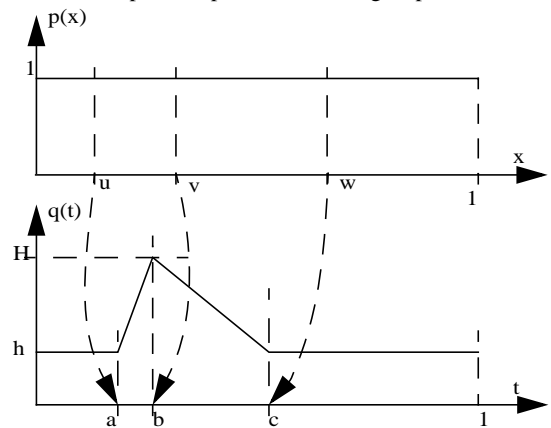

Figure 3. Modeling Random Gate Switching

Since the ratio α represents the peak-to-base current ratio as drawn by devices, it is not directly measurable. To determine α, we first determine the ratio of the peak-to-base current through the C4 pads or bondwires (referred to as β) using the techniques presented in [9]. We then adjust the value of α in the simulation until the value of β obtained matches the measured β. Note that β is much smaller than α due to the charge supplied by on-chip decoupling capacitance. For a typical PowerPC[tm] design, β is approximately 1.2, which results in an α of 5.0.

Using the above current model, multiple current profiles can be constructed, each representing an instruction with a different power level. For each instruction, the total average current and α are determined. The current profiles for different instructions are then combined into a sequence of multiple instructions to simulate the power grid behavior during a transition from a low to high power instruction and vice versa.

2.3 Package Inductance and Grid Resistance Models

The parasitic inductances of the power grid in a package must be extracted and modeled to study their effect on the power grid voltage and resonance behavior. The major sources of parasitic inductances in the package are the power planes, ball arrays/bond wires, and package vias. A number of inductance extraction tools and techniques[10][11] are available to extract the model of the package power network. Defining ports for the package network at each supply and ground input to the package and at connection

points to the die, the extracted model can then be reduced to a compact n-port model. The n-port model is a completely dense matrix which represents the self and mutual inductances between port connections.

The parasitic resistances of the on-chip power and ground grid are either extracted from the layout with a commercial extraction tool or, in early phases, are determined directly from wire sizes using sheet resistance. The n-port model of the package and the RC elements of the on-chip power model are then combined with the extracted decoupling capacitance models and current source models. Finally, the combined power grid network is simulated using the techniques described in Section 3.1.

2.4 Model Simplifications

Because a chip's mutual package inductances and on-chip decoupling capacitances couple its power and ground grids, the two grids influence each other and must be simulated simultaneously as one combined power network. Since power grids are already extremely large for microprocessors, doubling the size of the network to be simulated is undesirable. By taking advantage of the fact that power and ground grids are often symmetric (especially in early analysis), we can reduce the combined Vdd/Gnd power grid network back down to a single power grid network.
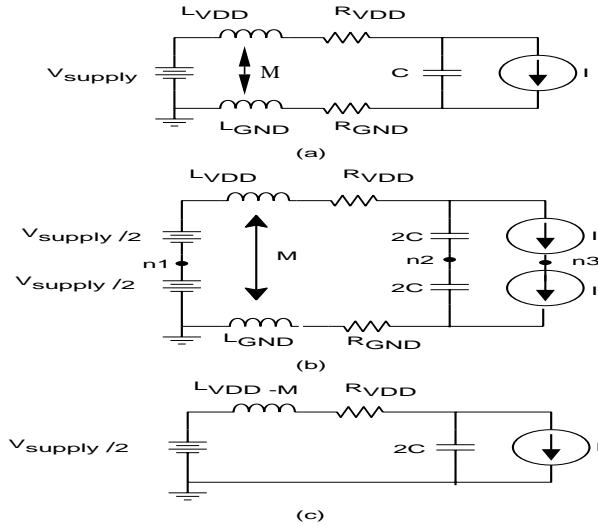

Figure 4. Transformation of a combined Vdd/Gnd grid into an individual grid.

To illustrate this circuit transformation, Figure 4(a) shows an abstract representation of the power grid network. The inductances L_{vdd}, L_{gnd}, and M represent the self and mutual inductances of the package. The resistances R_{vdd} and R_{gnd} represent the resistance network of the Vdd and Gnd grids, respectively, and the current source I and capacitance C represent the device switching currents and decoupling capacitance. We first transform the circuit into the form in Figure 4(b) by splitting the decoupling capacitance, current source, and voltage source into an equivalent structure with two series-connected components. Since the current in L_{vdd} will be equal and opposite to the current in L_{gnd}, we also subtract the mutual inductances M from the self inductance L_{vdd} and L_{gnd}, as shown. This transformation does not change the behavior of the circuit, and only introduces three new nodes, n1, n2, and n3. If the

power and ground grids are symmetric ($L_{vdd} = L_{gnd}$ and $R_{vdd} = R_{gnd}$), we can connect the three nodes n1, n2, and n3 to ground, decoupling the power grid network into two independent networks. We can then simulate one of the two power grids as shown in Figure 4(c) and infer the voltages in the other.

3. Circuit Solution Techniques

3.1 Efficient Transient Simulation with Inductance

Certain computational advantages are lost when an RC network model is expanded to include a package model. Note that an RC model produces a symmetric positive definite left-hand side (LHS) matrix in a modified nodal analysis of the system Ax = b. These properties of A make it possible to solve the system very efficiently using either Cholesky factorization or the incomplete Cholesky pre-conditioned Conjugate Gradient approach. When the package model is included in the analysis, however, the self and mutual inductors of the package now require the currents through the inductors to be declared as variables, and the resulting LHS matrix is not guaranteed to be positive definite. One could use general solution techniques, such as LU-decomposition, to solve the RLC model, but the large size of the network makes such techniques difficult. We overcome this problem using the following approach.

The network is partitioned at the interface between the package network and the power grid network. The power grid network (consisting only of R's, C's, and the current sources) is then reduced to equivalent admittance and currents at the interface points, and the package network is solved including the reduced representation of the power grid. This approach works well, since the reduction of the power grid network involves solving a symmetric positive definite system. The package network with the reduced power grid model is much smaller and can be solved using a general solution technique, such as LU-decomposition.

Suppose Ax = b is the system representing the combined network, and

$$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{12}^T & A_{22} \end{bmatrix} \qquad x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \qquad b = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix}$$

where x1 is the vector of voltages at the nodes in the power grid and *x2* is the vector of voltages and inductor currents in the package network.

The above system is then solved in two steps as follows:

$$x_2 = (A_{22} - A_{12}^T A_{11}^{-1} A_{12})^{-1} (b_2 - A_{12}^T (A_{11}^{-1} b_1))$$

$$x_1 = A_{11}^{-1}(A_{22} - A_{12}x_2)$$

The pre-multiplications with the inverse of A11 are performed indirectly using Cholesky factors, or with the Conjugate Gradient method for greater efficiency. The model reduction requires solving the power network *p+1* times, where p is the number of interface nodes. If a constant time step is used, however, the matrix A11 will not change between time steps. Hence, the matrix A11 can be factored once, and those factors can be reused throughout the simulation. The number of ports (C4 pads or bondwire pads) is typically between 100 and 300 for a large microprocessor, a small

number when compared to the number of time points in the entire simulation, which can easily exceed 2000. Thus, the initial factorization time does not contribute significantly to the run-time of the overall simulation.

3.2 Decreasing Simulation Time to Reach Steady-State

When studying the effects of transience and resonance during transitions between two different power levels, say from sleep state to a high power state, a prolonged simulation in the first(sleep) state is necessary to attain the steady state at that power level before applying the transition to the next(high) power state. Since the initial states of the inductances and capacitances are determined by a DC solution and the damping factor of the grid is very low, it takes several cycles for the grid to settle to a steady state. This is a serious problem for power grid analysis since simulation of every additional cycle adds considerable run-time overhead. By obtaining a better estimate of the steady state values for the inductor currents and the capacitor voltages at the start of the simulation, we can reduce the time to reach steady-state. We estimate the steady state conditions of the circuit by building a small representative model of the full grid and then simulating this simple model in SPICE until a steady state is obtained.
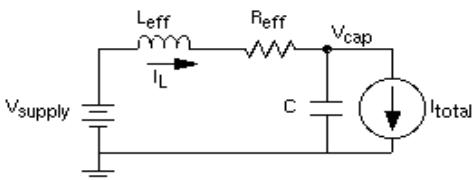

Figure 5. Simplified circuit for estimating steady state behavior.

Figure 5 shows the elements of the representative model. L_{eff} is the total effective package inductance, calculated as the parallel inductance of the self inductances of all pads. R_{eff} is the effective resistance from the pad to the device located at the point of worst voltage drop in a DC simulation. It is calculated by dividing the worst DC voltage drop by the total chip current. Capacitance C is the sum of all decoupling capacitances in the grid, and current I is the sum of all current sources in the grid. The representative circuit is then simulated using SPICE, and the steady state current I_L and voltage V_{cap} are recorded for a reference time point in a cycle. The inductor currents and capacitor voltages obtained in a DC solution of the full network are then scaled such that the total inductor current is equal to I_L and the worst capacitor voltage is equal to V_{cap}. With these values as initial conditions, a transient analysis is performed. This method requires only one DC solution of the full network and the transient simulation of a very small model circuit. The overhead incurred is insignificant when compared to the improvement in run-time. Actual results are provided in the next section.

4. Results

The methods discussed above have been implemented and exercised on a number of industrial microprocessor designs. Figure 6 shows a transient simulation for a 200MHz PowerPC[tm] processor. The simulation consists of 40 low power instruction cycles with an average current of 0.4A, followed by 40 high power instruction

cycles with an average current of 4A. Figure 6 shows the voltage at the device with the worst drop. The blow up in Figure 6 shows the total power grid current during the low power to high power transition. In steady-state under the high-power instructions, the worst voltage drop is 110mV and the maximum overshoot is 31mV. The worst drop and overshoot, however, occur during the transition from the low power instruction to the high power instruction, with a maximum drop of 183mV and a maximum overshoot of 100mV. The wide voltage fluctuation at the start of the simulation is simply an artifact of the transition from the initial DC solution and should be ignored.
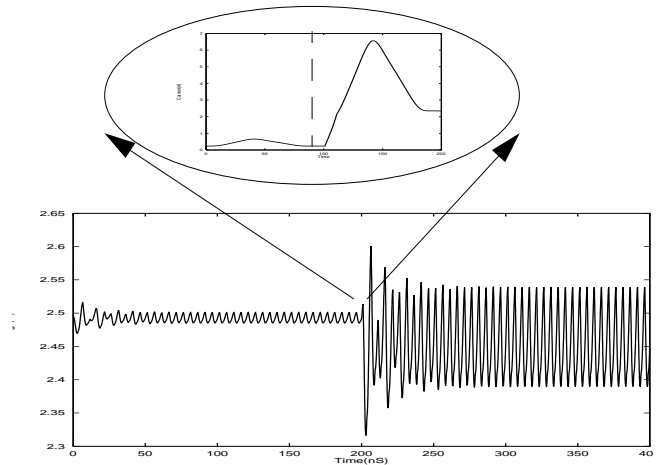

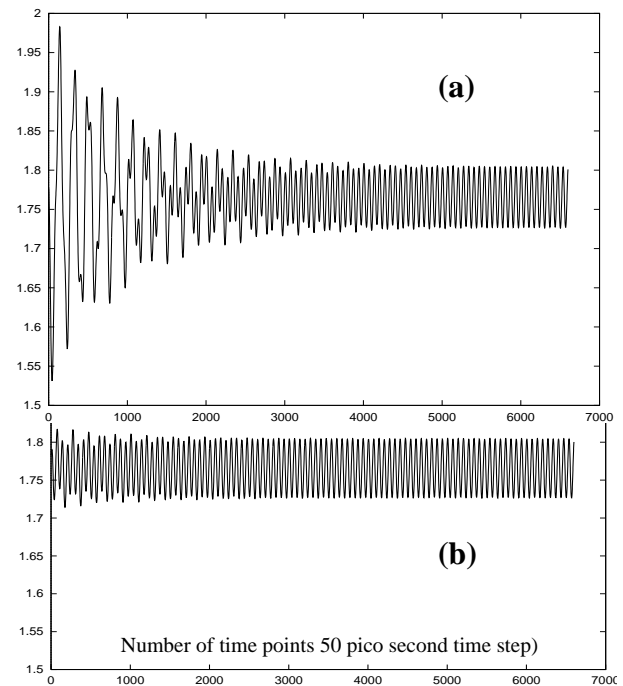Figure 6. Transient simulation of a 200MHz PowerPC[tm] processor.

Figure 7. Transient analysis starting from (a) DC solution and (b) estimated steady state solution

The combined package/on-chip analysis resulted in higher voltage drop (183mV) than a corresponding DC analysis with only on-chip resistance (101mV). Also, the voltage distribution was observed to be significantly different, indicating that reliable power grid analysis must be performed with a combined package/on-chip model. DC analysis is still useful to detect gross design errors and partial disconnects, but a combined analysis is necessary to achieve higher accuracy.

To demonstrate the reduction in simulation time using the estimated steady-state behavior, Figure 7 shows a transient analysis of a 300Mhz PowerPC[tm] processor. Figure 7(a) shows the transient simulation with DC initialization, and Figure 7(b) shows the same simulation with the initialization method presented in Section 3.2. Initializing the network closer to steady-state using the estimate is seen to bring the network to steady state in approximately one third the number of clock cycles it takes from a DC initialization. In steady state, the current and worst voltage at the start of a clock cycle were 4.74A and 1.785V respectively. The DC initialization however set the current at 2.8A and the worst voltage at 1.77V, thus leaving a deviation of 62% in current from the steady state. But the proposed method estimates these values as 4.713A with a worst voltage of 1.782V, only a 6.5% deviation in current. As a result, our method reduced the time to converge from 48 hours to 16 hours.
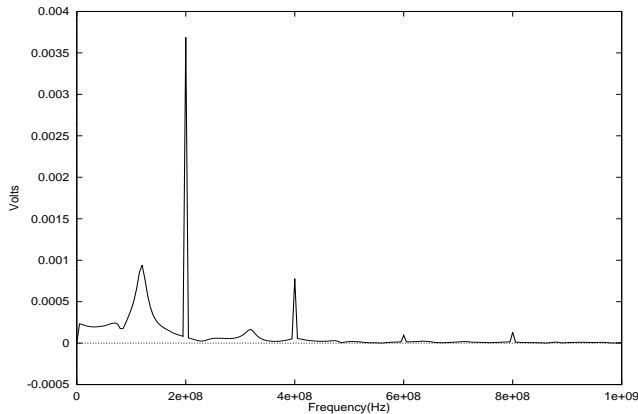

Figure 8. FFT of transient voltage of a 200MHz PowerPC[tm]

Finally, Figure 8 shows the FFT of the transient voltage of a 200MHz PowerPC[tm] processor. The total decoupling capacitance(C) and the effective lumped package inductance(L) were 30nF and 0.08nH respectively. The first peak of the frequency spectrum was observed near 120 MHz which is close to the resonance frequency of 102MHz estimated by the expression

$$f_r = 1/(2\pi\sqrt{LC})$$

. Table 1 shows the resonance and operating frequencies (columns 2 and 3) of 3 PowerPC[tm] processors, along with their worst voltage drops in DC analysis (column 4) and their maximum undershoot (column 5) and overshoot (column 6) during transient analysis. The marked difference in the DC and transient performances of the power grid stresses the importance of the transient analysis with an accurate model of the power grid as proposed in the foregoing sections. The results also show that the power supply noise is increasing and the resonance frequency is decreasing as the speed and size of the processors increase.

5. Conclusions

We presented new techniques for accurately modeling the decoupling capacitance and switching currents of microprocessors for power grid simulation. We also demonstrated three techniques for efficient transient simulation of a combined package/on-chip power network. We showed how these techniques are essential in making power grid simulation for large processors practical. The presented methods have been implemented in an industrial power grid analysis tool called ElixIR, and results demonstrating their effectiveness were shown for three PowerPC[tm] processors.

Table 1: Resonance and transient voltages

Chip	Frequency(MHz)		Worst drop(mV)		Max. over-shoot (mV)
	Operat-ing	Reso-nance	DC	Tran-sient	
μP1	200	120	101	183	100
μP2	300	115	67	246	159
μP3	500	90	150	345	199

PowerPC[tm] is the registered trademark of the International Business Machines Corporation.

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