Investigation of Candidate VRM Topologies for Future Microprocessors

Xunwei Zhou, *Member, IEEE*, Pit-Leong Wong, *Student Member, IEEE*, Peng Xu, Fred C. Lee, *Fellow, IEEE*, and Alex Q. Huang, *Senior Member, IEEE*

***Abstract*—By reducing the power supply voltage, faster, lower power consumption, and high integration density data processing systems can be achieved. The current generation high-speed complementary metal-oxide-semiconductor (CMOS) processors (e.g., Alpha, Pentium, Power PC) are operating at above 300 MHz with 2.5 to 3.3 V output range. Future processors will be designed in the 1.1–1.8 V range, to further enhance their speed-power performance. These new generations microprocessors will present very dynamic loads with high current slew rates during transient. As a result, they will require a special power supply, voltage regulator module (VRM), to provide well-regulated voltage. The VRMs should have high power densities, high efficiencies, and good transient performance. In this paper, the critical technical issues to achieve this target for future generation microprocessors are addressed. And a VRM candidate topology, interleaved quasisquare-wave (QSW), is proposed. The design, simulation, and experimental results are presented.**

***Index Terms*—Interleaved, microprocessor, QSW, voltage regulator module.**

I. Introduction

AN EVOLUTION in microprocessor technology poses new challenges for supplying power to these devices. The evolution began when the high-performance Pentium processor was driven by a nonstandard, less-than 5 V power supply, instead of drawing its power from the 5-V plane on the system board [1].

In order to meet faster and more efficient data processing demands, modern microprocessors are being designed with lower voltage implementations. The processor supply voltage in future generation processors will decrease from 3.3 V to 1.1 V $\sim$ 1.8 V. Meanwhile, because more devices are packed on a single processor chip and the processors operates at higher operating frequencies, microprocessors need aggressive power management. Future generation processors' current draw will increase from 13 A to 30 A $\sim$ 50 A [2]. These currents in turn require special power supplies, voltage regulator modules (VRMs), to provide lower voltages with higher current capability for microprocessors.

As the speed of the processor increases, they increase the dynamic loading of the VRM. These slew rates represent a severe problem for large load changes that are usually encountered in systems with power management when the systems transition from the sleep mode to the active mode and vice versa. In this case, the parasitic impedance of the power supply connection to the load and the parasitic elements of capacitors have a dramatic effect on VRM voltage [2]. Future microprocessors are expected to exhibit higher current slew and larger current draw. Moreover, the total voltage tolerance will become much tighter. Currently, the voltage tolerance is 5% (for 3.3 V VRM output, the voltage deviation can be $\pm$ 165 mV). In the future, the total voltage tolerance will be 2% (for 1.1 V VRM output, the voltage deviation can only be $\pm$ 33 mV). All these requirements pose serious design challenges. Table I shows the specifications for current and future VRMs.

TABLE I
SPECIFICATIONS FOR CURRENT AND FUTURE VRM

	Current	Future
Output Voltage:	2.1~3.5V	1~2V
Load Current:	0.3~13A	1~30A
Output Voltage Tolerance:	± 5%	± 2%
Current Slew at decoulping Capacitors	1A/nS *	5A/ns

*: Current Slew rate at today's VRM output is 30A/uS

Most of today's VRMs use conventional buck or synchronous rectifier buck topology. In future microprocessor application, the limitations of these topologies are very clear. In order to maintain voltage regulation of future requirements during the transient, more output filter capacitors and decoupling capacitors will be needed [3]. However, the space of the VRM and motherboard are very limited. Increasing capacitors is an impractical approach. To meet future specifications, novel VRM topologies are required. On the other hand, an advanced integration approach is required to minimize the effect of connection and component parasitics.

To achieve this target, a number of critical issues have to be addressed. For example, advanced power device and control technologies are needed for high efficiency and high frequency operation. Today's vertical power device technology can not provide acceptable conversion efficiency at multimegahertz due to its high conduction and switching and gate drive losses. In this paper, advanced VRM topologies for fast transient response

Manuscript received March 16, 1998; revised May 18, 2000. This work was supported by Intel, Texas Instruments, National Semiconductors, Inc., SGS Thomson, Delta Electronics, Inc., ERC Shared Facilities, and the National Science Foundation under Award EEC-9731677. Recommended by Associate Editor K. Smedley.

X Zhou is with Volterra Company, Fremont, CA 94538 USA.

P.-L. Wong, P. Xu, F. C. Lee, and A. Q. Huang are with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA.

Publisher Item Identifier S 0885-8993(00)09795-7.

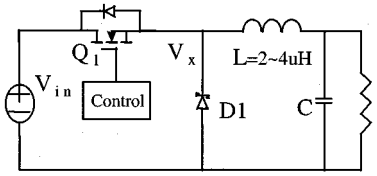

Fig. 1. Conventional buck converter.

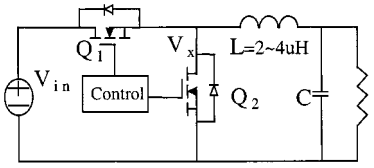

Fig. 2. Synchronous rectifier buck.

and low ripple voltage together with advanced packaging technologies for improving power density are among these important issues to be addressed. In addition, the limitations of today's technologies, VRM topologies and power device, are analyzed.

II. Limitations of Today's Technologies

A. Limitation of Present VRM Topologies: Transient Limitation

Most of today's VRMs use conventional buck or synchronous rectifier buck topology. Fig. 1 shows the conventional buck circuit, which is the most cost-effective approach. Usually, Schottky diodes are used as a rectifier. The top MOSFET transfers energy from the input and the bottom rectifier conducts the inductor current. The control regulates the output voltage by modulating the conduction interval of the top MOSFET. Fig. 2 shows the synchronous rectifier buck circuit. This topology increases the efficiency by replacing the rectifier with a low Rds(on) MOSFET. The synchronous switch is controlled by the complementary signal of the top switch's gate signal. The synchronous rectifier buck always operates in continuous current mode. In order to reduce output ripple, conventional VRMs inductor design is according to

$$L \geq \frac{10 \times (Vin - Vo) \times D}{Io \times fs} \tag{1}$$

where

D duty cycle;
Vin input voltage;
Vo output voltage;
Io full load current;
Fs switching frequency.

Today's VRMs usually use large output filter inductance, 2∼4 μH.

The simulation circuit for the VRM and today's processor is shown in Fig. 3. The power stage is a traditional synchronous buck converter with 5 V input and 3.1 V output. The load is simplified as a current source with exponential transition from 1 A to 13 A with the highest slew rate being 1.6 A/ns (the slew rate is 1A/ns at decoupling capacitor and 30 A/μs at VRM output). The packaging capacitor is the parasitic capacitor inside the microprocessor package. There are a lot of decoupling capacitors

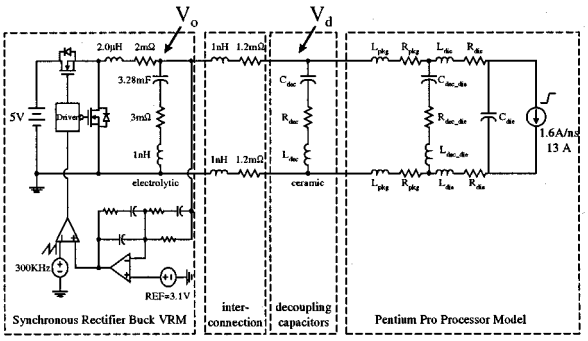

Fig. 3. Pentium Pro processor simulation model.

near and around the microprocessors to reduce noise and maintain voltage regulation. Bulk capacitors are VRM output capacitors. Because of the low voltage, high current, and fast load transient characteristics, parasitic parameters play very important roles in both steady state and transience. In transient analysis, a capacitor can no longer be considered an ideal capacitor. It is actually a capacitor with equivalent-series-resistor (ESR) and equivalent-series-inductor (ESL). The interconnections between the VRM and motherboard, motherboard and processor, and so on cannot be ignored either. In this case, all these parasitics have significant effect on VRM transient voltage. These parasitic parameters form resonant loops in the circuit. The resonance corresponds to the transient voltage drop spikes. In steady state, the interconnection resistance also causes regulation error due to the high current that flows through it at full load. The circuit parasitic parameters such as ESR and ESL of the capacitors and link impedance are also shown in Fig. 3. The transient voltage waveforms at VRM output Vo and decoupling capacitors Vd are shown in Fig. 4. For today's requirement, the transient voltage deviation limit at VRM output is 5% and 7% at the decoupling capacitors. The waveforms show that they both meet their requirements.

Assume that a future processor still has the same structure as shown in Fig. 3 except that the transient load magnitude is changed to 0.1∼30 A with a higher slew rate of 8 A/ns. The steady state output of the VRM also is changed to a lower voltage of 1.5 V. The transient voltage waveforms of Vo and Vd are shown in Fig. 5. The transient voltage deviation limit at Vo and Vd will be 2% and 100 mV, respectively, as also shown in Fig. 5. Neither of the waveforms meets the requirement.

A closer look at the transient voltage waveforms reveals that the VRM output transient voltage drop contains three spikes. They are marked as first, second, and third spike, respectively, as shown in Fig. 4 and Fig. 5. These three spikes are decided by the R-L-C resonant loops shown in Fig. 6. The first high frequency spike is dominated by loop 1, which combines the parasitic of the packaging capacitors and decoupling capacitors and the interconnection between them. The second spike is controlled by loop 2, which combines the parasitic of the decoupling capacitors and VRM bulk capacitors and the interconnection between them. The third spike is decided by loop 3, which is combines the parasitic of the VRM output filter inductor and bulk capacitors.

However, for different loops, because of the different characteristics of different capacitors, the effects of each parameter

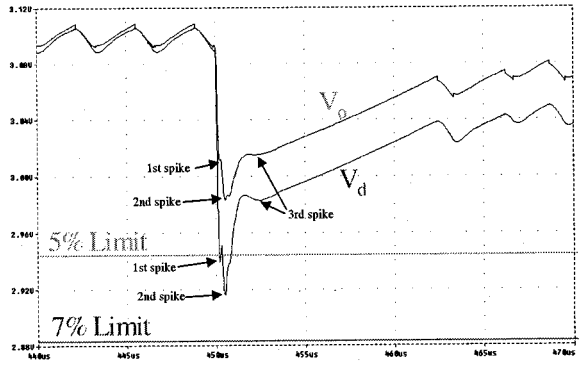

Fig. 4. Transient-voltage waveforms at VRM output and decoupling capacitor for present processor model.

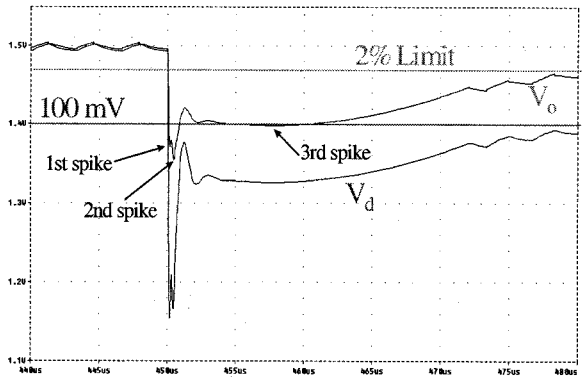

Fig. 5. Transient-voltage waveforms at VRM output and decoupling capacitor for future processor model.

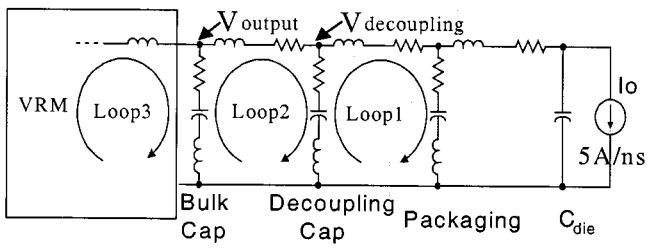

Fig. 6. Processor model can be considered as three resonant loops with different resonant frequencies.

are quite different. For example, the die capacitor, C_{die}, has very small ESR and ESL that can be ignored. The voltage spike on it will not have the proportional and differential part. For the other capacitors in the model, the ESR and ESL cannot be ignored, as shown in Fig. 3. Fig. 7 shows the practical capacitor model. When a capacitor provides a current, i, the total voltage drop on it can be divided into three parts:

1) PROPORTIONAL PART is due to the current flow through the ESR of the capacitor

$$\Delta V_P = ESR \cdot i. \tag{2}$$

2) INTEGRAL PART is due to the loss of charge in the capacitor. Charge is equal to the integral of current. The part

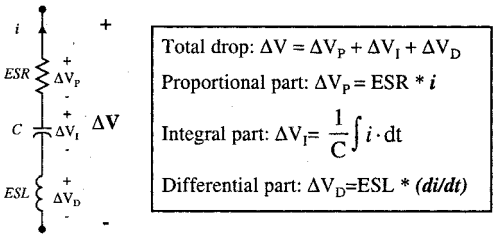

Fig. 7. Voltage drop of a capacitor can be divided into three parts: proportional, integral, and differential.

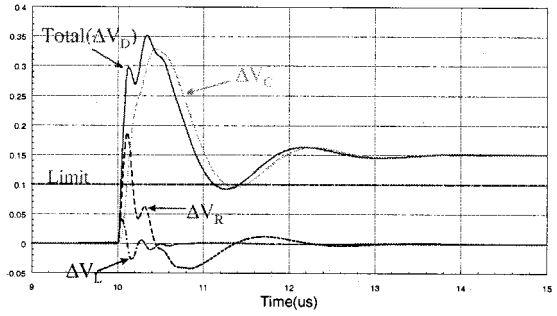

Fig. 8. Voltage drops distribution on decoupling capacitor (for future application: $Vo = 1.5$ V and load $= 30$ A).

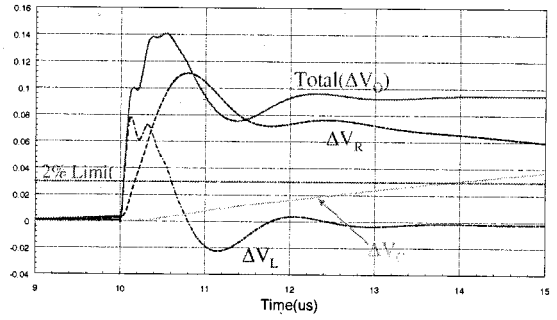

Fig. 9. Voltage drops distribution on VRM output capacitor (for future application: $Vo = 1.5$ V and load $= 30$ A).

is determined by the capacitance and the integral of the current

$$\Delta V_I = \frac{1}{C}\int i \cdot dt. \tag{3}$$

3) DIFFERENTIAL PART is caused by the di/dt on ESL of the capacitor

$$\Delta V_D = ESL \cdot \frac{di}{dt}. \tag{4}$$

The breakdown of the voltage drop on decoupling capacitors is shown in Fig. 8. The major part of voltage drop on decoupling capacitors is the integral part. It indicates that the decoupling capacitors do not have enough capacitance. It can be expected that effective increase of the decoupling capacitance can improve the performance greatly.

For VRM output bulk capacitors, the story is different. The three parts contributing to the voltage drop on bulk capacitors are shown in Fig. 9. The proportional part and the differential part contribute major portions to the voltage drop on the bulk

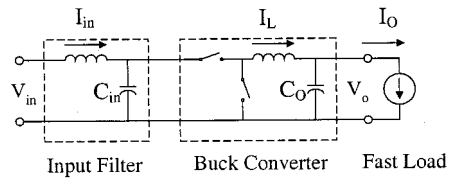

Fig. 10. Simplified VRM model.

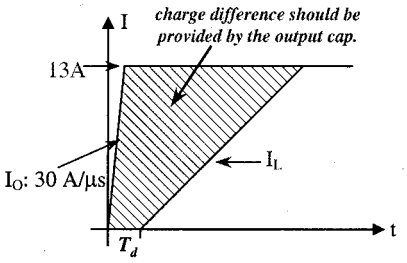

Fig. 11. Unbalanced current through Co during transient.

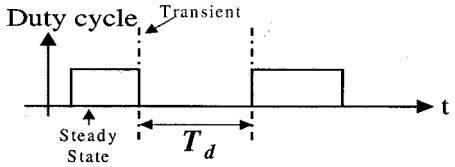

Fig. 12. Control delay.

capacitors. The capacitance of the bulk capacitors is not a big problem. The problem arises because of the high ESL and ESR of the bulk capacitors. High ESL restricts the speed at which the capacitor can provide current. ESR limits the largest current the capacitor can provide if the total voltage drop is set. It is obvious that effective reduction of ESL and ESR on bulk capacitors can be of great improvement to the performance. But, in today's VRM topologies, the bulk capacitor design is not that simple. Fig. 10 shows the simplified VRM model. The VRM output capacitance $\boldsymbol{C_O}$ is basically determined by the unbalanced current between the VRM output current $\boldsymbol{I_O}$ and the VRM inductor current $\boldsymbol{I_L}$ during transient.

The unbalanced current is determined by the two second-order resonant loops. The simplified curves are shown in Fig. 11. The shaded area is the charge that needs to be provided by the VRM output capacitor during the transient. It is determined by the delay time $\boldsymbol{T_d}$ and the slew rate of $\boldsymbol{I_L}$. The delay time $\boldsymbol{T_d}$ consists of the delay in the control feedback loop and the power stage. The major part of it is because of the switching frequency of the power stage. For today's application, the inductor charge voltage is equal to $Vin - Vo$, which is 1.9 V. And the inductor discharge voltage is V_o, which is 3.1 V. As a result, when the load changes from light load to heavy load, the output voltage has the largest voltage drop. The design of the VRM output filter capacitance has to make this voltage drop meet the requirement.

When a transient comes, the duty cycle of VRM can only be changed at the next switching cycle. The worst case is shown in Fig. 12. Change of the duty cycle can only start from the next switching cycle if the transient happens after the upper switch is turned off.

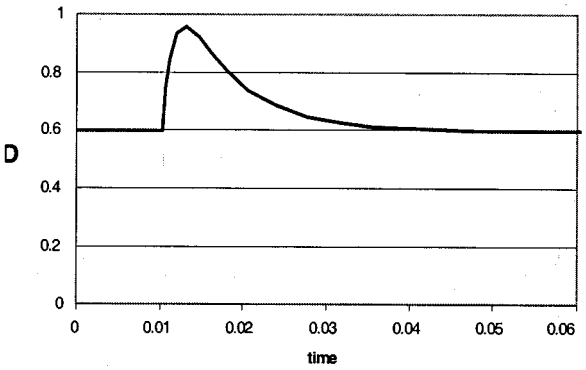

Fig. 13. Typical duty cycle signal during transient.

In worst case

$$T_d = (1-D)\cdot T_s = \frac{(1-D)}{F_s}. \tag{5}$$

During transient the current slew rate on the VRM output inductor is determined by the following formula:

$$\frac{dI_L}{dt} = \frac{D_{tr}V_{\text{in}} - V_o}{L} = \frac{V_{\text{in}}}{L}\cdot(D_{tr} - D) \tag{6}$$

where $\boldsymbol{D_{tr}}$ is the duty cycle during the transient, D is the steady state duty cycle.

The slew rate of $\boldsymbol{I_L}$ shown in Fig. 11 is the effective slew rate of the VRM output inductor current. From the circuit point of view the maximum slew rate can be got is when the duty cycle is saturated. The maximum inductor current charge slew rate is

$$\left(\frac{dI_L}{dt}\right)_{\max} = \frac{V_{\text{in}} - V_o}{L} = \frac{V_{\text{in}}}{L}\cdot(1-D). \tag{7}$$

However, this maximum duty cycle can not be achieved for the whole transient period with conventional voltage loop feedback design. The typical duty cycle curve during transient is shown in Fig. 13. The duty cycle can not be saturated for the whole transient period.

The effective inductor current charge slew rate can be approximated as

$$SR(I_L) = \frac{dI_L}{dt} = K\cdot\left(\frac{dI_L}{dt}\right)_{\max} = K\cdot\frac{V_{\text{in}} - V_o}{L}. \tag{8}$$

The VRM output capacitor need to maintain output voltage during transient. The capacitance requirement can be estimated as

$$C_o > \frac{\Delta I_o\cdot T_d}{\Delta V_o} + \frac{\Delta I_o^2}{2\cdot SR(I_L)\cdot\Delta V_o} \tag{9}$$

where $\Delta \boldsymbol{I}o$ is the load step magnitude of the transient, $\Delta \boldsymbol{V}o$ is the VRM output voltage drop due to the discharge of the output bulk capacitor, which is shown in (3). Considering the effect of ESL and ESR, leave one-third transient-voltage drop budget for capacitor discharge voltage $\Delta \boldsymbol{V}o$

$$\Delta V_o = \frac{5\%\cdot V_o}{3} = 50\,\text{mV}. \tag{10}$$

For worst case, $\Delta \boldsymbol{Io} = 13$ A. Let $Fs = 300$ KHz, $L = 2$ μH, $K = 0.5$, the output capacitance requirement can be estimated

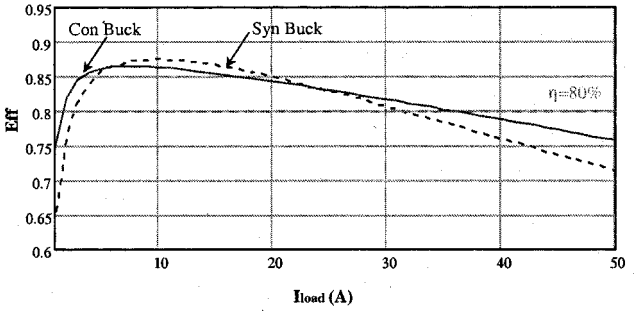

Fig. 14. Conventional VRM efficiency ($Vin = 5$ V, $Vo = 2$ V, $fs = 300$ kHz, switches: IRL3803).

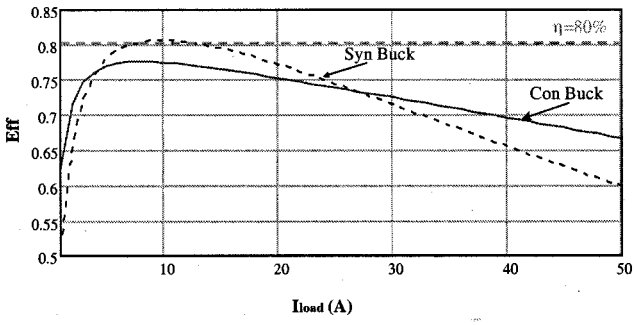

Fig. 15. Conventional VRM efficiency ($Vin = 5$ V, $Vo = 1.2$ V, $fs = 300$ kHz, switches: IRL3803).

as $Co > 3$ mF. In the simulation model shown in Fig. 3, four OSCON capacitors are used as output bulk capacitor, which has 820 μF capacitance, 12 mΩ ESR and 3 nH ESL each. The transient result is shown in Fig. 4, which can meet today's specification. Lots of today's commercial VRMs operates at 150 kHz switching frequency and use 3.8-μH output filter inductance. Usually, four to six 1500 μF aluminum capacitors are used as output bulk capacitors, which has 5 nH ESL and 30 mΩ each. For future application, $\Delta \boldsymbol{Io}$ is increased to 30 A. Let $Fs = 300$ KHz, $L = 2$ μH, $K = 0.5$ and $Vo = 2$ V. According to (9), the output capacitance needed is larger than 20 mF. Actually, since the output voltage is reduced, the largest voltage drop is happened when the load changes from heavy load to light load. The needed filter capacitance is even more. With such large capacitance, it will be too expensive and too large to use high performance low ESR capacitors like ceramic capacitors and the VRM will be very bulky.

The transient limitation of today's VRM topologies comes from their large output filter inductance. According to (9), the inductor current slew rate is too low. During the transient, this large inductor limits the energy transfer speed and the capacitors have to store or discharge all the energy from load. With the large output filter inductance, the VRM not only needs large filter bulk capacitance to reduce the third spike, but also requires large decoupling capacitance to reduce the second spike. For future application, if the VRM operates at 300 kHz with 2 μH filter inductor and enough bulk capacitance to maintain VRM output voltage regulation, the microprocessor still needs 23 times the decoupling capacitors to maintain the voltage drop on the decoupling capacitors lower than 100 mV during the transient [3]. However, the space of VRM is very limited and the real estate of motherboard is very expensive. The need of a large quantity of capacitors makes the VRMs, which use today's techniques, impractical for future microprocessors.

B. Limitation from Power Devices: Efficiency Limitation

Another limitation of the conventional VRM is efficiency. Fig. 14 shows the conventional VRM efficiency at 2-V output. Using IRL3803 as switches, with an on-resistance of 6 mΩ and 30 V voltage rating, the conventional VRM can not meet 80% efficiency requirement at heavy load. For lower output voltage, it will be even more difficult to meet the efficiency requirement. Fig. 15 shows the conventional VRMs' efficiency at 1.2-V

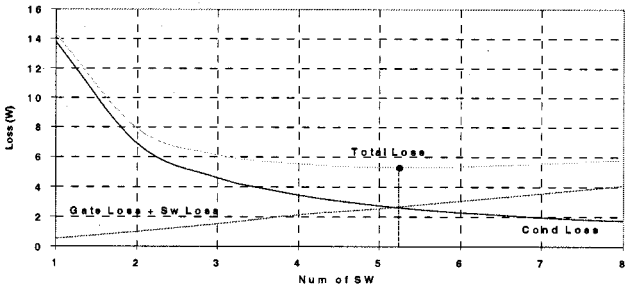

Fig. 16. Switching loss and gate drive loss and conduction loss of IRL3803 versus parallel switch number ($Vin = 5$ V, $fs = 300$ kHz, $Iload = 50$ A, total loss of IRL3803 is 6 mΩ).

output. Their efficiency can not meet the 80% requirement for the whole load range.

This limitation is from today's power device's technology. Based on vertical power MOSFET technology, most of today's low-voltage power MOSFETs are available at a rating of 30 V. Roughly, the total power loss of a power device can be divided into three parts

1) conduction loss;
2) gate drive loss;
3) switching loss.

Fig. 16 shows the relationship between conduction loss and gate drive plus switching loss. For this kind of low-voltage high-current application, conduction loss contributes a large percentage of the total loss. When only one IRL3803 is used, the MOSFETs conduction loss is 25 times gate drive plus switching loss. To reduce conduction and total loss, more switches need to be paralleled. However, this does not necessarily mean that more parallel switches equals lower total loss. When five IRL3803 are paralleled, the total loss is reduced to the minimum. After this point, paralleling more switches will not improve efficiency. Fig. 17 shows the VRM efficiency with five IRL3803 in parallel. With the optimized efficiency design, the VRMs efficiency still can not meet the 80% requirement for the whole load range. This limitation is due to high Figure of Merit (FOM) of today devices. FOM is equal to $Rdson$ times Qg. For today's device technology, the lowest FOM value is around 400 (m$\Omega \times nC$). With such a high FOM value, power devices not only limit the VRMs efficiency, but also limit the VRMs ability to operate at

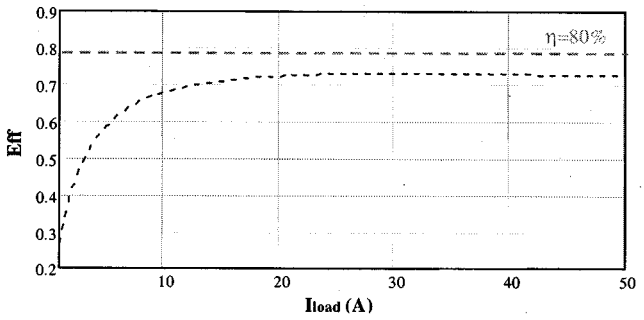

Fig. 17. Efficiency of synchronous buck VRM ($Vin = 5$ V, $Vo = 1.2$ V, $fs = 300$ kHz, 5 IRL3803 in parallel).

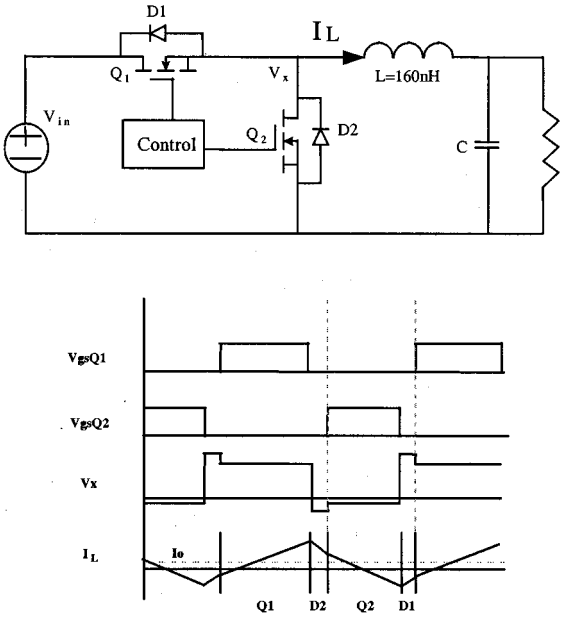

Fig. 18. Quasi-square-wave (QSW) VRM topology.

higher operating frequencies. Most of toady's VRMs operate at a switching frequency lower than 300 kHz. This low switching frequency causes slow transient response and very large energy storage components.

III. Advanced VRM Topologies

A. Fast VRM Topology—The Quasi-Square-Wave (QSW) VRM

To overcome the transient limitation occurring in conventional VRMs, smaller output filter inductance is more desirable to increase the energy transfer speed. Fig. 18 shows the quasi-square-wave (QSW) circuit and operation waveforms. When Q1 turns on, the input voltage charges the inductor current from negative to positive. After Q1 turns off and before Q2 turns on, the inductor current flows through Q2's body diode. Then Q2 can turn on at zero voltage. After Q2 turns on, the inductor current is discharged to negative. After Q2 turns off and before Q1 turns on, the inductor current flows through Q1 body diode. Then Q1 can turn on at zero voltage. In QSW topology, both top switch and bottom switch can turn on at zero voltage. The miller effect in both switches is eliminated and the gate drive loss and switching loss is reduced. The QSW topology keeps the VRM

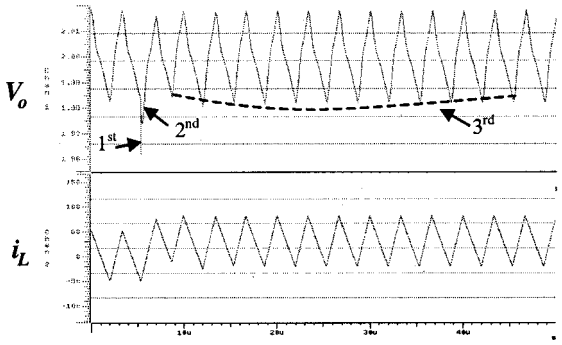

Fig. 19. Transient response of the QSW.

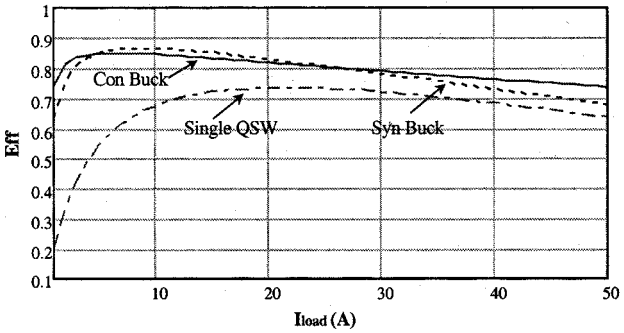

Fig. 20. Efficiency of the QSW compared with a conventional VRM ($Vin = 5$ V, $Vo = 2$ V, $fs = 300$ kHz).

output inductor current peak to peak value is two times the full load current, which make the inductor current go negative in all load range. Its inductor design is according to

$$L \leq \frac{(Vin - Vo) \times D}{2 \times Io \times fs}. \tag{11}$$

Compared with inductor design [see (1)] in conventional buck and synchronous buck topologies, its output filter inductance is reduced significantly, 20 times smaller. At 13 A load and 300 kHz switching frequency, it needs only a 160 nH inductor as compared with a 2∼4 μH inductor used in the conventional design at the same frequency. This small inductance makes the VRM transient response much faster. Fig. 19 shows the transient response of the QSW topology. The third spike in output voltage becomes insignificant and the second spike is reduced significantly.

There are two disadvantages in this fast VRM topology. The first one is the large current ripple. Large VRM output filter capacitance is needed to suppress the steady state ripple. Smaller inductance results in faster transient response, but requires larger bulk capacitance. The second one is its low efficiency shown in Fig. 20. Due to the large ripple current, QSW switches have larger conduction loss. Its efficiency is lower than that of conventional VRMs.

B. A Fast VRM with a Small Ripple—The Interleaved QSW VRM

In order to meet both the steady state and transient requirements, a novel VRM topology, the interleaved QSW, is proposed

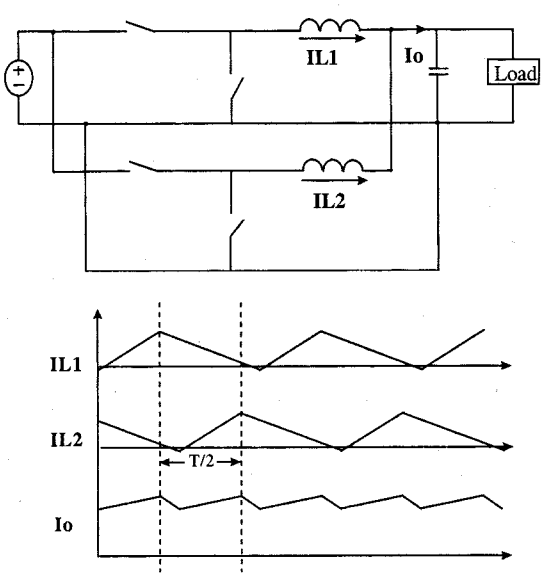

Fig. 21. Current ripple canceling effect of interleaved QSW.

in Fig. 21. The interleaved QSW topology naturally cancels the output current ripple and still maintains the fast transient response characteristics of the QSW topology. A smaller capacitance is needed compared to both the single-module QSW VRM and the conventional VRM design. Fig. 22 shows the comparison of ripple canceling effect in two-module interleaved QSW VRM and four-module interleaved QSW VRM. In two-module interleaved VRM, only when duty cycle is 0.5, the ripple is fully canceled. But, in four-module interleaved VRM, the ripple can be fully canceled when duty cycle is 0.5 or 0.25 or 0.75. If duty cycle is not at these points, for example, when duty cycle is 0.3, 80% ripple is canceled in four-moduel structure and only 45% ripple is canceled in two-module structure. The more modules in parallel, the better the ripple canceling effect.

Fig. 23 shows a four-module interleaved QSW VRM. Fig. 24 shows its transient response. Fig. 24(a) shows the current in each single module, which has large ripple. Fig. 24(b) shows the total current in output, which has very small ripple. Fig. 24(c) shows the output voltage during transient. The results show that this technique can meet future transient requirements without a large steady-state voltage ripple. In the simulation shown in Fig. 24, the full load current is 30 A and the output voltage is 2 V. Each channel handles 7.5 A current and operates at 300 kHz. According to (11), the inductance is 320 nH in each channel. The equivalent inductance is 80 nH. Compared with traditional technology, 2 μH in Fig. 3, the filter inductance is reduced by 25 times. Therefore, the inductor current charge slew rate is increased by 25 times. Another benefit is the delay time is reduced by 75%. According to (9), the output capacitance needed is only 2 mF. Considering the worst case when load change from heavy load to light load, in the simulation, 3 mF bulk capacitance is used. Meanwhile, due to the small inductance, the decoupling capacitance needed is only three times, as compared with 23 times requirement in conventional technologies. The interleaved QSW topology can not only reduce output current ripple, but can also reduce input current ripple. For the same load, both input and output filter size can be dramatically reduced. As a result, interleaved QSW VRM can achieve very high power density and motherboard space can be saved. Fig. 25 shows the efficiency comparison results. For conventional buck, synchronous buck and single channel QSW VRM, IRL3803 is used as switches, which has 6 mΩ on resistance. For interleaved QSW VRM, each channel uses Si4480 as switches, which has 18.5 mΩ on resistance. Compared with the single-module QSW topology, since the equivalent silicon die size is increased, the interleaved QSW VRM has higher efficiency.

IV. Experimental Evaluations

A four-module interleaved QSW VRM is built and tested. The prototype is shown in Fig. 26. This VRM is designed for 5 V input voltage and 2 V output voltage. The load current changes from 0.8 A to 30 A. The power devices are Si4410DY, which has 14 mΩ on resistance and SO-8 package. Each module operated at 300 kHz. The output ripple frequency is 1.2 MHz. The inductance in each module is 320 nH. The equivalent inductance of the four-module interleaved VRM is 80 nH. The output filter capacitance totally is 1200 μF. The output capacitors are combined by ceramic and tantalum capacitors. The profile of the power stage is 0.3 in. The power density is higher than 30 W/in^3.

In the VRM, integrated magnetic design is used. Every two inductors use one magnetic core. As a result, totally, two magnetic cores are used for these four channel inductors. Fig. 27 shows the integrated magnetic structure [4]. By taking advantage of interleaVing technology, AC flux of the two inductors is canceled in the center leg. As a result, the core loss and center leg crossing area is reduced. The planar core structure make the VRM very low profile. And this kind of low profile magnetic also has good thermal management. In the magnetic design, the PCB trace is used as inductor winding. With symmetrical PCB layout design, the resistance of the PCB winding can be used to control average inductor current. Thus, the current sharing in each module can be achieved [5]. This approach is very cost effective.

Fig. 28 shows the VRM transient response. When load change from 0.8 A to 15 A and vice versa, the four-module interleaved QSW VRM has only 40 mV voltage drop as compared to conventional VRM which has 150 mV voltage drop. Fig. 29 show the VRM efficiency. At 30 A full load, its efficiency is higher than 85%. Table II compares the design of interleaved QSW VRM and conventional VRM. The interleaved QSW VRM uses much smaller capacitance, only one-sixth capacitance used in conventional VRM. And its power density is much higher, six-time higher than that of a conventional one.

V. Future VRMS—High Frequency, High Power Density

In order to develop low-cost, high-efficiency, low-profile, high-power density, fast-transient-response, board-mount VRM modules for future generation microprocessor loads, high operating frequencies are desirable. Fig. 30 shows the transient response of the interleaved QSW VRM when it operates at 1 MHz. Obviously, the voltage spike is reduced significantly.

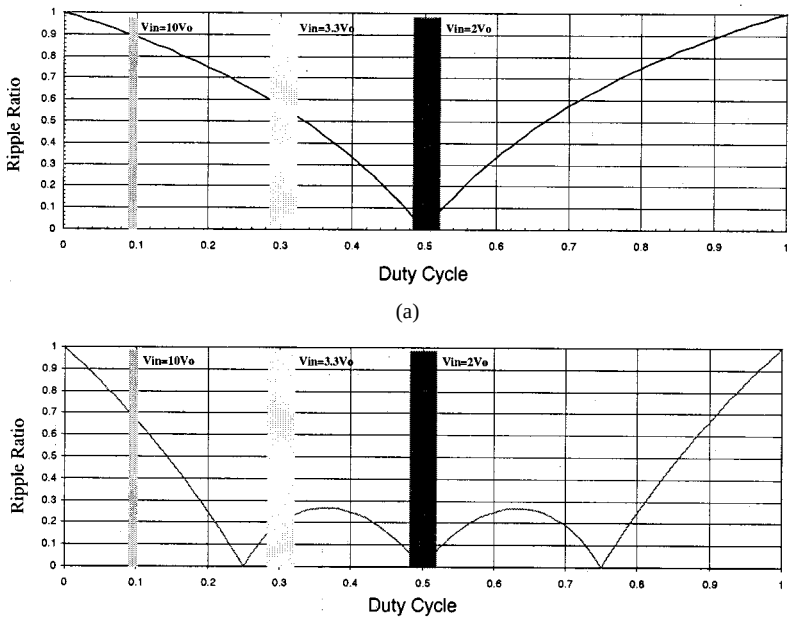

Fig. 22. Ripple canceling effect: (a) two modules interleaved and (b) four modules interleaved.

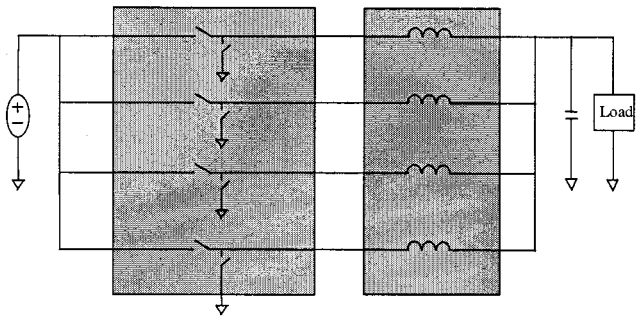

Fig. 23. Four-module interleaved QSW VRM.

Fig. 31 shows the inductance and capacitance needed in the interleaved QSW VRM when it operates at a high switching frequency. At 10 MHz, the inductance needed is only 9.25 nH and the capacitance needed is only 5.26 μF. With such a small inductance and capacitance, very high-power-density VRMs can be created and energy storage costs can be dramatically reduced. However, due to today's device technology, most VRMs' operating frequencies are lower than 300 kHz. Even at this frequency, the VRM can not meet efficiency requirements. When the frequency is increased, the resulting VRM efficiency levels are shown in Fig. 32. At 10 MHz, the VRM will only have 40% efficiency. This efficiency makes thermal management and packaging very difficult.

For future microprocessor application, the power device must have a smaller FOM value [$< 100(\text{m}\Omega \times nC)$] and a lower miller charge. With improved device technologies, such as the SOI LDDMOS technology [6], future VRM efficiency will be higher than 90% at several MHz operating frequencies. Fig. 33 shows the difference between a vertical DMOS and the proposed LDD MOSFET on SOI structure. Whose power density will be higher than 100 W/in^3. Table III shows the VRM efficiency comparison based on today's device technology and the improved LDDMOS technology.

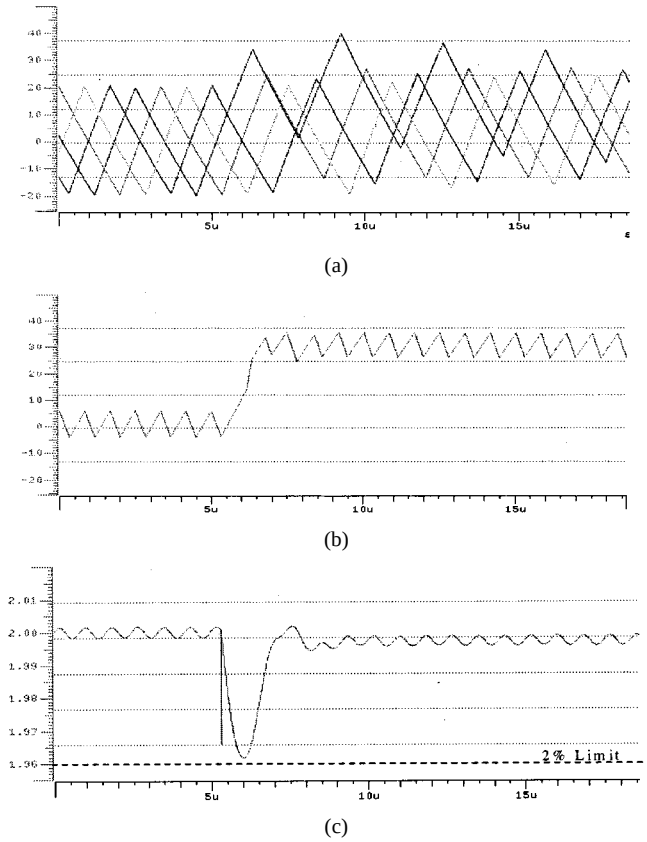

Fig. 24. Transient response of the four-module interleaved QSW: (a) current in each module, (b) total output current, and (c) output voltage.

Although advanced topologies have very fast transients and future device techniques can operate at very high frequencies, in order to minimize the effects of the interconnection, an innovation design with a possible integration of the VRM and the processor is still the key to meeting the ever-increasing demand for processor performance and speed.

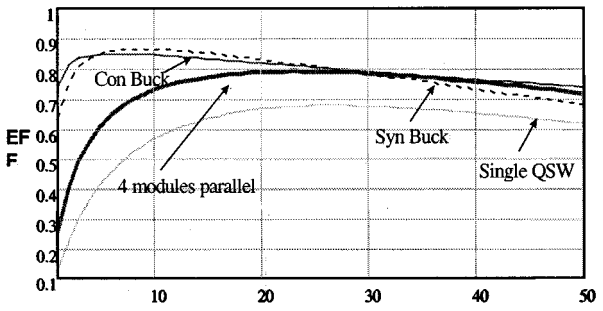

Fig. 25. Efficiency comparison.

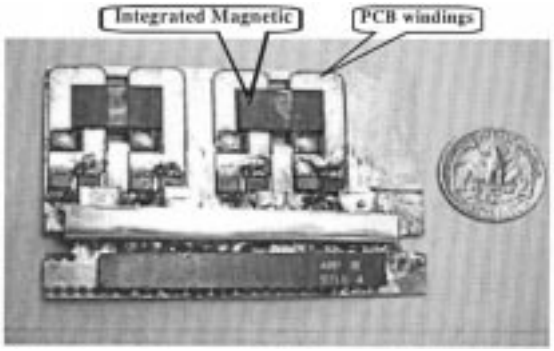

Fig. 26. Four-module interleaved QSW VRM.

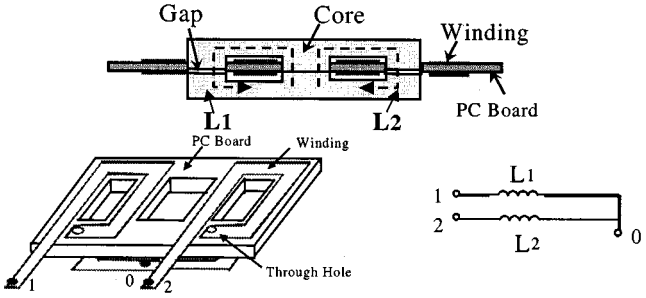

Fig. 27. Integrated magnetic structure: (a) integrated magnetic structure and (b) implementation of the integrated magnetic.

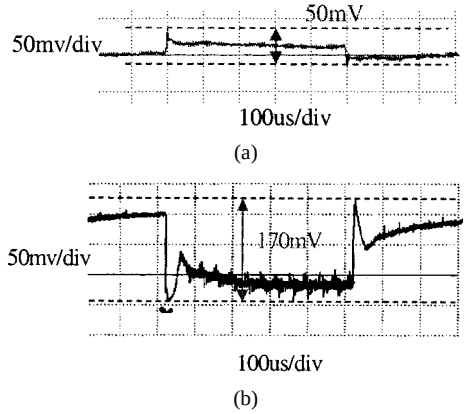

Fig. 28. Transient response test results: (a) transient response of the four-module interleaved QSW and (b) transient response of the conventional VRM.

The integration of the VRM with the processor can take either a hybrid or a monolithic approach. In the hybrid approach,

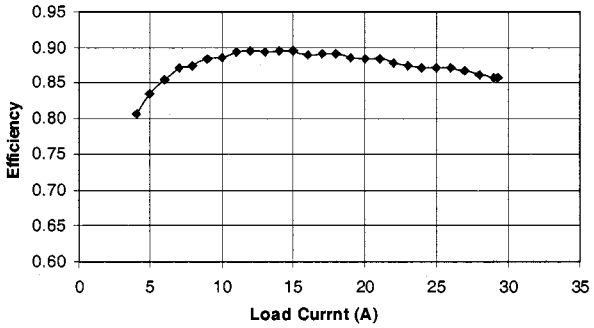

Fig. 29. Efficiency of four-module interleaved QSW VRM.

TABLE II
DESIGN COMPARISON OF THE INTERLEAVED QSW VRM AND THE CONVENTIONAL VRM

	Interleaved QSW	Conventional VRM
Vin	5	5
Bulk capacitance	1200uF	7500uF
Output Inductance	320nH (×4)	3.8uH
Transient voltage drop:	50 mV	150 mV
Vo @ load	2V@30A	2V@13A
Power stage power Density (W/in^3)	30	3~5

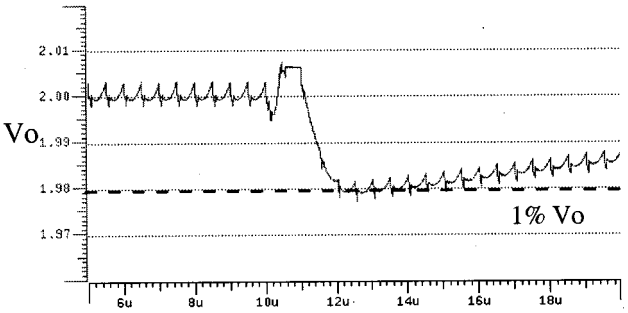

Fig. 30. Transient response of the interleaved QSW ($Vin = 5$ V, $Vo = 2$ v, $fs = 1$ MHz).

the VRM can be made as a silicon chip with all the control functions. As shown in Fig. 34(a) and (b), several VRM chips can be placed in parallel and be mounted close to the microprocessor on the same cartridge. Ceramic capacitors with small ESRs and ESLs can be used as the output capacitors, and can be placed on the PCB board next to the processor. By connecting the output of the VRM and the power input of the processor via a path through a magnetic material sheet, the small output inductor can also be created. With this kind of packaging approach, interconnection parasitics can be minimized. For future application, some other advanced packaging technologies, such as flipchip, can also be used.

VI. CONCLUSIONS

Except for adding capacitors, it is difficult for conventional VRMs to meet the transient requirements for future microprocessors. The interleaved QSW topology can significantly improve VRM transient response. With this technique, both VRM

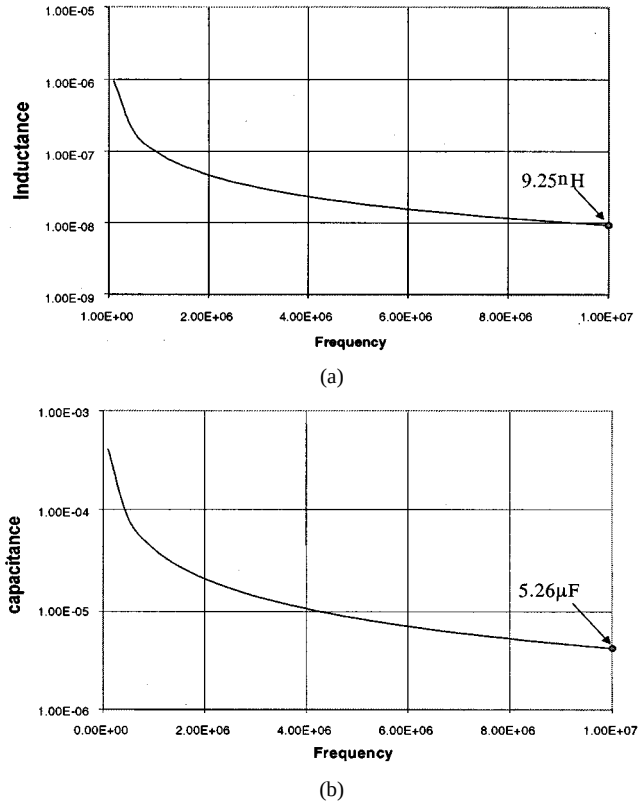

Fig. 31. Inductance and capacitance needed in the interleaved QSW VRM topology at a high operating frequency: (a) inductance needed versus frequency and (b) capacitance needed versus frequency.

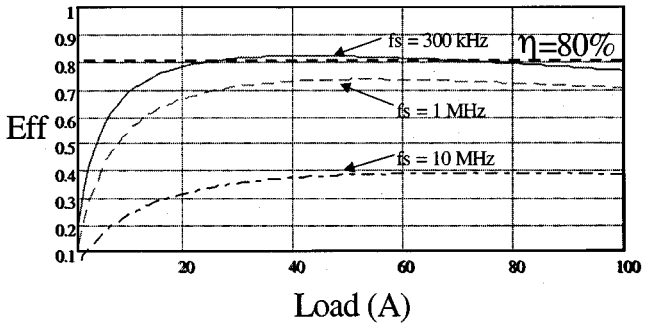

Fig. 32. VRM efficiency based on today's device technology ($Vin = 5$ V, $Vo = 2$ V, switches: 5 IRL3803 in parallel).

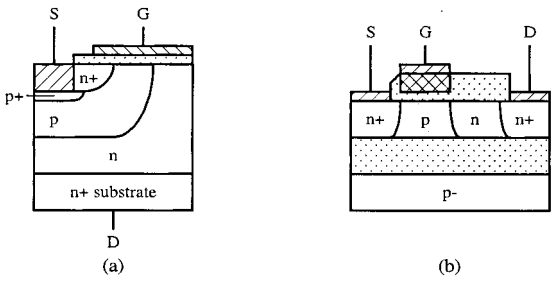

Fig. 33. Future power device technology.

input current ripple and output current ripple are canceled. Both VRM input and output filter sized can be dramatically reduced.

TABLE III
VRM EFFICIENCY COMPARISON

Vin=5V, Vo=2V	BV (V)	FOM (mΩ*nC)	Optimized Efficiency For Interleaved QSW VRM		
			300kHz	1 MHz	10MHz
LDDMOS	10	77	95%	91%	88%
Today's Device	30	473	87%	79%	60%

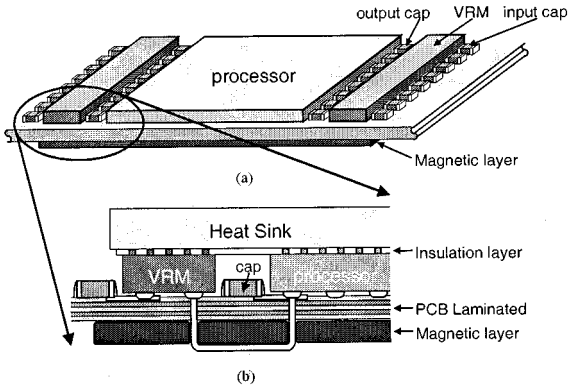

Fig. 34. Hybrid approach: (a) 3-D view and (b) side view.

As a result, the interleaved QSW VRM can achieve very high power density and can be easily packaged.

ACKNOWLEDGMENT

The authors would like to thank Dr. X. Zhang, Dr. W. Chen, Dr. D. Y. Chen, J. Liu, J. Chen, N. Sun, L. Amoroso, and H.-P. Wu for their exemplory teamwork, without whom this paper could not have been accomplished.

REFERENCES

[1] S. Goodfellow and D. Weiss, "Designing power systems around processor specifications," *Electron. Design*, pp. 53–57, January 1997.
[2] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, "Design consign considerations for low-voltage on-board DC/DC modules for next generations of data processing circuits," *IEEE Trans. Power Electron.*, vol. 11, Mar. 1996.
[3] P. Wong, X. Zhou, J. Chen, H. Wu, F. C. Lee, and D. Y. Chen, "VRM transient study and output filter design for future processors," in *Proc. VPEC Sem.'97*, 1997.
[4] W. Chen, F. C. Lee, X. Zhou, and P. Xu, "Integrated planar innductor scheme for multi-module interleaved quasisquare-wave DC/DC converter," in *Proc. IEEE PESC'99*, 1999.
[5] X. Zhou, X. Peng, and F. C. Lee, "A high power density, high efficiency and fast transient voltage regulator module with a novel current sensing and current sharing technique," in *Proc. IEEE APEC'99*, 1999.
[6] A. Q. Huang, N. X. Sun, B. Zhang, X. Zhou, and F. C. Lee, "Low voltage power devices for future VRM," in *Proc. ISPSD'98*, 1998, pp. 395–398.
[7] B. You, A. Huang, and J. Sin, "A new trench bipolar junction diode," in *Proc. ISPSD*, 1999, pp. 133–136.
[8] A. Rozman and K. Fellhoelter, "Circuit considerations for fast sensitive, low-voltage loads in a distributed power system," in *Proc. IEEE APEC'95*, 1995.
[9] X. Zhou, X. Zhang, J. Liu, P.-L. Wong, J. Chen, H.-P. Wu, L. Amoroso, F. C. Lee, and D. Y. Chen, "Investigation of candidate VRM topologies for future microprocessors," in *Proc. IEEE APEC'98 Conf.*, 1998.

Xunwei Zhou (M'99) received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1991 and 1994, respectively, and the Ph.D. degree from the Virginia Polytechnic Institute and State University, Blacksburg, in 1999.

He joined Volterra Semiconductor Company, Fremont, CA, in 1999. His research interests include design and control of distributed power system, high-frequency power conversion and magnetics, PFC techniques, and low-voltage power management techniques.

Pit-Leong Wong (S'99) was born in Fujian, China, in 1971. He received the B.E. degree in control, B.S. degree in physics, and M.S. degree in systems engineering, all from Tsighua University, Beijing, China, in 1994 and 1996, respectively, and is currently pursuing the Ph.D. degree in power electronics at the Virginia Polytechnic Institute and State University, Blacksburg.

Mr. Wong is a member of Phi Kappa Phi.

Peng Xu was born in Zhejiang, China, in 1973. He received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1994 and 1997, respectively, and is currently pursuing the Ph.D. degree in power electronics at the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg.

Fred C. Lee (S'72–M'74–SM'87–F'90) received the B.S. degree in electrical engineering from the National Cheng Kung University, Taiwan, R.O.C., in 1968, and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, in 1971 and 1974, respectively.

He is a University Distinguished Professor at the Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, and was the Lewis A. Hester Chair of Engineering at Virginia Tech and the James S. Tucker endowed professor in the Bradley Department of Electrical and Computer Engineering. He directs the Center for Power Electronics Systems (CPES), a National Science Foundation engineering research center whose participants include five universities and over 100 corporations. In addition to Virginia Tech, participating CPES universities are the University of Wisconsin-Madison, Rensselaer Polytechnic Institute, North Carolina A&T State University, and the University of Puerto Rico-Mayaguez. He is also the Founder and Director of the Virginia Power Electronics Center (VPEC), one of the largest university-based power electronics research centers in the country. His research interests include high-frequency power conversion, distributed power systems, space power systems, power factor correction techniques, electronics packaging, high-frequency magnetics, device characterization, and modeling and control of converters.

Dr. Lee received the Society of Automotive Engineering's Ralph R. Teeter Education Award (1985), Virginia Tech's Alumni Award for Research Excellence (1990), and its College of Engineering Dean's Award for Excellence in Research (1997). In 1989, he received the William E. Newell Power Electronics Award, the highest award presented by the IEEE Power Electronics Society for outstanding achievement in the power electronics discipline. He is also the recipient of the Power Conversion and Intelligent Motion Award for Leadership in Power Electronics Education (1990) and the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology (1998). From 1993 to 1994, he served as President of the IEEE Power Electronics Society and, before that, as Program Chair and then Conference Chair of IEEE-sponsored power electronics specialists conferences.

Alex Q. Huang (SM'97) received the B.S. degree from Zheijiang University, China in 1983, the M.S. degree from the Chengdu Institute of Radio Engineering, China, in 1986, both in electronic engineering, and the Ph.D. degree from Cambridge University, Cambridge, U.K., in 1992.

He is an Assistant Professor with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg. Since 1983, he has been involved in the development of modern power semiconductor devices and power integrated circuits. He fabricated the first IGBT power device in China in 1985. While at Cambridge, he developed a high voltage power IC process to integrate power devices and advanced CMOS devices using conventional CMOS technology. His other works include research on monolithic power electronics systems such as the monolithic voltage regulator module (MVRM). He has published more than 70 papers in the international conferences and journals, and has four U.S. patents and more than ten inventions pending for United States and United Kingdom patents.

Dr. Huang received the NSF presidential career award.