Short Summary on Stacked DC-DC Systems

1 Schematics of stacked DC-DC systems

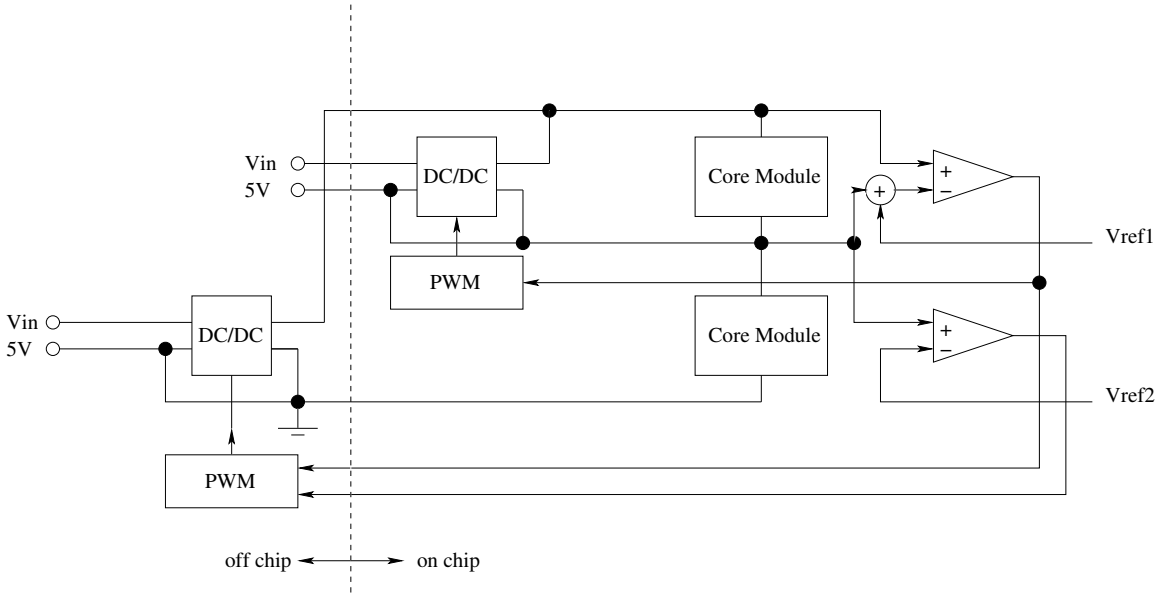

Figure 1: Schematic of 2-level stacked DC-DC converters

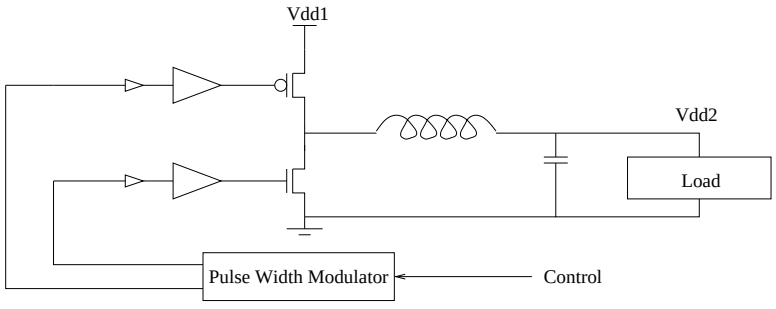

Figure 2: Schemattic of Buck DC-DC converter

2 Determination of design parameters

2.1 Buck DC-DC converters

2.1.1 zero voltage switching

Zero voltage switching (ZVS) means that the internal point of DC-DC converters switches under a zero voltage. [1] has detailed description on how to achieve zero voltage switching. My experiment results show that under 5MHz operation frequency, without ZVS results in an over 15% additional power loss. It also increases with the operation frequency. Therefore, ZVS is critical if we want to use high operation frequency to reduce the area of LC filter.

2.1.2 Output voltage ripple

According to [2], the current ripple on the inductor and voltage ripple on the capacitor are

$$\Delta i = \frac{(V_{DD1} - V_{DD2})D}{2Lf_s} \tag{1}$$

and

$$\Delta V_{DD2} = \frac{(V_{DD1} - V_{DD2})D)}{16LCf_s^2} = \frac{\Delta i}{8Cf_s} \tag{2}$$

, respectively, where L is the filter inductance, C is the filter capacitance, f_s is the switching frequency, and D is the duty cycle. This formulas have been verified by SPICE simulations.

2.1.3 Power efficiency

The efficiency of a buck converter is

$$\eta = 100 \times \frac{P_{load}}{P_{load} + P_{buck}} \tag{3}$$

where P_{buck} is the average total internal power consumption of a buck conversion, which could be approximated by the total power loss of two power transistors. The total power loss of a MOSFET is a combination of conduction losses and dynamic switching losses, i.e.,

$$P_{MOS} = i_{rms}^2 R + \frac{\alpha}{\alpha - 1}(C_{ox} + C_{gs} + 2C_{gd} + C_{db})V_{DD1}^2 f_s, \tag{4}$$

where R is the equivalent resistance of the transistor, i_{rms} is the root mean square current passing through the MOSFET, α is the tapering factor of the power MOSFET gate drivers, C_{ox}, C_{gs}, C_{gd} and C_{db} are the gate oxide, gate-to-source overlap, gate-to-drain overlap and drain-to-body junction capacitances, respectively. The equvivalent resistance of the transistor can be calculated as

$$R = \frac{1}{\mu_n c_{ox}(V_{DD1} - V_{th})} \cdot \frac{L}{W}, \tag{5}$$

where μ_n is the electron mobility with a typical value of $0.05m^2V^{-1}s^{-1}$, and

$$c_{ox} = \frac{\epsilon_0 \epsilon_{SiO_2}}{T_{ox}} \tag{6}$$

$$= \frac{8.854 \cdot 10^{-14} \cdot 3.9}{2.5 \cdot 10^{-9}} \tag{7}$$

$$= 1.38 \times 10^{-4} (F/m^2) \tag{8}$$

Here, we use 100nm generation and assume T_{ox} equals to $2.5 \cdot 10^{-9}m$.

2.2 Stacked buck DC-DC converters

2.2.1 Output voltage ripple

2.2.2 Power efficiency

References

[1] A. Stratakos, S. Sanders, and R. Brodersen, "A low-voltage cmos dc-dc converter for a portable battery-operated system," in *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, June 20-25, 1994, pp. pp. 619–626.

[2] V. Kursun, S. Narendra, V. De, and E. Friedman, "Analysis of buck converters for on-chip integration with a dual supply voltage microprocessor," vol. 11, no. 3, pp. 514 – 522, June 2003.