Techniques for Improving the Accuracy of Geometric-Programming Based Analog Circuit Design Optimization

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Abstract

We present techniques for improving the accuracy of geometric-programming (GP) based analog circuit design optimization. We describe major sources of discrepancies between the results from optimization and simulation, and propose several methods to reduce the error. Device modeling based on convex piecewise-linear (PWL) function fitting is introduced to create accurate active and passive device models. We also show that in selected cases GP can enable nonconvex constraints such as bias constraints using monotonicity, which help reduce the error. Lastly, we suggest a simple method to take the modeling error into account in GP optimization, which results in a robust design over the inherent errors in GP device models. Two-stage operational amplifier and on-chip spiral inductor designs are given as examples to demonstrate the presented ideas.

Keywords: convex optimization, geometric programming, analog circuit synthesis

1. Introduction

The recent trend in ICs is an increasing integration of analog and digital functions. This trend relies on design automation to meet time-to-market and cost-effectiveness. Digital design community has well-developed suites of design automation tools that have helped designers significantly enhance productivity; meanwhile design tools for analog and mixed-signal circuits still lag. To bridge the gap, there has been extensive research in computer-aided design of analog and mixed-signal circuits.

Analog design synthesis has been a particularly active area of research [1]. Recently a technique using geometric programming (GP) [2] has attracted considerable attention by proving its viability in optimizing CMOS opamps [2], pipelined ADC [3] and CMOS DC-DC buck converter design [4].

The major limitations of this approach are the incapability of handling non-convex constraints, which can be critical in many cases, and the discrepancy between the results from the GP optimization and traditional circuit verification tools such as SPICE. One approach to alleviate the former is solving a series of GPs as known as reversed GP (RGP) [5], while the latter still remains a challenging task especially with deep submicron technology.

The major source of the discrepancy is two-fold. First, because GP is a subset of *convex optimization*, the discrepancy is inherent because accurate transistor characteristics in models such as BSIM3v3[1] are not convex functions. The approximation as a convex function inevitably leads to some degree of modeling error. Second, the error in estimating the circuit biasing by the GP can result in a significant prediction discrepancy between SPICE and GP. We refer to this error in estimating the bias as a *bias estimation error*.

This paper presents several methods to reduce the prediction discrepancies by addressing errors due to both modeling and bias estimation. Section 2 reviews previous work in this area and illustrates several sources of error in the published approach. Section 3 presents a new device modeling method and its practical variant which enable us to achieve accurate modeling of device characteristics in deep sub-micron technology. Section 4 describes a useful technique that can reduce the bias estimation error by enabling posynomial equalities, which are non-convex constraints, utilizing monotonicity. Section 5 suggests a simple method to take the inherent modeling errors into consideration in GP-optimization, which yields a robust design over modeling errors in GP. Section 6 shows how these ideas are applied to the design of a two-stage opamp and on-chip spiral inductor. We give concluding remarks in section 7.

2. Previous work

Geometric programming (GP) is an optimization problem that has the following format

$$\begin{array}{lll} \text{minimize} & f_0(x) & \\ \text{subject to} & f_i(x) \le 1, & i = 1, \ldots, m \\ & g_i(x) = 1, & i = 1, \ldots, p \\ & x_i > 0, & i = 1, \ldots, n \end{array} \quad (1)$$

where f_i are *posynomial* functions and g_i are *monomial* functions. A *posynomial* function is defined as

$$f(x_1, \ldots, x_n) = \sum_{k=1}^{K} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_n^{\alpha_{nk}}, \quad x_i > 0. \quad (2)$$

Posynomial functions, or posynomials, are real-valued functions of n real, positive variable x_i with nonnegative coefficients $c_k \ge 0$ and any real exponents $\alpha_{ij} \in \mathbf{R}$. When the

[1] We are using BSIM3v3 model as the benchmark data. The same modeling can be applied to measured data.

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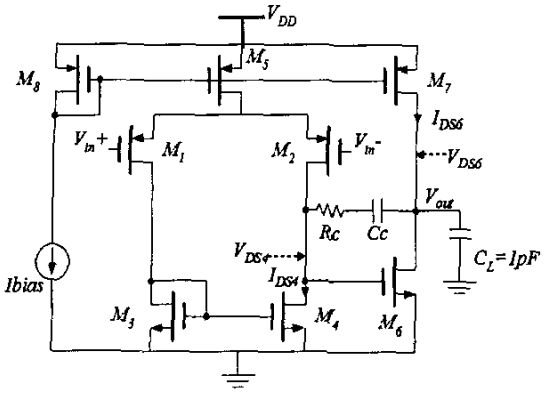

Figure 1. Two-stage OPAMP design

posynomial has only a single term, it is known as a *monomial, i.e.,*

$$g(x_1, \ldots, x_n) = c_1 x_1^{\alpha_1} x_2^{\alpha_2} \cdots x_n^{\alpha_n}, \quad x_i > 0. \qquad (3)$$

Geometric programs can be transformed to convex optimization problems by a change of variable and a transformation of objective and constraint function [6].

Previous work, [2], casts a two-stage opamp design problem in Figure 1 as GP using monomial device models. Although it produced excellent results in long-channel devices, the predictions from GP-based optimization in the short-channel regime can deviate considerably from SPICE simulation. We illustrate this in the following example.

We optimized the two-stage opamp in Figure 1 such that gain-bandwidth product is maximized by using the problem formulation in [2]. In order to extend the work to the short-channel regime, we created new monomial device models for TSMC $0.18-\mu m$ technology where model fitting is done via L_∞ minimization [6] over about 2000 data points.

Table 1 shows the modeling errors of design parameters in N/PMOS devices operating in saturation region. We listed max/mean percentage modeling errors ($|(f_{model} - f_{spice})/f_{spice}| * 100$) for selected monomial design parameters. Although errors are reasonable for some characteristics, the parameter such as g_{ds} exhibits significant modeling error whose maximum is over 100%. Clearly, these errors translate into the discrepancy between GP prediction and SPICE simulation.

Table 2 illustrates the bias estimation error and its impact on the small-signal gain specification. Note that in SPICE simulations, bias conditions (*i.e.* I_{DS}) are determined through bias calculations with the given W and L of the transistors and the circuit topology. The small-signal performance specifications (*i.e.* D.C. gain) depend on the bias conditions. In the GP-optimization, we obtain the size (W and L), biasing (I_{DS}) and small-signal characteristics of all transistors simultaneously as a result of solving the problem. When simulating the circuit with the GP-predicted W and L in SPICE, the discrepancy in bias-related variables, which we refer to as *bias-estimation error*, can result in significant deviation in the small-signal performance specifications. In this example, the bias estimation error in I_{DS6}, as shown in the third row in Table 2, is compounded with the inherent modeling error of g_{ds6} and reflected in the significant prediction error for open-loop gain as shown in Table 2.

Table 1. Max/mean % modeling error in monomial models

Design Parameter	Variables	% error NMOS	% error PMOS
$1/g_m$	W, L, I_{DS}	29.8/10.9	23.1/7.4
g_{ds}	W, L, I_{DS}	132.7/49.7	128.8/48.7
$V_{GS} - V_{TH}(= V_{OV})$	W, L, I_{DS}	26.9/10.1	20.3/6.7

Table 2. Bias estimation error and its impact on performance

	GP	SPICE
W_6 $[\mu m]$	12.2	12.2
L_6 $[\mu m]$	0.33	0.33
I_{DS6} $[\mu A]$	159.4	181.6
g_{ds6} $[\mu S]$	20.6	122.7
Open-loop gain	3162 (70dB)	707 (57dB)

With these sources of errors, we propose several methods to help minimize the prediction error. First, in section 3, we minimize modeling error using a convex piecewise-linear function fitting that achieves the highest fitting accuracy for design parameters. Second, section 4 suggests a method to minimize the bias estimation error by enabling nonconvex bias constraints using monotonicity. Also, in section 5 we describe a GP-formulation technique that accounts for inherent modeling errors in the optimization which in turn helps the GP predictions meet the given specifications

3. Convex piecewise-linear device modeling

In order to cast the circuit design problem as a GP-optimization problem, design parameters must be either in the form of monomial or posynomial depending on where and how they appear in actual design constraints. For instance, a typical minimum gain (A_{min}) specification

$$g_m \cdot r_o = g_m / g_{ds} \geq A_{min} \qquad (4)$$

translates into the following inequality

$$A_{min} \cdot 1/g_m \cdot g_{ds} \leq 1 \qquad (5)$$

Since posynomials are closed under multiplication, (5) remains a posynomial inequality as long as $1/g_m$ and g_{ds} are either monomials or posynomials of design variables. Note that posynomial type of g_m and $r_o(= 1/g_{ds})$ does not result in a posynomial inequality. Since some of the device characteristics such as $1/g_m$ and g_{ds} in (5) can be modeled using posynomials

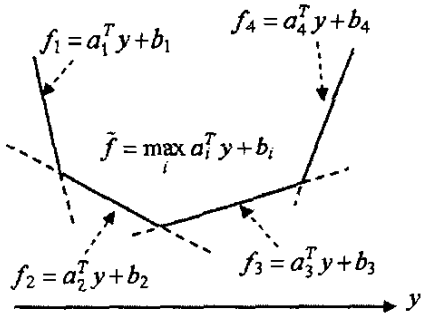

Figure 2. Covex piecewise-linear (PWL) function

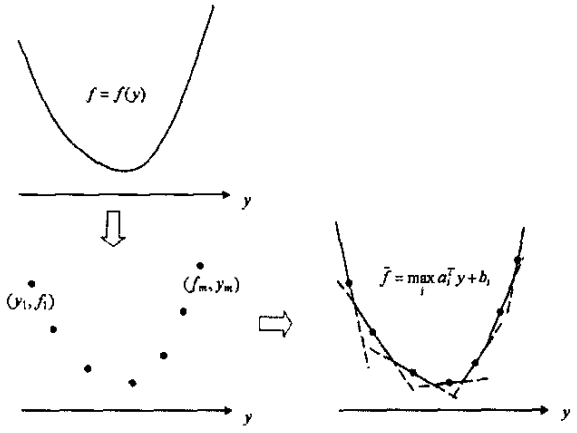

Figure 3. Concept of convex piecewise-linear function fitiing

instead of monomials, the model can be fitted to actual characteristics with greater accuracy. Unfortunately, however, there is no reported obvious convex formulation for posynomial fitting. Some methods are addressed in [7] and [8], but both require heuristic parameter selections and it's difficult to address the optimality of the fittings. The method in [9] uses similar idea of this work, *i.e.* piecewise-linear function fitting, but does not consider the convexity of the fitting function, therefore is not compatible with GP. This paper proposes an alternative fitting algorithm which guarantees the smallest possible modeling error for a given set of data without heuristic intervention.

First, we define

$$\tilde{f}(y) = max_i\ f_i(y) \tag{6}$$

as a *convex piecewise-linear* (PWL) function where $f_i(y)$ is a linear functions of y. As illustrated in Figure 2, it can be easily proven that $\tilde{f}(y)$ is a convex function [6].

Second, we note that data set $(y_i, f_i),\ i = 1, \ldots, m$ generated by any convex function can be fitted by a PWL function with an *arbitrarily small* fitting error if we are allowed to tailor the PWL function with an *arbitrarily large* number of segments. An easy example of this argument is the

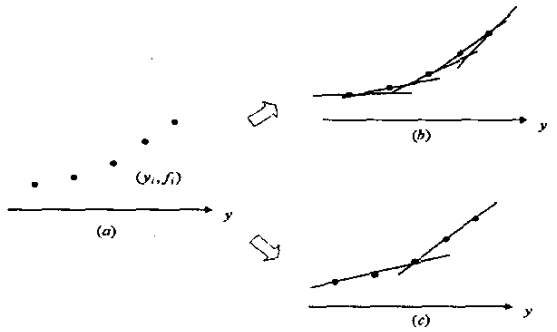

Figure 4. PWL fitting with fewer planes

maximum of tangential planes defined at every y_i. In other words, the PWL function $\tilde{f}(y) = max_i\ a_i^T y + b_i$ where $a_i^T y + b_i$ represents tangential planes will exactly pass through the original data sets $(y_i, f_i),\ i = 1, \ldots, m$ with no fitting error. Because posynomial function becomes convex after the logarithmic transformation, we can replace the posynomial function by PWL function in the logarithmic variable and functional value space.

The following describes how such sets of planes, or PWL function, can be created for a given data set . The fitting can be cast as a following linear optimization problem [6]

$$\begin{array}{ll} \text{minimize} & \|f - \tilde{f}\|_\infty \\ \text{subject to} & \tilde{f}_j \geq \tilde{f}_i + g_i^T(y_j - y_i), i, j = 1, \ldots, m \\ \text{with variable} & \tilde{f} \in \mathbf{R}^m,\ g_1, \cdots, g_m \in \mathbf{R}^k, \\ \text{for given data} & (y_i, f_i),\ i = 1, \ldots, m, \\ & y_i \in \mathbf{R}^k, f \in \mathbf{R}^m. \end{array} \tag{7}$$

Essentially, for a given (y_i, f_i), we would like to find $\tilde{f}_i$ as close as possible to f_i, but only under the condition that all $\tilde{f}_i$s are interpolated by PWL function. We find m planes that pass through $(y_i, \tilde{f}_i)$ with the slope g_i while minimizing the fitting error denoted by $\|f - \tilde{f}\|_\infty$. Figure 3 illustrates the idea where a PWL function composed of seven planes is fitted to the seven data points.

The resulting PWL function can be recovered by

$$\begin{aligned} \tilde{f}(y)_{,fitted} &= max_{i=1,\ldots,m}(\tilde{f}_i + g_i^T(y - y_i)) \\ &\quad max_{i=1,\ldots,m}(a_i^T y + b_i), \end{aligned} \tag{8}$$

where $a_i = g_i, b_i = \tilde{f}_i - g_i^T y_i$. In terms of original real-domain variable $x = exp(y)$,

$$\tilde{f}(x)_{,fitted} = max_{i=1,\ldots,m} c_i \cdot x_1^{a_{i_1}} \cdot x_2^{a_{i2}} \cdots x_k^{a_{ik}}, \tag{9}$$

where $c_i = exp(b_i)$ and $a_{ik} = k_{th}$ component in $a_i \in \mathbf{R}^k$.

The challenge in this method of fitting is the size of the problem. Since the number of inequalities in (7) grows by m^2, *i.e.*, $O(m^2)$, the problem is impractical when dealing with a large data set ($\geq$ 10,000). In this paper, we present one possible variant with a problem size that grows linearly by m.

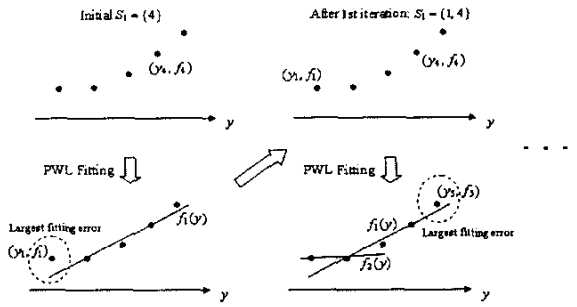

Figure 5. Reduced complexity PWL fitting algorithm

Table 3. Max/mean % model errors in TSMC $0.18-\mu m$ NMOS device in saturation

Model Dependency	Monomial W, L, I_{DS}	PWL W, L, I_{DS}, V_{DS}
$1/g_m$	29.8/10.9	5.4/1.7
g_{ds}	132.7/49.7	39.8/9.4
V_{GS}	11.3/3.5	3.14/0.79
C_{GS}	15.5/5.4	11.7/3.1

The idea is that we usually need significantly less number of planes than m planes that are used in the original method. As illustrated in Figure 4, given five data points Figure 4-(b) is the PWL function fitting with five planes, but it is possible that PWL function with fewer planes can achieve acceptable fitting error as in Figure 4-(c) where we used only two planes.

The algorithm to create such PWL function is illustrated in Figure 5. The method iteratively finds a near-optimal subset of planes. The method begins with a small subset of planes defined as the set $1(S_1)$, and iteratively adds more planes to achieve smaller fitting errors. The planes are added at a point that is responsible for the largest fitting error in each iteration. This reduced complexity algorithm is described as follows.

1. Solve the following problem
   minimize $\|f - \widetilde{f}\|_\infty$
   subject to $\widetilde{f}_j \geq \widetilde{f}_i + g_i^T(y_j - y_i)$,
   $i \in S_1, j = 1, \ldots, m$
   with variable $\widetilde{f} \in \mathbf{R}^n$where n is size of S_1, (10)
   $g_1, \cdots, g_m \in \mathbf{R}^k$.
2. Calculate fitting error and quit if acceptable.
3. Find index i which causes max. fitting error.
4. Add i to set S_1 and go back to step 1.

The algorithm described above is implemented in MATLAB and tested for both active and passive device models. MOSEK [10] is the optimization engine and the fittings are performed on a Xeon 2.8-GHz CPU with 2-GB memory running Linux.

Table 3 is the fitting result for saturated NMOS device in the TSMC 0.18-μm technology. SPICE generated roughly 2000 data points over broad ranges of sizes and bias conditions in order to cover all important physical phenomena such as weak or strong inversion, velocity-saturation, DIBL, etc. Since characteristics of short channel device are affected considerably by the drain-source voltage, the new models are fitted as functions of the drain-source voltage (V_{DS}) in addition to the width (W), length (L) and drain current (I_{DS}). Table 3 shows significant improvements in PWL modeling over monomial based 3-variable (W, L, and I_{DS}) modeling. In particular, PWL modeling achieves average fitting errors less than 5% except g_{ds}. Note that the fitting error in BSIM3v3 model itself is on the order of $3-5\%$[2] for I-V characteristic and much higher for g_{ds}. Hence, the modeling accuracy of PWL fitting is reasonable supposing additional process variations.

Table 4. Max/mean % model errors of on-chip inductance in TSMC $0.13-\mu m$ technology

Model	Monomial	PWL
$1/L$	16.7/4.2	4.03/1.09
$1/Q$	41.0/12.6	22.1/8.53

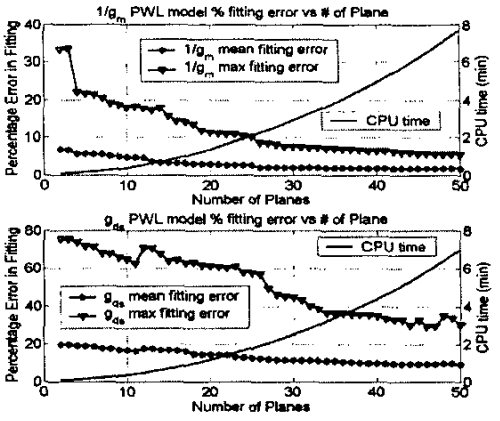

Figure 6. Fitting errors vs. # of planes in reduced-complexity algorithm

Table 4 shows the improvements in the modeling errors in on-chip spiral inductor model in the TSMC 0.13-μm technology. ASITIC [11] generates the data used in the fitting and models are fitted as functions of d_{out} (outer diameter), w (turn width), s (turn spacing), n (number of turns) and f (frequency). Again, significantly better accuracy is observed.

Figure 6 shows the decrease in fitting error and the increase in the computation time with the increasing number of planes for the reduced-complexity method. From the two parameters shown and other fittings we studied, approximately 50 planes are enough in most cases in order to achieve the near-optimal result with reasonable computational effort.

Finally, we point out that PWL constraints are equivalent

[2]I-V characteristic of BSIM3 model for TSMC 0.18-μm mixed-signal model shows mean/max fitting error of about 3%-5%.

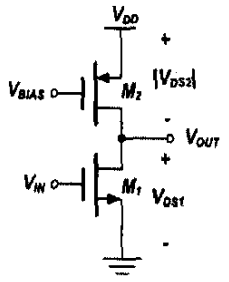

Figure 7. Simple common-source amplifie

to a set of linear inequalities, thus are readily handled in GP. The details are described in the Appendix

4. Bias constraints as posynomial inequalities

As mentioned in section 2, bias estimation errors can be critical in determining circuit performance. One source of bias estimation error is the incomplete bias description in GP.

The difficulty in formulating the bias condition can be illustrated in the example shown in Figure 7. Bias conditions are often equalities. For instance, one of the bias constraints for Figure 7 is

$$V_{DS1} + |V_{DS2}| = V_{DD}, \tag{11}$$

which is a *posynomial equality* given that V_{DS1} and $|V_{DS2}|$ are design variables. In general, posynomial equality is a non-convex constraint therefore not compatible with GP. Here we provide a simple but useful method that can enable posynomial equality in many restricted cases.

The technique we propose is first to relax the constraint (11) as a posynomial inequality

$$V_{DS1} + |V_{DS2}| \leq V_{DD}, \tag{12}$$

and ensure that (12) is active when the problem is solved. A simple method is to exploit the monotonicity inherent in the problem [6]. For instance, consider the following GP description of gain maximization problem in the amplifier in Figure 7.

$$\begin{aligned}
\text{minimize} \quad & 1/g_{m1} \cdot (g_{ds1} + g_{ds2}) \text{ (= 1 / gain)} && (13)\\
\text{subject to} \quad & V_{DS1} + |V_{DS2}| \leq V_{DD}, && (14)\\
& (V_{DSAT1} + V_{OUT,min}) \cdot V_{DS1}^{-1} \leq 1, && (15)\\
1/g_{m1} \quad = \quad & max_i c_i \cdot W_1^{a_{i1}} \cdot L_1^{a_{i2}} \cdot I_{DS1}^{a_{i3}} \cdot V_{DS1}^{a_{i4}} && (16)\\
& \ldots
\end{aligned}$$

For simplicity, we only consider $1/g_{m1}$ as our PWL model which is described as (16), but the same argument can be applied to other models such as g_{ds1}. Equation (14) becomes always active as long as other inequalities and objective values such as (13) and (15) improve or do not degrade as V_{DS1} or $|V_{DS2}|$ grow. More specifically, GP-optimizer wants to minimize the objective value (13) thus tries to push $1/g_{m1}$ as small as possible. Provided that $1/g_{m1}$ monotonically decreases as V_{DS1}, *i.e.* $a_{i4} \leq 0$, GP-optimizer pushes V_{DS1} as large as possible. We then restrict (14) to be the only inequality in the problem that limits the increase of V_{DS1}, hence (14) becomes always active at the optimum. This idea can be easily extended to activate more general KVL "equalities". More examples are discussed in (24), with the two-stage opamp problem.

Note that this formulation implies that we must constrain the values of the exponents of the fitted model. In this particular case, exponents of V_{DS1} in g_{ds1} , $1/g_{m1}$ and V_{DSAT1} have to be nonpositive. From the designs we studied, the degradation in model fitting due to this exponent limitation is negligible.

5. Robust optimization over modeling error

Previous sections explored the methods to reduce the prediction errors by having accurate device model and better problem formulation. In select cases, there are device parameters (most notably g_{ds}) whose modeling errors are relatively large even in PWL fitting. Also, in analog circuit design problems, there are unavoidable cases where monomials must be used for the equalities. We propose to cope with these errors by expressing the problem based on the idea of robust design [2]. The following gives two examples.

First, consider the small-signal gain constraint in (5) and suppose $1/g_m$ and g_{ds} have a maximum modeling error (%) of α and β respectively. We can include this uncertainty as (17) which retains the posynomial inequality

$$A_{min} \cdot (1+\alpha) \cdot 1/g_m \cdot (1+\beta) \cdot g_{ds} \leq 1. \tag{17}$$

Similar method can also apply to the bias estimation error. As will be seen in section 5, current-mirroring devices should have equal gate overdrive voltages

$$V_{OV1}/V_{OV2} = 1. \tag{18}$$

With the maximum % modeling error of α in V_{OV}, (18) can be modified to

$$V_{OV1}/V_{OV2} = \gamma. \tag{19}$$

where $\gamma \in [\frac{1-\alpha}{1+\alpha}, \frac{1+\alpha}{1-\alpha}]$.

We then simultaneously solve several sets of the problem that take the two extreme cases in (19) and one nominal case in (18). The solution guarantees that performance specifications are satisfied within the range of the modeling errors. Interestingly, this method can result in more robust design over the process variations because process variations can be considered as the uncertainty in the device model.

It is however noteworthy that this technique results in a bigger problem size, and potentially causes over-design. The optimum is some (often slight) distance away from the true optimum without modeling errors. To avoid significant over-design, the strategy should be used judiciously for specifications that are more sensitive to modeling errors such as D.C gain specification. By using this method, modeling errors are dealt with in a more predictable way.

6. Design examples and results

Previous sections have investigated several error-reduction methods in GP-based circuit optimization. This section applies the presented methods to the design of two-stage opamp and on-chip spiral inductor.

6.1. Two-stage opamp design

The two-stage op-amp design in Figure 1 is the test vehicle in [2] and is revisited here. Using the proposed error reduction techniques, constraints related to bias description and D.C. gain are rewritten while some of the small-signal specifications such as phase margin constraints are reused. As pointed out earlier, the design parameters such as V_{DSAT}, V_{GS}, g_{ds} and $1/g_m$ are fitted as functions of W, L, I_{DS}, and V_{DS}. Due to the space limitation, only parts of the GP descriptions are shown.

A. Biasing and voltage swing.

To keep the devices in saturation, we specify

$$V_{DS}^{-1} \cdot (V_{DSAT} + \Delta V_{DSAT,min}) \leq 1, \quad (20)$$

where $\Delta V_{DSAT,min}$ is the predetermined margin in V_{DS} to avoid operating in the linear region. We used $\Delta V_{DSAT,min} = 50mV$ in this optimization. Since V_{DS} is one of the design variables, (20) is a posynomial inequality provided that V_{DSAT} is a posynomial or PWL function. We employ PWL model for V_{DSAT}. Diode-connected devices (M_8,M_3, and M_4) have an additional constraint

$$V_{GS}/V_{DS} = 1, \quad (21)$$

which is a monomial equality when a monomial model of V_{GS} is used.

At the output, the voltage swing specifications are applied to M_6 and M_7 as

$$V_{OUT,min}^{-1} \cdot (V_{DSAT6} + \Delta V_{DSAT,min}) \leq 1, \quad (22)$$

$$(V_{DD} - V_{OUT,max})^{-1} \cdot (V_{DSAT7} + \Delta V_{DSAT,min}) \leq 1, \quad (23)$$

where $V_{OUT,min}$ and $V_{OUT,max}$ are given minimum and the maximum output voltages, respectively. Inequalities (22) and (23) are posynomial inequalities because we employ PWL model for V_{DSAT}.

B. KCL,KVL and circuit topology

The drain-source voltages in transistors should satisfy KVLs given by the circuit topology. This requires the following three equalities

$$\begin{aligned} (|V_{DS5}| + |V_{GS1}|)/(V_{DD} - V_{in,cm}) &= 1, \\ (V_{DS3} + |V_{DS1}| + |V_{DS5}|)/V_{DD} &= 1, \\ (V_{DS6} + |V_{DS7}|)/V_{DD} &= 1, \end{aligned} \quad (24)$$

where $V_{in,cm}$ is the common-mode voltage at the gate of M_1. All of the equalities in (24) are written as posynomial inequalities and activated by utilizing monotonicity as explained in section 4. We use a PWL model for $|V_{GS1}|$.

Table 5. GP-prediction and SPICE simulation for both PWL and monomial model-based optimizations

Performance Measure	Spec.	GP-PWL	SPICE-PWL	GP-MON	SPICE-MON
Output swing [V]	≥ 1.4	1.4	1.43	1.46	1.54
Quiescent Power [mW]	≤ 0.2	0.2	0.2	0.2	0.22
Open-loop gain [dB]	≥ 70	73.78	70.3	70.0	55.56
GB product [MHz]	Max	74.00	66.9	109.6	82.8
Phase-Margin [deg]	≥ 60	60	66.48	60	69.2

We specify KCL and current mirrors as monomial equalities, *i.e.*,

$$I_{DS5} = 2 \cdot I_{DS1\sim4}, I_{DS6} = I_{DS7}, \quad (25)$$

$$V_{OV8} = V_{OV5} = V_{OV7}, \quad (26)$$

where overdrive voltage, V_{OV}, is a monomial.

The connection between the 1st and 2nd stages translates into the following monomial equality

$$V_{DS4} = V_{GS6}, \quad (27)$$

where monomial V_{GS6} model is used.

C. Gain specification

Since PWL model of g_{ds} has relatively large modeling error, we use the robust optimization technique described in section 4.3 to describe the gain specification, *i.e.*,

$$A_{min}(1+\alpha_p) \cdot 1/g_{m1} \cdot ((1+\beta_p)g_{ds2} + (1+\beta_n)g_{ds4}) \cdot (1+\alpha_n) \cdot 1/g_{m6} \cdot ((1+\beta_p)1/g_{ds7} + (1+\beta_n)g_{ds6}) \leq 1,$$

where α_p,α_n,β_p, and β_n are maximum modeling percentage error of $1/g_m$ and g_{ds} respectively (the subscripts p and n denote PMOS and NMOS), and A_{min} is the minimum specified gain. We employ PWL models for $1/g_m$ and g_{ds}.

Proposed GP descriptions are combined with other design constraints such as matching, phase margin, and power consumption previously shown in [2], and optimizations are carried out such that gain-bandwidth (GB) product is maximized. In order to evaluate the amount of error reduction, we conducted two optimization-simulation scenarios as shown in Table 5.

In Table 5, The GP-PWL refers to the result from a GP optimization using PWL models and new description techniques. The SPICE-PWL is the SPICE simulation based on GP-PWL predicted variables. To compare with prediction errors, GP-MON is the GP-optimization that uses the published GP description in [2] and monomial device models. SPICE-MON is the corresponding SPICE simulation. Note that all of the specifications are met in SPICE-PWL while there is a 15dB violation of gain specification in the SPICE-MON case.

Figure 8 illustrates the GP-prediction and SPICE simulation

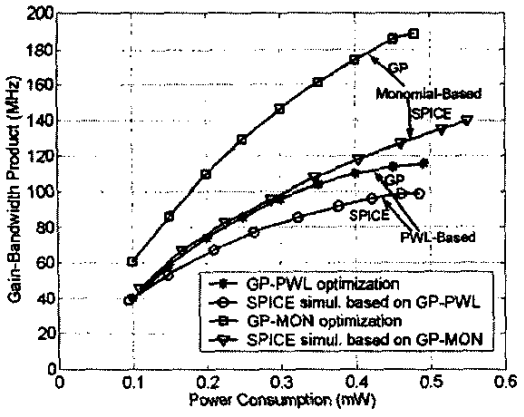

Figure 8. Optimal GB product from GP and SPICE

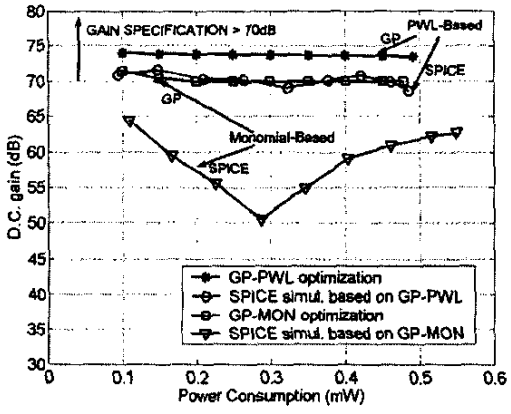

Figure 9. D.C. gain from GP and SPICE

discrepancy both in GP-PWL and GP-MON cases over different DC power constraints ranging from 0.1mW to 0.5mW. Clearly, PWL-based scenario achieves significantly better accuracy of gain-bandwidth product prediction. Interestingly, GP-MON and the corresponding SPICE simulation have *larger* GB-product than the GP-PWL counterpart. However, Figure 9 reveals that the higher GB-product in GP-MON is at the cost of significantly violating the D.C. gain specification.

6.2. On-chip inductor design

A second example uses an integrated inductor as the design problem. A common goal is to maximize the quality factor (Q_L) for a given inductance (L_{req}) with a lower bound on the self-resonance frequency (w_{sr}). The design problem can be cast as (28),

$$\begin{aligned} \text{maximize} \quad & Q_{L,min} \\ \text{subject to} \quad & Q_{L,min} \leq Q_L, \\ & L = L_{req}, w_{sr} \geq w_{sr,min}. \end{aligned} \tag{28}$$

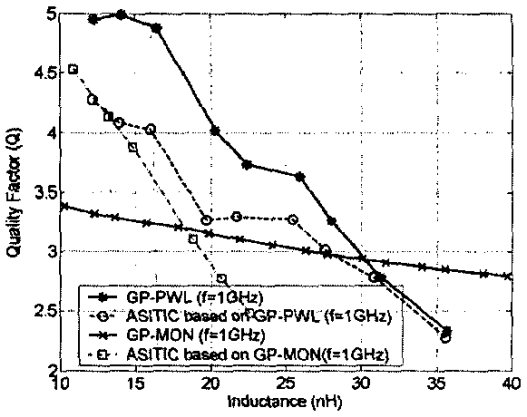

Figure 10. Optimal Q_L vs. inductance L

We created new PWL model of $1/Q_L$, $1/L$, and $1/w_{sr}$ as a function of d_{out} (outer diameter), w (turn width), s (turn spacing), n (number of turns) and f (frequency). Note this extends the models in [12] by including the frequency dependency. The problem, (28), can be rewritten as follows

$$\begin{aligned} \text{minimize} \quad & Q_{L,min}^{-1} \\ \text{subject to} \quad & Q_{L,min} \cdot 1/Q_L \leq 1, \\ & L_{req} \cdot 1/L \leq 1, \\ & w_{sr,min} \cdot 1/w_{sr} \leq 1. \end{aligned} \tag{29}$$

Because we use PWL inductance model, we must impose the inequality to replace $L = L_{req}$. Since the optimizer will try to find the smallest possible inductance to maximize the quality factor, L is driven to the lower bound, L_{req}, and the inequality is therefore active when the problem (29) is solved.

In Figure 10, we show the GP-prediction and ASITIC simulation of the maximum quality factor versus inductance at $f = 1GHz$. Again, significantly improved prediction accuracy is observed in the GP that utilizes the PWL model.

7. Conclusion

This paper illustrates several techniques to reduce errors in GP-based analog circuit optimization. The contributions of this paper are summarized as follows.

First, an improvement in the device modeling for GP-based analog design optimization is reported. This paper presents an efficient method to create GP-compatible device models and it is demonstrated that this method is capable of creating accurate device models in today's deep sub-micron technology.

Second, several improvements to the circuit design formulation in GP are described. It is shown that bias-related non-convex constraints can be enabled by exploiting monotonicity, which reduces the bias estimation error. Also, it is shown that simple approach that takes the modeling error into account can result in a robust optimization over the inherent modeling error.

Presented ideas are verified by optimizing a 2-stage opamp

and an on-chip inductor. The results are compared with previously published techniques and show significantly improved matching with SPICE simulations.

8. Appendix

PWL inequality is equivalent to a set of linear inequalities, thus readily handled in GP. For instance, suppose we've created PWL model for g_{ds} as

$$g_{ds} = max_{i=1,\ldots,m}(c_i \cdot W^{\alpha_{i1}} \cdot L^{\alpha_{i2}} \cdot I_{DS}^{\alpha_{i3}} \cdot V_{DS}^{\alpha_{i4}}). \quad (30)$$

Then (5) can be written as

$$A_{min} \cdot 1/g_m \cdot (max_i c_i \cdot W^{\alpha_{i1}} \cdot L^{\alpha_{i2}} \cdot I_{DS}^{\alpha_{i3}} \cdot V_{DS}^{\alpha_{i4}}) \leq 1. \quad (31)$$

By introducing slack variable t, we can rewrite (31) as a following $m+1$ equivalent inequalities

$$A_{min} \cdot 1/g_m \cdot t \leq 1 \quad (32)$$

$$c_i \cdot W^{\alpha_{i1}} \cdot L^{\alpha_{i2}} \cdot I_{DS}^{\alpha_{i3}} \cdot V_{DS}^{\alpha_{i4}} \leq t,\ i = 1,\ldots m, \quad (33)$$

which is still GP-compatible inequalities [6]. Also, it's noteworthy to point out that we can't use equalities for PWL functions just as posynomial functions [6].

9. References

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