# Multiphase Voltage-Mode Hysteretic Controlled DC–DC Converter With Novel Current Sharing

Jaber Abu-Qahouq, *Member, IEEE*, Hong Mao, and Issa Batarseh, *Senior Member, IEEE*

***Abstract*—Today's on-board high-density, low-output-voltage, high-output-current, fast transient point-of-load (POL) dc–dc converters design requirements for the new generation of integrated circuits, digital signal processors, and microprocessors are increasingly becoming stricter than ever. This is due to the demand for high dynamic performance dc–dc conversion with tight dynamic tolerances for supply voltages coupled with very high power density. In this paper, a multiphase voltage-mode hysteretic controlled POL dc–dc converter with new current sharing is presented. Theoretical analysis is provided for multiphase and interleaved dc–dc converters with new current sharing method. The simulation and experimental results are compared based on a specific design example.**

***Index Terms*—converter, current sharing, dc–dc, fast transient, high-density, high-output-current, hysteretic, integrated circuit (IC), interleaving, low-output-voltage, multiphase, point-of-load (POL), voltage regulator module (VRM).**

## I. Introduction

POINT-OF-LOAD (POL) dc–dc converters and voltage regulator modules (VRMs) for the next generation of integrated circuits (ICs) for microprocessors and communication systems are required to have many strict and challenging specifications that include high power and current densities, high current capability, low output voltage deviation in both steady-state and transient conditions, small size, light weight, and high efficiency [1]–[3], [8], [9], [11]. All such requirements must be achieved at very low output voltage that is expected to drop below 1 V in the next few years, below 0.6 V by 2010, and below 0.4 V by 2016 [3].

Both the interleaving (multiphase) and the single-phase voltage-mode hysteretic control techniques can reduce the output voltage ripple. However, the overshoot and undershoot requirements during large magnitude transients still have to be investigated. It is known that to obtain low output overshoot, the multiphase VRMs require the design of high-performance feedback control that can also provide current sharing [1], [4], [5]. Hence, even though the interleaving technique reduces the output voltage ripple and helps in achieving faster current transient response, a careful control design and/or increase in the output capacitance size will be needed in order to satisfy the maximum overshoot and undershoot limits during large load transients.

In the single-phase hysteretic voltage-mode control technique, the hysteretic window can be set to a certain level such that the controller will respond quickly to load transients and correct the voltage before deviating from the maximum allowed overshoot and undershoot. Even though the output capacitor size still plays an important role here, its size is significantly reduced because of the hysteretic control.

On one hand, voltage-mode hysteretic control has many advantages over many other control techniques that include simplicity, no feedback loop compensation is needed, near instantaneous response to load transients, and no limitations on the switches ON time. On the other hand, the interleaving technique has several advantages such as the high frequency output voltage ripple with lower switching frequency, ripple cancellation, current division (sharing) between the phases which allows higher current carrying capability, and also fast transient response which is limited by the feedback control loop. From this, it is clear that combining the voltage-mode hysteretic control technique with the interleaving technique will result in a VRM that has the advantages of both techniques [6], [7], [10].

However, multiphase converters are required to have high performance current sharing functionality in order to keep almost equal division of the load current between the phases at all load conditions in addition to the voltage regulation [1], [4]–[6].

In this paper, a multiphase voltage-mode hysteretic controlled dc–dc converter or POL with current sharing is presented with theoretical and experimental verification. In the next section, the multiphase voltage-mode hysteretic control method is discussed. Section III presents the concept of the proposed current sharing method and how it is applied to a two-phase interleaved voltage-mode hysteretic controlled dc–dc converter. In Section IV, the proposed method is generalized for $N$ interleaved phases. The theoretical analysis with key design equations is discussed in Section V. The simulation and experimental results are given in Sections VI and VII. Finally, the conclusion is given in Section VIII.

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J. Abu-Qahouq and I. Batarseh are with the Electrical and Computer Engineering Department, University of Central Florida, Orlando, FL 32816 USA (e-mail: batarseh@mail.ucf.edu).

H. Mao is with Astec Power, Andover, MA 01810 USA.

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## II. Multiphase Voltage-Mode Hysteretic Control

When applying the hysteretic voltage-mode control to interleaved buck converters, one must note that

1) the derived control signal from the output ripple (hysteretic control) must be frequency divided while keeping the same control-signal ON-time (interleaving);

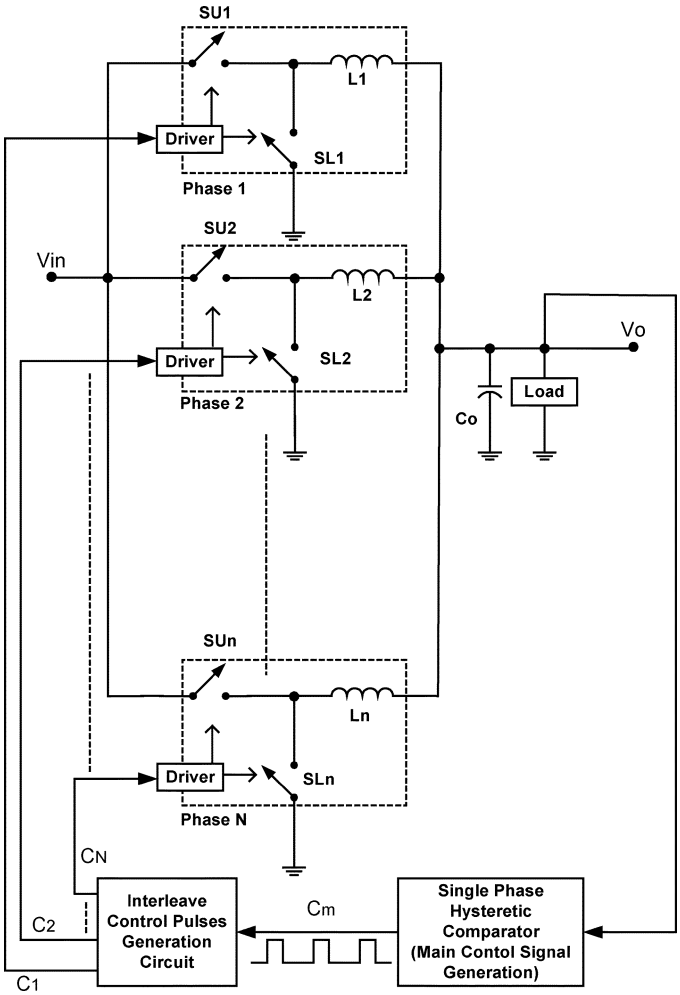


Fig. 1. Block diagram of N interleaved buck converters with voltage-mode hysteretic control.

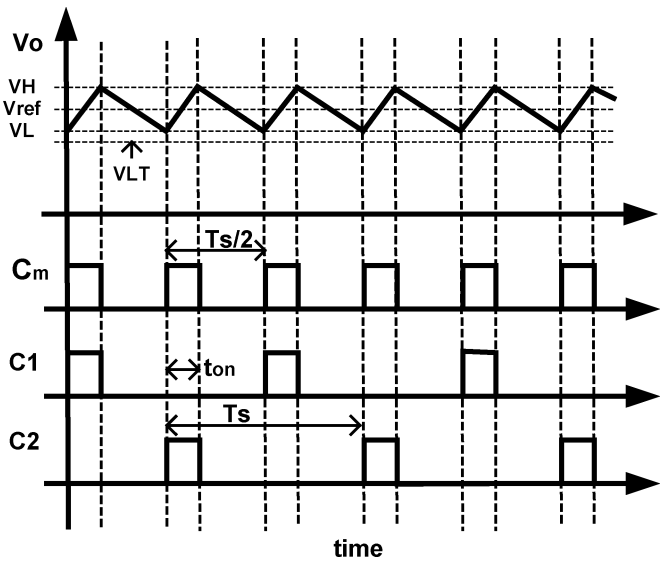


Fig. 2. Example of control signals for two interleaved phases $(\mathrm{N} = 2)$.

2) during transients, multiphase control operation must be disabled so that all the phases' switches will switch ON and OFF at the same time.

The first note is to keep the switching frequency low for the same output voltage ripple so that the interleaving can be achieved, whereas, the second note is to achieve faster transient response and synchronization between the phases during transients.

Fig. 1 shows the basic block diagram of N interleaved synchronous buck phases with voltage-mode hysteretic control, while Fig. 2 shows the example of control signals for two interleaved phases $(\mathrm{N} = 2)$ for illustration purposes. It must be noted that the voltage waveform $V_o$ of Fig. 2 is true only when the voltage ripples across the output capacitor and its equivalent series inductance (ESL) are zero.

The main control signal $(C_m)$ is generated by comparing the output voltage to a minimum value $(V_L)$ and a maximum value $(V_H)$, forming a hysteretic window. Then, the generated pulses are distributed between the phases interchangeably so that one phase high-side switch is ON at a time whereas all the other switches are OFF at that time. This will generate the required multiphase control-signals $C_1, C_2, \ldots, C_N$.

At transients, another comparator with threshold of $V_{\mathrm{LT}} < V_L$ turns ON all the high-side switches [metal oxide semiconductor field effect transistors (MOSFETS)] and turns OFF all the low-side switches at low-to-high load transients (which cause voltage undershoot). This new threshold $(V_{\mathrm{LT}})$ is added to make the transient response faster and maintain equal current sharing even at transients, otherwise, if this threshold is not added, only one phase switch will be turned ON at low-to-high load transients when $V_o < V_L$, resulting in slower transient response. However, at high-to-low load transients (which cause voltage overshoot), all the high-side switches are turned OFF by the hysteretic comparator without the need of another comparator with another threshold larger than $V_H$.

Fig. 3 shows how the multiphase control signals can be generated from the main control signal using discrete components for two and four phases along with their corresponding waveforms.

## III. Multiphase Voltage-Mode Hysteretic Control With Current Sharing

It is very important that the current be distributed almost equally between the interleaved phases in the multiphase converter. Unfortunately, components, connections and layout differences from phase-to-phase to the load and other nonidealities may cause the current distribution (sharing) to be unequal, especially at large load transients [1], [4]. Hence, current sharing functionality is necessary for the multiphase voltage-mode hysteretic control described in the previous section.

Current sharing between the interleaved converters is usually achieved by controlling the ON-time of each converter phase, such that the ON-time of the phase that carry larger current from the other phases is smaller than the ON-time of the other phases, and the phase that carries the smallest current has the largest ON-time, i.e., the current sharing regulation is performed by shortening (changing) the ON period of phases switches [1], [4], [5]. In this case, the current sharing function is dependent on the control method being used in the voltage regulation. These current sharing methods require some kind of reference to achieve current sharing. Moreover, the current sharing functionality in addition to the control loop adds complexity to the closed loop design (current control loop with compensation

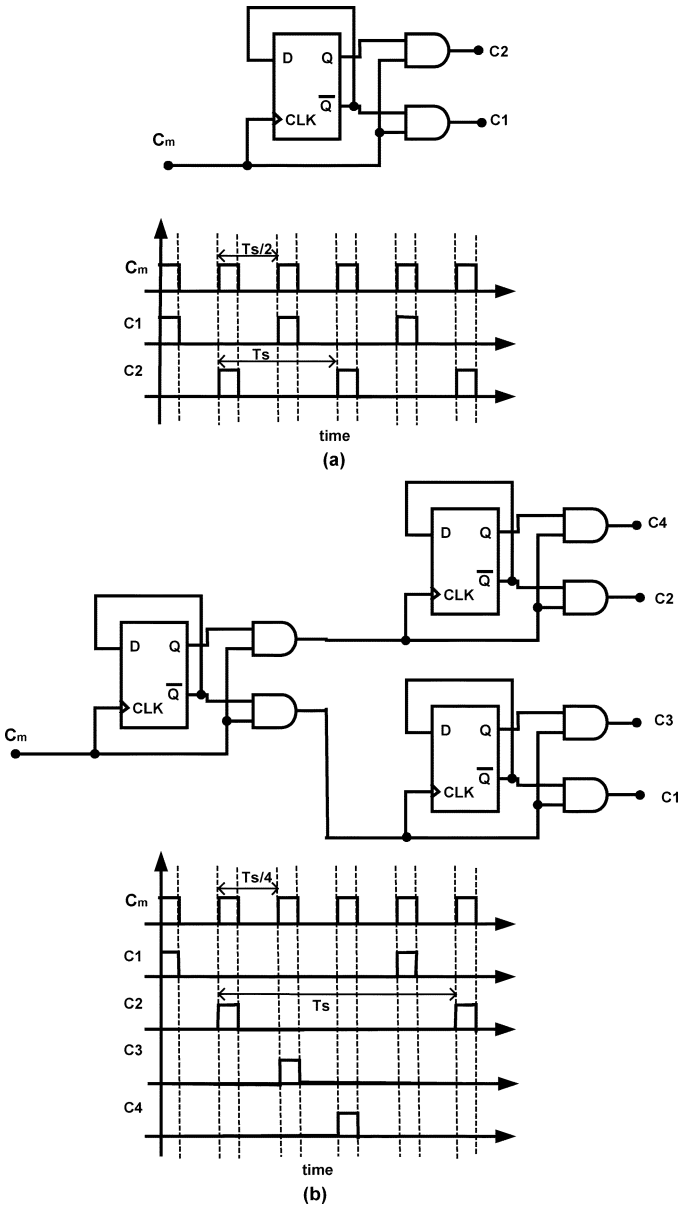


Fig. 3. Multiphase logic circuits to generate multiphase control signals: (a) two phase and (b) four phase.

is needed). Moreover, the ON-time of the switches in the voltage-mode hysteretic control is directly derived from the output voltage ripple by toggling the switches OFF and ON as the output voltage hits the upper and lower limits of the hysteretic comparator (comparator hysteretic window). Hence, changing the ON time of a phase switch means changing the hysteretic window if another switch is not directly turned ON. If another switch is directly turned ON, this may cause several turn ONs within one comparator switching period, causing higher switching frequency for each phase.

Fig. 4 shows the basic block diagram of the proposed current sharing method. In this method, the instantaneous currents in each phase are sensed $(I_1, I_2, \ldots, I_N)$ and each compared relative to the other phases instantaneous currents generating a comparison digital code $(D_1, D_2, \ldots, D_N)$, without the need for a reference, to find the phase that carries the smallest current. When the main regulation control loop that has no current sharing functionality decides that it is the time to turn ON a switch, the high-side switch in the buck converter for example, to deliver energy to the converter output, the phase that carries the smallest current at that time will be turned ON by producing a turn ON rising edge signal $(C_{Main})$, while the other phases are turned OFF by producing the final control signals $(C_1, C_2, \ldots, C_N)$. In simple terms, only one switch will be turned ON at a given time and this switch will be chosen by monitoring which phase is carrying the smallest instantaneous current at the instant when a switch needed to be turned ON.

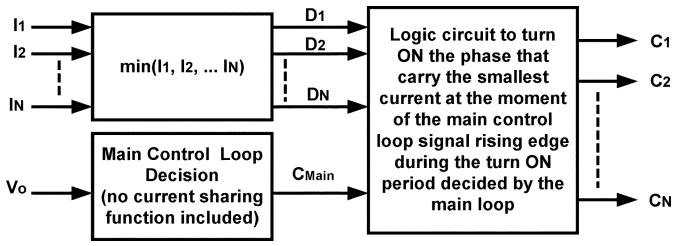


Fig. 4. Basic block diagram of the proposed current sharing method.

It must be noted that even though the instantaneous current in each phase is being compared relative to the other phases continuously, the decision of this comparison is taking effect only at the rising edge of the main control signal $C_{\rm Main}$, turning ON the appropriate phase. Hence, the instantaneous point value of each phase current, just before turning ON a phase switch, is the only value that will affect the current sharing process. Fig. 5 shows the current sharing part for two-phase buck dc–dc converter as an example.

The instantaneous currents can be sensed by several methods. For example, it can be sensed by the conventional method directly through the inductors, by placing a small series resistor with the inductors. Unfortunately, even though this sensing method is simple and relatively accurate, it degrades the efficiency due to the loss in the current sense resistor especially in the high current applications. Another way to sense the instantaneous current is done by sensing the voltage across the low-side switches (at the switches junctions). This is possible because

1) the instantaneous current information for a buck converter is available while the low-side switch is ON and the high-side one is OFF;
2) the instantaneous current information just before turning ON one high-side switch is what required for the current sharing process of the proposed method;
3) before turning ON one high-side switch, all the low-side switches will be ON and hence the current information is available.

The above proposed current sharing can be applied to the multiphase voltage-mode hysteretic control of the previous section, resulting in a new controller. Fig. 6 shows the basic controller diagram for the multiphase voltage mode hysteretic controller with the proposed current sharing, while Fig. 7 shows general waveforms sample for the current sharing process in steady and symmetric condition. The basic operation of the circuit shown in Fig. 6 with its related waveforms in Fig. 7 can be summarized as follows: The main control signal $(C_{\rm Main})$ is generated by comparing the output voltage to a minimum value $(V_L)$ and

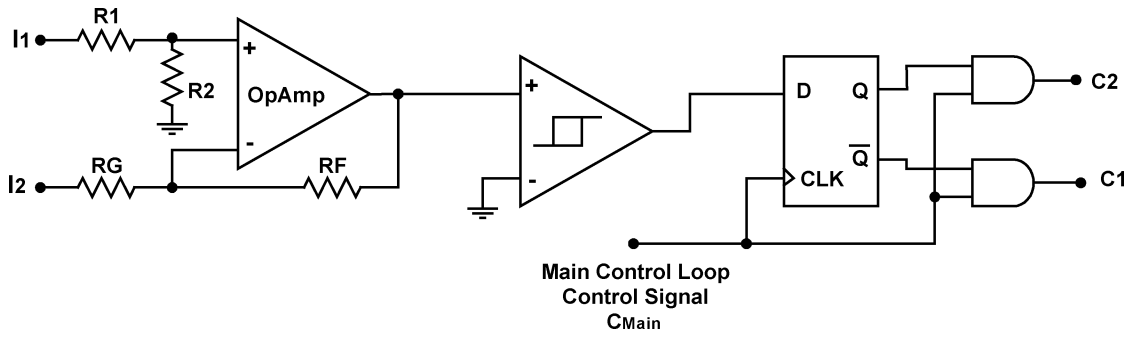


Fig. 5. Current sharing part for two-phase buck dc–dc converter.

a maximum value $(V_H)$ around a reference voltage $(V_{\rm ref})$ using the hysteretic comparator Comp2. When the time comes to turn ON one high-side switch when the output voltage hits the limit $V_L$, the rising edge of the turn ON signal of $C_{\rm Main}$ which is used as a clock for a D-type flip flop cause the current sharing decision of Comp1 to be activated, turning ON the phase that carries the smallest current at that time. Comp3 has a lower limit $V_{\rm LT} < V_L$. This comparator output is logic zero (low) during the steady state operation when $V_o > V_{\rm LT}$, and logic one (high) during startup and during the low to high load transients when $V_o < V_{\rm LT}$, which cause the phases to switch together (no interleaving) during these transients. This process will generate the require phases' control signals $C_1$ and $C_2$ to achieve voltage regulation with current sharing.

## IV. Method Generalization for N Interleaved Phases

Fig. 8 shows the basic controller generalized diagram for N multiphase voltage-mode hysteretic controlled current-shared converters. In Fig. 8, only one of the outputs $D_1, D_2, \ldots, D_N$ of the current comparison circuit can be logic high at a time, causing the phase that carries the smallest instantaneous current to be turned ON at the rising edge of the voltage mode loop as described in the previous section for the two-phases case.

Fig. 9 shows one possible arrangement for the current sharing circuit by using a set of comparators to find the phase that carries the smallest current for N interleaved phases. The logic circuit after the comparators generate signals $D_1, D_2, \ldots, D_N$ from the comparators outputs $X_1, X_2, \ldots, X_m$, so that one of the D-type flip-flops can be logic high at a time. If this arrangement is to be used, the required number of comparators (m) for N interleaved phases is

$$m = \frac{N(N-1)}{2}. \tag{1}$$

Fig. 9 also shows that the main control signal from the voltage loop $(C_{\rm Main})$ can be from any type of controller and not limited to the voltage-mode hysteretic control.

## V. Theoretical Analysis

In this section, multiphase voltage-mode hysteretic controlled buck converter is analyzed and the frequency equation is derived. It is assumed during this analysis, that the converter is in steady-state operation, and all components are ideal except the following nonidealities: output capacitor has equivalent series resistance (ESR) and equivalent series inductance (ESL), the switches have ON resistance, and the inductor and its traces also have resistance. In addition, it is assumed that the input voltage is constant with no ripple and the control loop has finite delay time.

Fig. 10 shows the voltage across the output capacitor in steady-state considering the ESR and the ESL of the output capacitor. In steady-state, the voltage ripple across the output capacitor considering the ESR and the ESL, is given by

$$v_{\rm ripple}(t) = v_C(t) + v_{\rm ESR}(t) + v_{\rm ESL}(t) \tag{2}$$

where

- $v_{\rm ripple}(t)$ output voltage ripple across the output capacitor as shown in Fig. 10;
- $v_C(t)$ voltage across the ideal output capacitor;
- $v_{\rm ESR}(t)$ voltage across the output capacitor ESR;
- $v_{\rm ESL}(t)$ voltage across the output capacitor ESL.

There are two modes of operation in steady-state. During Mode 1, when one of the high-side switches is ON, (2) becomes

$$\begin{aligned} v_{\rm ripple\_ON}(t) = &\left(\frac{\Delta I \times t^2}{2 \times C_O \times D \times T_S} - \frac{\Delta I \times t}{2 \times C_O}\right) \\ &+ \left(ESR \times \left(\frac{\Delta I \times t}{D \times T_S} - \frac{\Delta I}{2}\right)\right) \\ &+ \left(ESL \times \frac{\Delta I}{D \times T_S}\right) \quad t_0 \le t \le DT_S. \end{aligned} \tag{3}$$

During Mode 2 when all high-side switches are OFF, (2) is given by

$$\begin{aligned} v_{ripple\_OFF}(t) = &\left(-\frac{\Delta I \times t^2}{2 \times C_O \times (1-D) \times T_S} + \frac{\Delta I \times t}{2 \times C_O}\right) \\ &+ \left(ESR \times \left(\frac{\Delta I}{2} - \frac{\Delta I \times t}{(1-D) \times T_S}\right)\right) \\ &+ \left(-\frac{ESL \times \Delta I}{(1-D) \times T_S}\right) \\ &DT_S \le t \le T_S + t_0 \end{aligned} \tag{4}$$

where

- $\Delta I$ total inductor(s) ripple for N phases;
- $T_s$ switching period for N phases;
- $D$ duty cycle defined as the ratio between the ON time of high-side switch and the switching period $T_s$;
- $C_O$ total output capacitance of N phases.

The hysteresis window is then given by

$$Hyst = v_{\rm ripple\_ON}(t_{\rm ON} - t_{\rm del}) - v_{\rm ripple\_OFF}(t_{\rm OFF} - t_{\rm del}) \tag{5}$$

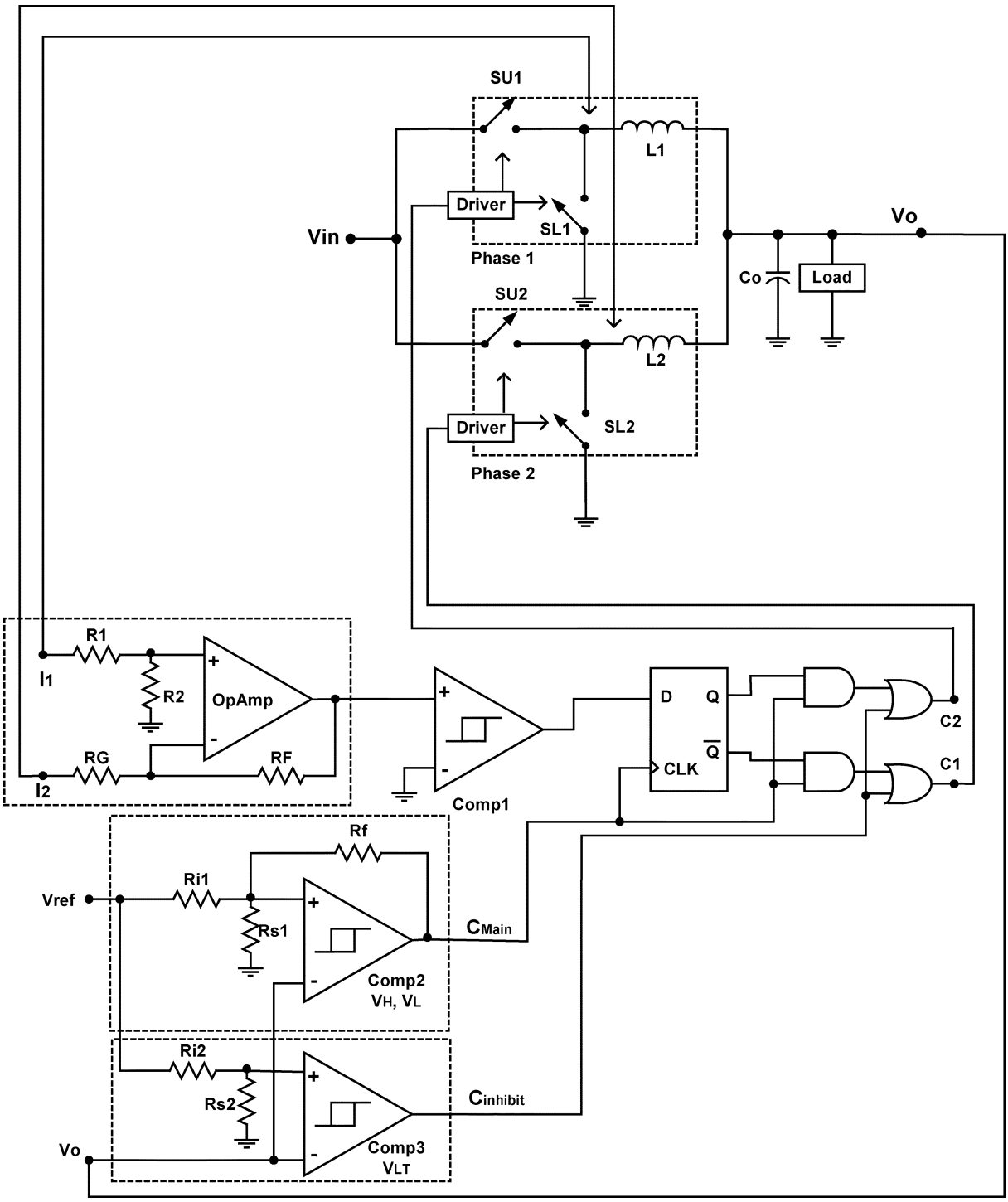


Fig. 6. Proposed control method applied to two-phase converter.

where

$Hyst$ hysteresis window;

$t_{\rm ON}$ time duration when one of the high side switches is ON where $t_{\rm ON} = DT_S$;

$t_{\rm OFF}$ time duration when all the high-side switches are OFF where $t_{\rm OFF} = (1 - D)T_S$;

$t_{\rm del}$ total delay time of the feedback loop from time the voltage hits one of the hysteresis window limits until the time the appropriate switches are actually turned ON and OFF.

Assuming that all the phases are identical and have the same output inductors, the total inductor(s) current ripple of N phases is given by

$$\Delta I = \frac{V_{\rm in} - I_o R_{\rm eq} - NV_O}{L} \times D \times T_S \tag{6}$$

where

$V_{\rm in}$ input voltage;

$V_O$ output voltage;

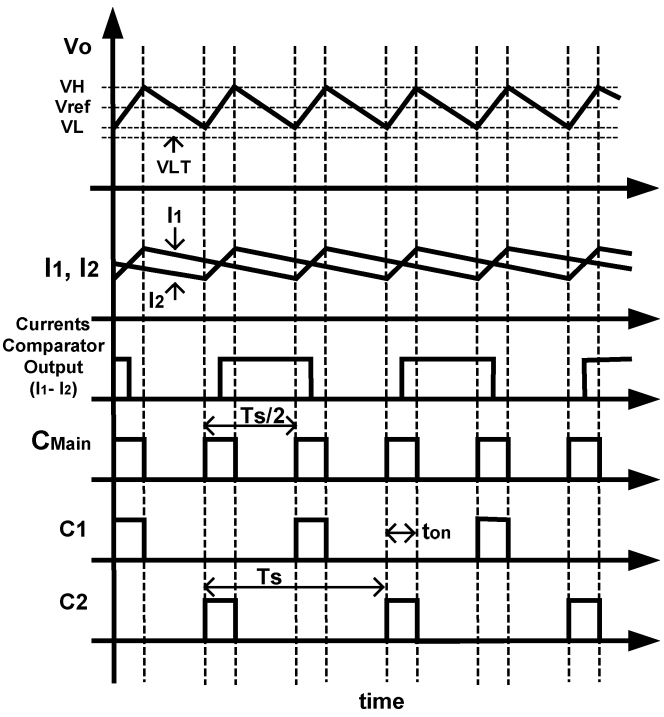


Fig. 7. General waveforms sample for the current sharing process.

$R_{\rm eq}$ total path resistance including the ON resistance of the switch and the inductor resistance;

$L$ output inductor of one phase assuming that all phases have equal output inductors.

and

$$D = \frac{t_{\rm ON}}{T_S} = \frac{V_O + \frac{I_O}{N} R_{\rm eq}}{V_{\rm in}}. \tag{7}$$

By substituting (3) and (4) in (5), and using (6) and (7), the phase switching frequency ($f_S = 1/T_S$) is given by (8), shown at the bottom of the page, where

$$\begin{aligned}
a =& (2 \times N \times V_{\rm in} \times R_{\rm eq} \times ESR \times t_{\rm del} - 2 \times N \times V_{\rm in} \\
&\times R_{\rm eq} \times ESL + 2 \times Hyst \times L \times R_{\rm eq})(C_o) \\
&- N \times V_{\rm in} \times R_{\rm eq} \times (t_{\rm del})^2 \\
b =& N \times (V_{\rm in})^2 - N^2 \times V_{\rm in} \times V_o \\
c =& \left(N^2 \times V_{\rm in} - N \times (V_{\rm in})^2\right)(2 \times V_o \times ESR \times C_o) \\
d =& (2 \times N \times Hyst \times L)(V_o - V_{\rm in}) \\
&+ \left(N \times (V_{\rm in})^2 - N^2 \times V_{\rm in}\right)(2 \times ESL) \\
e =& N \times V_o \times ESR \times C_o + I_o \times R_{\rm eq} \times ESR \times C_o \\
&- N \times V_o \times t_{\rm del} - I_o \times R_{\rm eq} \times t_{\rm del}
\end{aligned}$$

Even though (8) shows that the switching frequency depends on the load current, this dependency is very small since synchronous rectifiers have the same equivalent circuit over the switching period. This will be shown by plotting curves at different loads later in this section. This load current dependency appears since the switches' ON resistances and the inductors resistances have been considered in the mathematical derivation. Moreover, since synchronous rectifiers were used, there is no discontinuous mode of operation even at light loads.

Fig. 11 shows the phase switching frequency $f_S$ versus the input voltage in the case of 1–4 phases being used at no load and full load conditions for the following parameters $V_O = 1.5$ V, $L = 1$ $\mu$H per phase, 2 mF output capacitance with $ESR = 8\,{\rm m}\Omega/3$ and $ESR = 4.8\,{\rm nH}/3$ assuming three paralleled capacitors with a total of 2 mF, $t_{\rm del} = 100$ ns, and $Hyst = 20$ mV for full load $I_o = 50$ A. Fig. 11 shows that the phase switching frequency is decreased with the number of phases increased for the same hysteresis window. Of course, if the switching frequency of each phase for N phases is kept the same as the original switching frequency for one phase converter, the output voltage will have a smaller ripple.

It must be noted that the maximum output voltage for $N$ interleaved phases cannot ideally exceed $1/N$ of the input voltage (assuming $R_{\rm eq} = 0\,\Omega$, i.e., no voltage drop across components and traces) because of the restriction that only one high-side switch can be ON at anytime in steady-state conditions. Therefore, larger minimum input voltage is required when the number of phases increases for the same output voltage. This explains the switching frequency zero crossing of Fig. 11.

Equation (8) denominator has a zero that puts a condition on the maximum value of ESL. For the voltage across the ESL not to exceed the hysteresis window and cause the frequency to be very high and uncontrollable, the following condition must be satisfied:

$$ESL < \frac{a \times Hyst + b \times ESR + c}{2 \times N \times V_{\rm in} \times C_o \times (V_{\rm in} - I_o \times R_{\rm eq} - N \times V_o)} \tag{9}$$

where

$$\begin{aligned}
a =& (2 \times L \times C_o)(N \times V_{\rm in} - I_o \times R_{\rm eq} - N \times V_o) \\
b =& (2 \times N \times V_{\rm in} \times C_o \times t_{\rm del})(V_{\rm in} - I_o \times R_{\rm eq} - N \times V_o). \\
c =& (N \times V_{\rm in} \times (t_{\rm del})^2)(-V_{\rm in} + N \times V_o + I_o \times R_{\rm eq})
\end{aligned}$$

Fig. 12 shows the maximum allowable ESL value versus hysteresis window for 1–4 Phases at no-load condition for the same parameters of Fig. 11, since from (9) the design worst case for ESL is at no load since the maximum allowable ESL decreases as the load decreases. From Fig. 12 it is apparent that the maximum allowable ESL increases as the number of phases increase.

## VI. Simulation Results

Two-phase dc–dc buck converter with the proposed current sharing method and voltage-mode hysteretic control was simulated using Pspice/Orcad software package with the following design parameters $V_{\rm in} = 12$ V, $V_o = 1.5$ V, 50 A full load,

$$f_s = \frac{2V_o(N \times V_o + I_o \times R_{\rm eq} - N \times V_{\rm in})(V_{\rm in} - N \times V_o - I_o \times R_{\rm eq}) \times e}{NV_{\rm in}\,(a \times I_o + b \times (t_{\rm del})^2 + c \times t_{\rm del} + d \times C_o)} \tag{8}$$

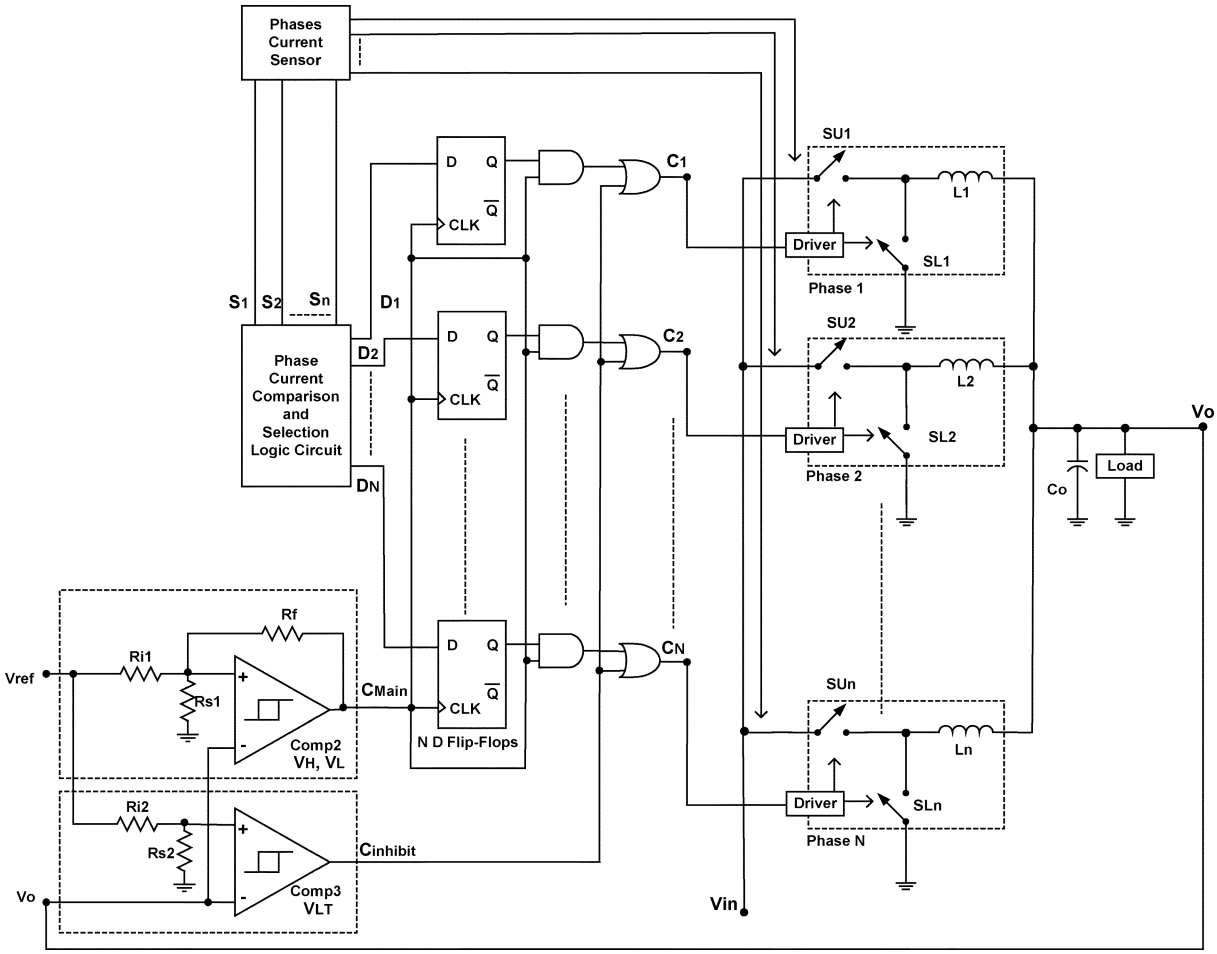


Fig. 8. Basic controller generalized diagram for N multiphase voltage-mode hysteretic controlled current-shared converters.

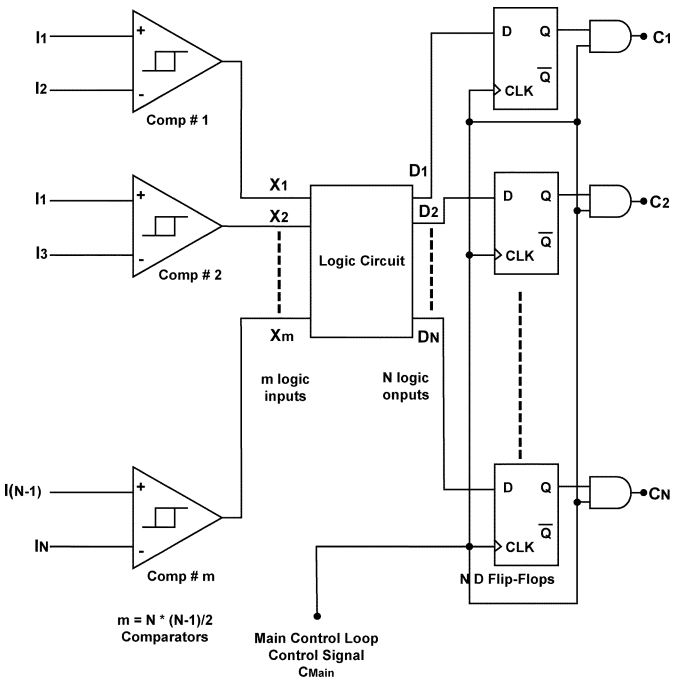


Fig. 9. Possible arrangement for current sharing circuit.

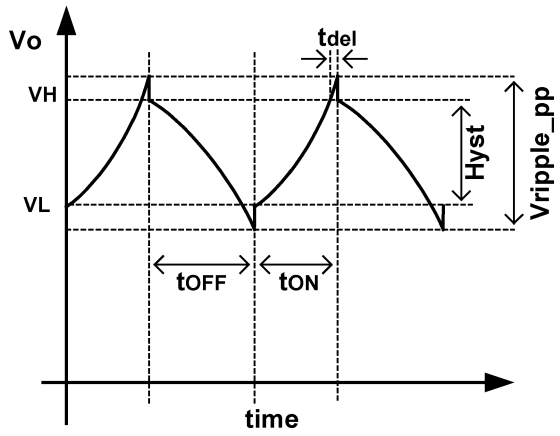


Fig. 10. Output voltage with its ripple when the equivalent series resistance (ESR), the equivalent series inductance (ESL), and feedback loop delay time ($t_{\rm del}$) are considered.

$L_{\rm phase1} = L_{\rm phase2} = 1\,\mu$H, and $C_o = 2$ mF, with a steady-state hysteretic band of $\pm 10$ mV and transient hysteretic band of 30 mV. It is assumed that three capacitors were paralleled with $ESR = 8\,\text{m}\Omega$ and $ESL = 4.8$ nH for each. Other simulation parameters were $t_{\rm del} = 100$ ns and $R_{\rm eq} = 10\,\text{m}\Omega$.

Figs. 13–17 show the simulation results at different conditions.

1) $V(V_o)$ is the output voltage waveform.
2) $I(LAo)$ and $I(LBo)$ are the output inductor currents waveforms for Phase A and Phase B, respectively.

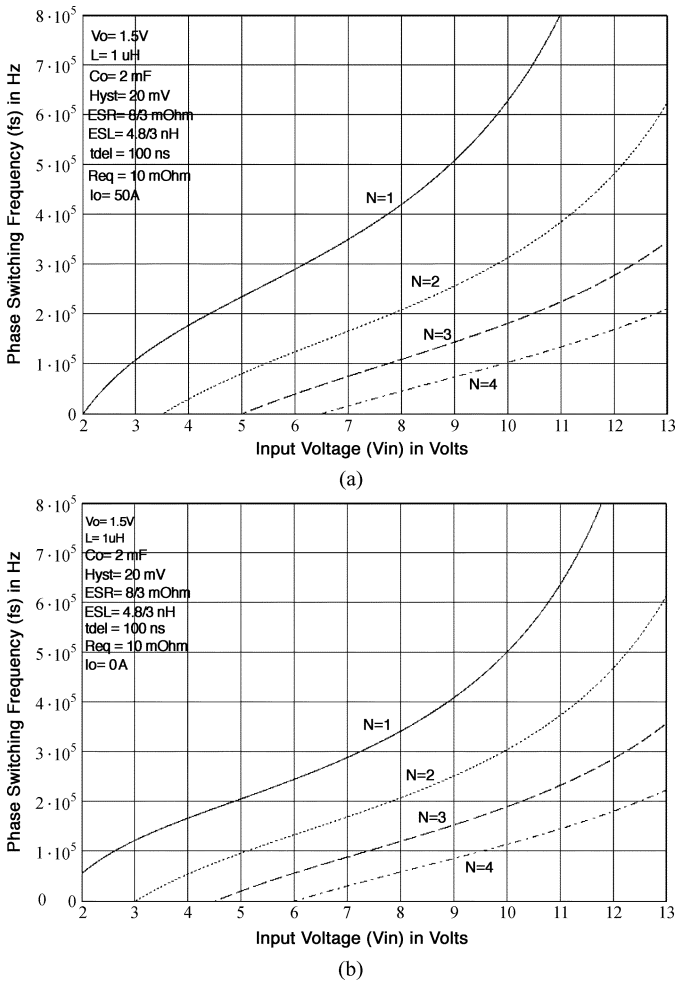


Fig. 11. Theoretical phase switching frequency versus input voltage for N Interleaved phases at (a) full load condition and (b) no load condition.

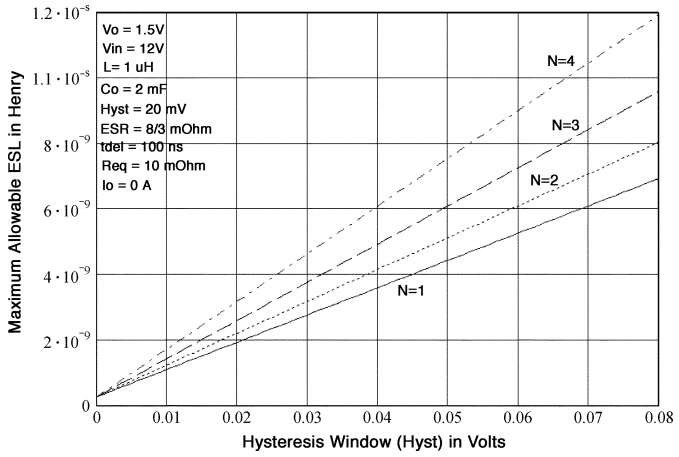


Fig. 12. Maximum allowable ESL versus hysteresis window for N interleaved phases.

3) $MCS$ is the hysteretic comparator output waveform derived directly from the output voltage ripple.
4) $V(Current\_Comp)$ is the current comparison waveform which is logic high when Phase A is smaller than Phase B, and logic low when Phase B is smaller than Phase A.

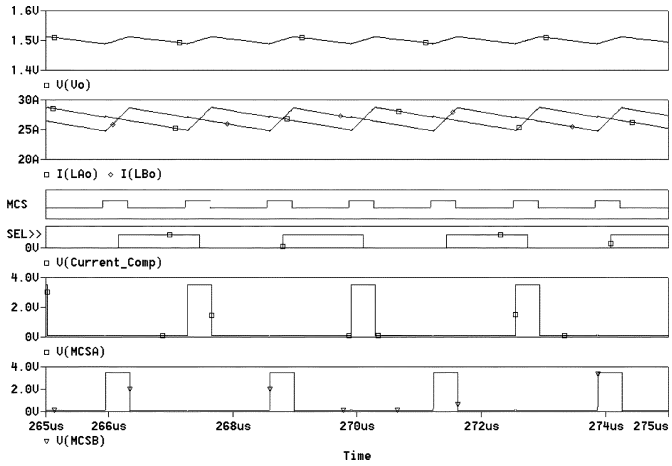


Fig. 13. Simulation results in steady-state condition.

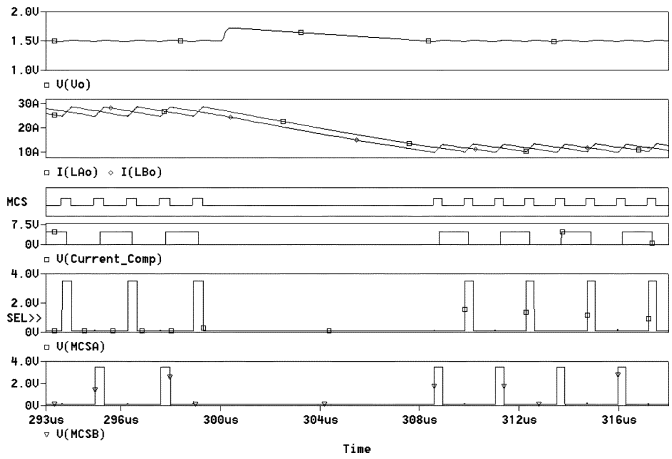


Fig. 14. Simulation results in high-to-low load transient condition.

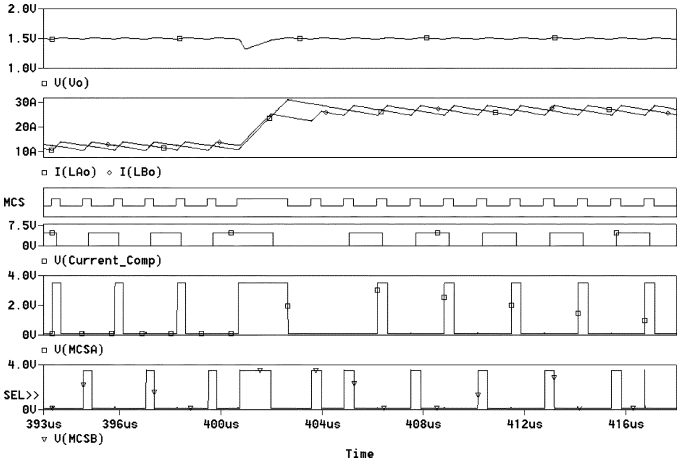


Fig. 15. Simulation results in low-to-high load transient condition.

5) $V(MCSA)$ and $V(MCSB)$ are the final high-side switches driving waveforms for Phase A and Phase B, respectively.

Fig. 13 shows the simulation results in steady-state condition. Figs. 14 and 15 show the simulation results at high-to-low load transient condition from 50 to 20 A and at low-to-high load transient condition from 20 to 50 A, respectively.

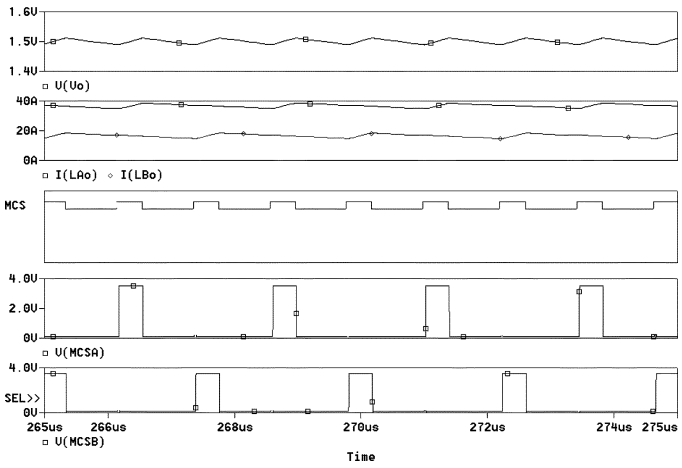


Fig. 16. Simulation results when the two phases are deliberately made unidentical so that phase A carries twice the current of phase B when the current sharing function is disabled.

Fig. 16 shows the simulation results when the current sharing function is disabled and the two phase currents are made different deliberately so that Phase A carries twice the current of Phase B. Fig. 17 shows the simulation results when the current sharing function is enabled for the case of Fig. 16, where Fig. 17(a) shows a sample waveform when the controller did not have to take a correction pulse to maintain the current sharing, and Fig. 17(b) shows a sample waveform when the controller had to take a correction pulse to maintain equal current sharing. It is apparent that the current sharing is maintained regardless of the large differences in the phase construction.

The simulations show that the switching frequency of the simulation results agrees with theoretical results of Fig. 11.

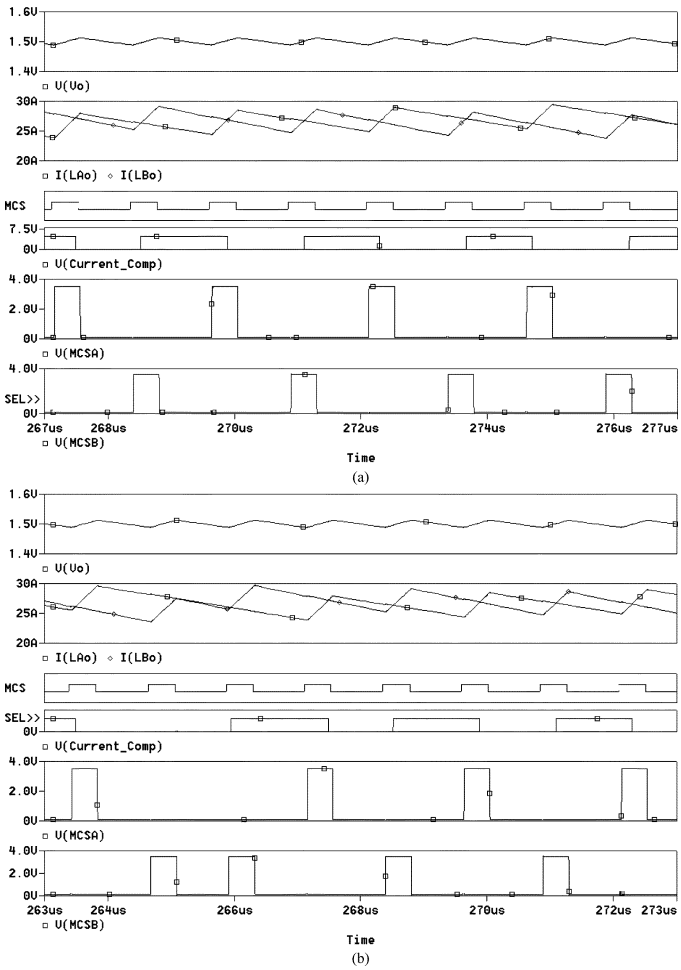


Fig. 17. Simulation results for the same case of Fig. 16 but when the current sharing function is enabled. Two waveform samples are shown: (a) with no current correction pulse and (b) with current correction pulse.

## VII. Experimental Results

Two-phase dc–dc buck converter experimental prototype with input voltage of 5 V and output voltage of 1.5 V and a maximum load current of 50 A is built for verification purposes.

Fig. 18 shows the experimental waveforms in steady-state for the output voltage, the high-side MOSFETs driving signals, and the output inductors currents when the current sharing function is enabled. Fig. 19 shows experimental output inductors currents of the two phases at load transients when the current sharing function is disabled and the two phases are deliberately made un-identical so that phase A carries more than three times the current of phase B. While Fig. 20 shows the results when the current sharing is enabled for the same case as Fig. 19. Fig. 21 shows the experimental waveforms when the controller had to take a corrective action to maintain equal current sharing.

It is clear that equal current sharing was achieved at all conditions, i.e., during full load steady-state, during low load steady-state, and during transients with small and large differences in the phases' layout.

The frequency of each phase was around 330 KHz even though the input is 5 V because of the total ESR and ESL. This matches the frequency (8) for the following parameters: $V_{\rm in} = 5$ V, $V_O = 1.5$ V, $L = 1$ $\mu$H per phase, $C_o = 2$ mF, $ESR = 10$ m$\Omega$, and $ESL = 3$ nH, $t_{\rm del} = 100$ ns, and $Hyst = 20$ mV, $R_{\rm eq} = 10$ m$\Omega$, and $I_o = 50$ A.

## VIII. Conclusion

Multiphase voltage-mode hysteretic control for dc–dc converters with current sharing method is presented in this paper. This current sharing method results in several advantages which include: simplicity to be applied to any control method, independent of the main control method used in the voltage regulation loop, no need for current reference, good equal current sharing accuracy at all load conditions in steady-state and transients, no need for compensation, and hence, does not affect the controller speed. Also, this sharing approach may be applied to any control method, even those that have no loop compensation such as multiphase hysteretic control. The application of the presented method is generalized for N interleaved phases.

Moreover, the presented current sharing method was applied to a multiphase voltage-mode hysteretic-controlled dc–dc converter, which resulted in a new and simple control technique with low output voltage ripple and fast transient response.

The frequency equation was derived for N interleaved phases by including ESR, ESL, and the path resistance with the output

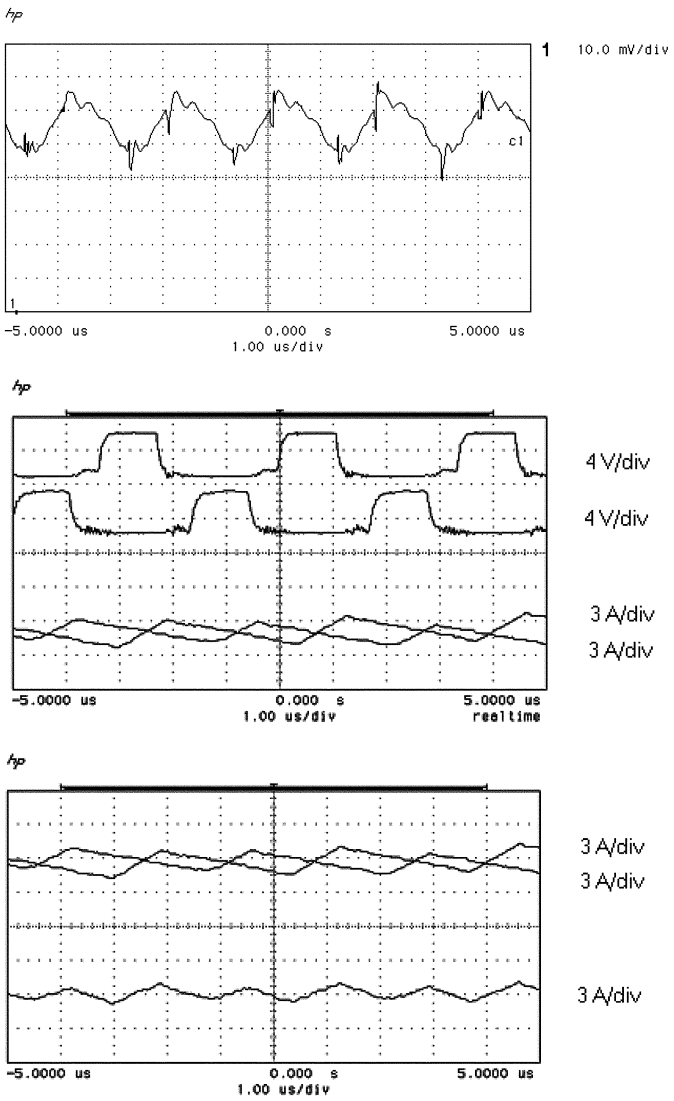


Fig. 18. Experimental waveforms in steady-state condition when the current sharing function is enabled: output voltage waveform, high-side MOSFETs driving signals, inductor currents, and total current, respectively.

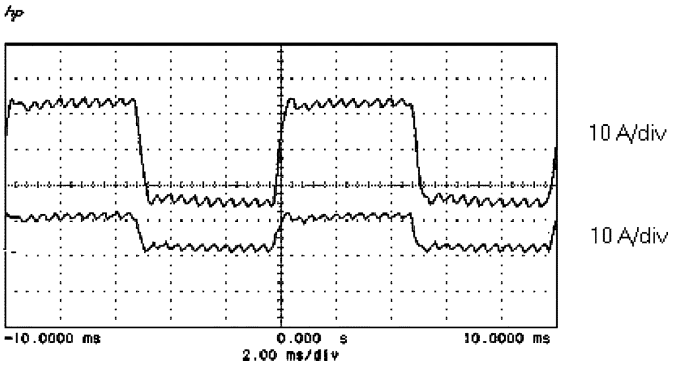


Fig. 19. Experimental output inductor currents of the two phases at load transients when the current sharing function is disabled and the two phases are deliberately made unidentical so that phase A carries more than three times the current of phase B.

current effect. Another equation that shows the maximum allowable ESL to keep the controller stable was also derived. Design

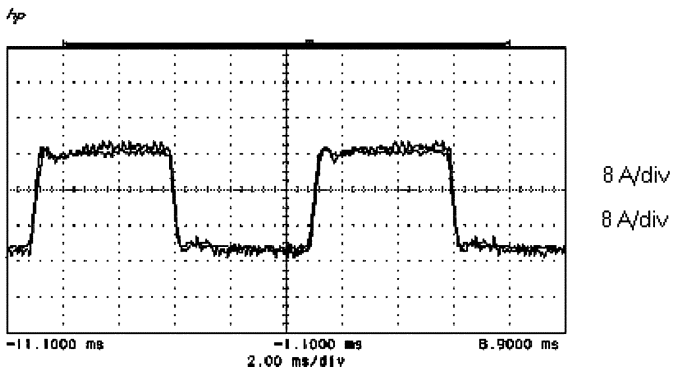


Fig. 20. Experimental output inductors currents for the same case as Fig. 19 but when the current sharing function is enabled.

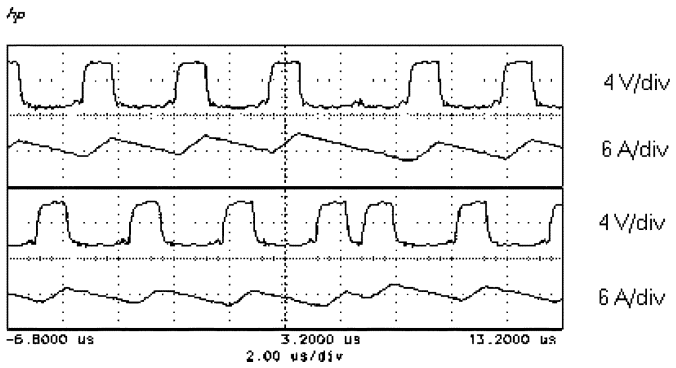


Fig. 21. Experimental results for the case of Fig. 20 when the controller had to take corrective action to maintain equal current sharing.

curves were plotted and compared to simulation results. An experimental prototype is built to verify the presented method.

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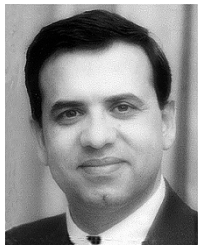
**Jaber Abu-Qahouq** (S'98–M'01) received the B.Sc. degree (first in class) in electronics engineering from Princess Sumaya University/Royal Scientific Society, Amman, Jordan, in 1998 and the M.S. and Ph.D. degrees from the University of Central Florida, Orlando, in 2000 and 2003, respectively.

He is currently a Visiting Assistant Professor in the Electrical and Computer Engineering Department, University of Central Florida. He has published over 20 research papers and several patents. He worked on several projects funded by the Florida Space Consortium, NASA, NSF, ASTEC Power, INTEL, and the University of Central Florida. His research interests include soft-switching power conversion, high-density low-voltage high-current fast-transient dc–dc converters, power factor correction converters, digital control in power electronics, and dc–ac inverters.

Dr. Abu-Qahouq received several awards including the Royal Watch. He is a member of Eta Kappa Nu, Phi Kappa Phi, and the IEEE Power Electronics and Circuits and System Societies.

**Hong Mao** received the B.S. degree from Sichuan University of Science and Technology, Chengdu, China, in 1992, the M.S. degree from Chongqing University, Chongqing, China, in 1997, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2000, all in electrical engineering.

He is currently a Senior Design Engineer with Astec Power, Andover, MA. From 1992 to 1994, he was an Assistant Professor with the Department of Electrical Engineering, Sichuan University of Science and Technology. From 1999 to 2000, he was a Project Leader in the ZTE (Zhongxing) Telecom Corporation, China. From 2000 to 2001, he was a Senior Engineer and Division Manager at PI Electronics, Hong Kong, where he led a team to develop adaptors for SONY laptop computers. From 2001 to 2002, he was with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, focusing on high-efficiency front-end dc–dc converters. In February 2002, he joined the University of Central Florida, Orlando, working on low-profile low-voltage dc–dc converters. He is an Assistant Director with the Florida Power Electronics Center, University of Central Florida. His current research interests include soft-switching dc–dc power conversion, power factor correction, and modeling of power electronic systems.



**Issa Batarseh** (S'84–M'85–SM'92) received the B.S. degree in computer engineering and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Chicago, in 1983, 1985, and 1990, respectively.

He is a Professor and Chair in the Electrical and Computer Engineering Department, University of Central Florida (UCF), Orlando. He was a Visiting Assistant Professor of electrical engineering at Purdue University, Hammond, IN, from 1989 to 1990, before joining the Department of Electrical and Computer Engineering, UCF, in 1991. He has more than 14 U.S. patents, and more than 50 refereed journal and 200 conference publications. His research work has been sponsored by Federal agencies and private sector. He published *Power Electronic Circuits* (New York: Wiley, 2003). His major research interest is power electronics, focusing on high frequency dc–dc conversion, soft-switching and dynamic modeling of dc-to-dc converters, dc–ac inverters, and power factor correction.

Dr. Batarseh received many national and international teaching, research, and service awards and is a member of Eta Kappa Nu. He served as Session Chairs and Committee Member for APEC and PESC Conferences. He will be the General Chair for the PESC'07 Conference, Orlando. He served as a Chairman of the IEEE Orlando Power Engineering Chapter, Chairman of the IEEE Orlando Section, and was Faculty Advisor for the IEEE Student Branch. He is a Registered Professional Engineer in Florida.