The Stacked Power System: A New Power Conditioning Architecture for Mainframe Computer Systems

Byungcho Choi, *Member, IEEE,* Bo H. Cho, *Member, IEEE,*
Fred C. Lee, *Fellow, IEEE* and Raymond B. Ridley, *Member, IEEE*

***Abstract*— The stacked power system combines series and parallel connections of multimodule power supplies to produce several low voltage outputs at high current levels. The system could generate ultra low voltage outputs with higher efficiencies than conventional centralized or distributed approaches, using standard single-output converters. This paper presents the architecture of the stacked power system and establishes a design procedure for the system.**

I. Introduction

RECENT advances in computer hardware have led to severe demands on computer power systems. Large mainframe computers require power systems which must provide several ultra low voltage outputs at ultra high current levels. This paper presents the power conditioning architecture developed for the IBM390 mainframe computer system. This new power system, hereafter referred to as the "stacked power system," employs a unique combination of series and parallel connections of a number of multimodule converters to produce low voltage outputs at high current levels.

Fig. 1 shows the block diagram of the stacked power system. The system consists of three converters (each with a number of power modules in parallel) connected in a stacked fashion, and provides five low voltage, high current outputs for the high-density emitter coupled logic circuits (represented by the five resistors in Fig. 1). V_{AB} (1.4 V) is regulated by Converter 1. V_{AC} (2.1 V) is regulated by Converter 2, and V_{AD} (3.6 V) is regulated by Converter 3. These three outputs are directly connected to R_{AB}, R_{AC}, and R_{AD}, respectively. The other two loads, R_{BC} and R_{BD}, utilize voltage differences between the outputs of two converters. R_{BC} utilizes the voltage difference between the output of Converter 2 (V_{AC} =2.1 V) and the output of Converter 1 (V_{AB} =1.4 V) to obtain an ultra low output voltage of 0.7 V. R_{BD} utilizes the voltage difference between the output of Converter 3 (V_{AD} =3.6 V) and the output of Converter 1 (V_{AB} =1.4 V) to obtain an output voltage of 2.2 V. While each converter has its own output capacitor, an additional load capacitor, C_{BC}, is employed across R_{BC} in order to further reduce the switching ripple on this particular output.

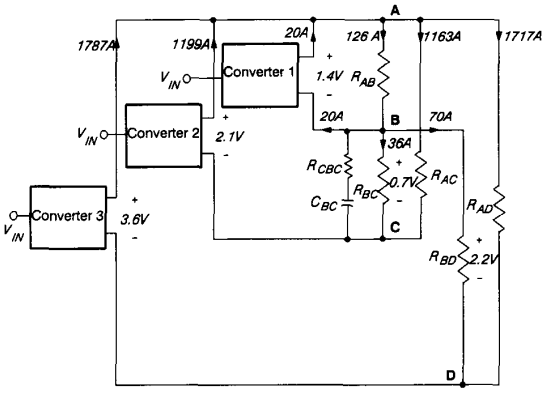


Fig. 1. Stacked power system: V_{IN} =287 V, C_{BC} =2720 μF, R_{CBC} =2.9 mΩ, R_{AB} =11 mΩ, R_{AC} =1.8 mΩ, R_{AD} =2.1 mΩ, R_{BC} =19 mΩ, R_{BD} =31 mΩ.

Three converters collectively deliver the high current to the loads. Converter 3 delivers 1787 A of current, Converter 2 delivers 1199 A, and Converter 1 delivers 20 A. The total current drawn from three converters is supplied to the three load resistors directly connected to the outputs of the converters: 126 A to R_{AB}, 1163 A to R_{AC}, and 1717 A to R_{AD}. The current through R_{AB} is further divided into three portions: 20 A back to Converter 1, 36 A to the load resistor R_{BC}, and 70 A to the load resistor R_{BD}. Each converter employs a number of power modules in parallel to deliver the high current efficiently. With current-mode control, the output current of each converter is equally distributed between the parallel modules, thereby improving reliability and providing fault-tolerance in the event of failure of a single module [1], [2]. Converter 1 has two modules in parallel, Converter 2 has four modules, and Converter 3 has six modules.

The current rating and number of power modules should be determined considering both the current requirement of each converter as a function of the individual load variation, and the fault-tolerance against the failure of a single module. The number and current rating of power modules for each converter are summarized in Table I.

Manuscript received April 13, 1993; revised June 13, 1994.

B. Choi is with the Power Electronics Team, Samsung Electronics Co., 82-3 Dodang-Dong, Wonmi-Ku, Buchun, Kyunggi-Do 421-130, South Korea .

B. H. Cho and F. C. Lee are with the Bradley Department of Electrical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA.

R. B. Ridley is with Ridley Engineering, Battle Creek, MI 49017 USA.

IEEE Log Number 9405304.

TABLE I
THE CURRENT RATING AND NUMBER OF POWER MODULES

	Maximum required current	Number of modules	Current Rating of individual module	Deliverable current with one module failed
Converter 1	126 Amps with: R_{AB} =11$m\Omega$ R_{BC} = ∞ R_{BD} = ∞	2	150 A	150 A
Converter 2	1199 Amps with: R_{BC} = 19 $m\Omega$ R_{AC} = 1.8 $m\Omega$	4	400 A	1200 A
Converter 3	1787 Amps with: R_{BD} = 31 $m\Omega$ R_{AD} = 2.1 $m\Omega$	6	400 A	2000A

The stacked power system offers several advantages. Most significantly, the stacked configuration could improve the overall efficiency considerably. As an example, Fig. 2 compares two different systems for the same low voltage, high current application. In the conventional approach of Fig. 2(a), the power conversion is performed by two stand-alone converters: Converter 1 delivers 400 A of current at the output voltage of 1.4 V, and Converter 2 delivers 200 A of current at the output voltage of 0.7 V. In this case, the loss associated with the internal voltage drop in the output diode (0.4 V for a Schottky diode) and the load current of two converters (600 A) is 240 W. In the stacked system of Fig. 2(b), each converter delivers 200 A of current for the same load requirements. The loss associated with the voltage drop in the diode (0.4 V) and the load current of two converters (400 A) is only 160 W, 33% less power loss compared to the conventional approach. Other unique features of the stacked power system include:

- generation of an ultra low voltage output using the voltage difference between the outputs of two converters.
- generation of five tightly regulated output voltages using only three single-output converters.

The dynamics of the converter operating as a subsystem of the stacked power system are markedly different from those of a stand-alone converter. The stacked configuration introduces complicated interactions between stacked converters and their associated loads. These subsystem interactions must be systematically characterized and properly incorporated in designing each converter. Otherwise, even though each converter might be properly designed for its stand-alone operation, the entire stacked power system could result in unacceptable performance or even instability.

Based on a comprehensive system level analysis, this paper presents a systematic design procedure for the stacked power system. The design procedure naturally incorporates all subsystem interactions and is simple enough to accommodate existing converter design techniques.

To verify the results of analysis and to demonstrate large-signal dynamics of the system, computer simulations are performed in both frequency- and time-domain. Frequency-domain simulations are performed using ASTAP [3] with

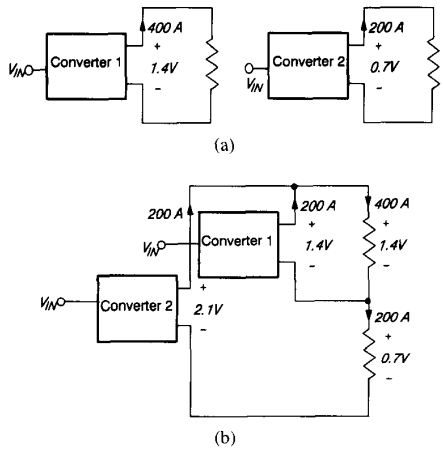


Fig. 2. Two approaches to the same application: (a) Two stand-alone converters. (b) Stacked system.

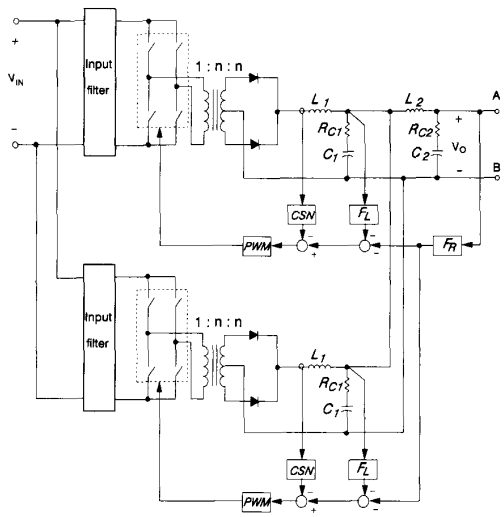


Fig. 3. Converter 1: V_{IN} =297 V, V_O =1.4 V, n =1/48, L_1 =0.82 μH, L_2 =0.15 μH, C_1 = 6000 μF, C_2 =0.052 F, R_{C1} = 5 mΩ, R_{C2} = 2 mΩ.

a small-signal model of the system [1], [2]. Time-domain simulations are performed using EASY5 [4] with an exact nonlinear model of the system. These simulation results will be used to substantiate theoretical discussions.

II. MULTIMODULE CONVERTER

Fig. 3 shows the schematic diagram of Converter 1 (Converter 2 and 3 have the same structure as Converter 1 other than the number of modules). Converter 1 consists of two full-bridge pulse width modulated (PWM) converter modules, a secondary LC filter (L_2 and C_2), and an output voltage feedback compensation circuit, F_R. The secondary LC filter is used to meet stringent ripple specifications. Each module consists of a power stage operating at 100 kHz ripple frequency, a PWM block, and two inner feedback circuits, CSN and F_L. CSN represents the current sensing network for the inductor current feedback. F_L is the compensation circuit for

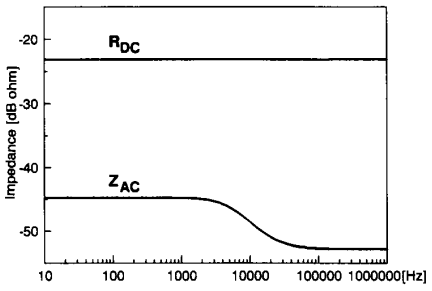


Fig. 4. Dc load (upper curve) and ac load (lower curve) of Converter 1.

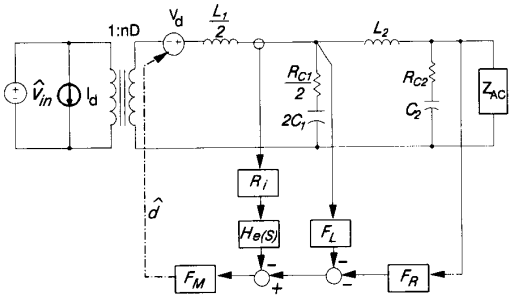


Fig. 5. Small-signal model of Converter 1: $I_d = (n^2 D V_{IN}/R_{DC})\hat{d}$, $V_d = nV_{IN}\hat{d}$ where D is the duty cycle of each switch with respect to the ripple frequency.

the voltage feedback from the output capacitor of each module. Reference [1] showed that this additional feedback offers significant improvements in the closed-loop performance of the converter, particularly the transient response in the event of failure of a module. Each module contains an input filter stage to prevent the pulsating switch current from being reflected to the input bus.

III. Load Dynamics and Design Strategy

One possible approach to simplifying the design of the stacked power system is to identify the effective load of each converter. Each converter in the stacked power system can be designed individually considering the remaining part of the system as its effective load. The control design using the effective load naturally incorporates the effects of subsystem interactions and offers good converter performance in the stacked configuration. Furthermore, the proper design of three individual converters using their effective loads would result in good performance of the entire stacked power system.

A converter operating as a subsystem of the stacked power system has unique load characteristics which cause significant impacts on the design. This section addresses these unique load characteristics and discusses the design strategy for the stacked converters.

A. Concept of ac Load and dc Load

The load of a converter is characterized by two different quantities. The first is the load impedance seen by the output of the converter, denoted as ac load Z_{AC}. The second is the ratio of the dc output voltage of the converter and the dc current drawn from the converter, denoted as dc load R_{DC}. These two load parameters, along with power stage parameters, fully characterize the small-signal dynamics of a converter and provide all information necessary to design the control loop and the input filter.

With the exception of a single converter with a purely resistive load, Z_{AC} and R_{DC} should be considered separately. For conventional converters, however, R_{DC} is identical to the magnitude of Z_{AC} evaluated at zero frequency ($|Z_{AC}|_{dc}$), since the power drawn from the converter should be the same as the power consumed at the load.

Unlike conventional converters, a converter in the stacked power system sees a complex load consisting not only of load resistors but also of the other converters in the system. In this case, the power drawn from the converter is not the same as the power consumed at the load. Due to this unique feature, R_{DC} can be completely unrelated with Z_{AC}. Fig. 4 compares the ac load, Z_{AC}, of Converter 1 with its dc load, R_{DC} =1.4 / 20 = 0.07 Ω (detailed discussions about Z_{AC} of Converter 1 will be given in Section IV). Converter 1 has an R_{DC} entirely different from $|Z_{AC}|$ for all frequencies. Since Z_{AC} and R_{DC} have two different roles in designing the converter, a clear distinction between Z_{AC} and R_{DC} is essential in designing the stacked power system.

B. Roles of ac Load and dc Load in Converter Design

In designing a converter, it is advantageous to design the control loop and the input filter separately. After designing the control loop assuming an ideal voltage source as the input of the converter, an input filter can be added whose output impedance is sufficiently lower than the closed-loop input impedance of the power stage. This approach simplifies the design and minimizes undesirable interactions between the input filter and control loop.

Fig. 5 shows the reduced-order small-signal model of Converter 1 with an ideal voltage source. Reference [1] showed that this reduced-order model preserves the small-signal characteristics of the original two-module converter. F_M is the modulator gain of PWM block, R_i is the current sensing network gain, and $H_e(s)$ represents the sampling gain of the current mode control [5]. Two load parameters, Z_{AC} and R_{DC}, are embedded in the small-signal model. From Fig. 5, it can be easily seen that the dependent current source I_d, the only parameter depending on R_{DC}, has no effect on transfer functions from the duty cycle to various feedback signals. In deriving these transfer functions, $\hat{v}_{in}$ is assumed to be zero and absorbs I_d. Thus the only load parameter which affects the control loop design is the ac load Z_{AC}. (This is true only for buck-derived topologies. For boost-derived topologies, both Z_{AC} and R_{DC} must be considered in the control loop design.)

On the other hand, R_{DC} directly affects the input filter design. As will be illustrated in Section V, R_{DC} can be used to estimate the minimum magnitude of the closed-loop input impedance of the power stage. This information is critical in designing an input filter which minimizes interactions with the control loop [6].

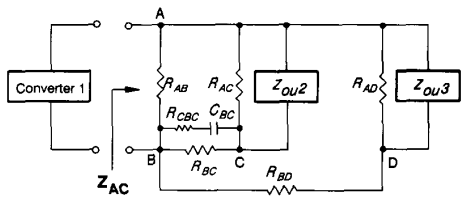


Fig. 6. Load impedance of Converter 1: $Z_{OU}2$ represents the output impedance of Converter 2, and $Z_{OU}3$ is the output impedance of Converter 3.

IV. Control Loop Design

This section discusses the control design of stacked converters using ac load, Z_{AC}. First Z_{AC} of each converter is analyzed in detail. Then the control design is presented based on the results of ac load analysis.

A. Load Impedance Analysis

The load impedance of a stacked converter is a complex combination of the load resistors/capacitor and the output impedance of the other converters. Fig. 6 shows the load impedance of Converter 1, where $Z_{OU}2$ and $Z_{OU}3$ represent the output impedance of Converter 2 and Converter 3 without load, hereafter referred to as an "unloaded output impedance," respectively. The load impedance of Converter 2 and 3 can be derived similarly from Fig. 1.

To analyze the load impedance of the converter, the unloaded output impedance of a converter should be characterized first. Fig. 7 shows the simplified small-signal model of a converter (Fig. 7(a)) and its corresponding block diagram (Fig. 7(b)). From Fig. 7(b), the unloaded output impedance can be derived as

$$Z_{OU} = \frac{\hat{v}_R}{\hat{i}_O} = \frac{Z_P + T_I\left[Z_P - \frac{F_4F_1}{F_5}\right] + T_L\left[Z_P - \frac{F_2F_1}{F_3}\right]}{1 + T_I + T_L + T_R} \tag{1}$$

where Z_P is the open-loop output impedance and T_I, T_L, T_R are given by

$$T_I = F_M F_5 R_i H_e(s),$$
$$T_L = F_M F_3 F_L,$$
$$T_R = F_M F_1 F_R.$$

While the unloaded output impedance is a complicated frequency-dependent quantity, its asymptotic behavior can be easily deduced. At low frequencies, T_R approaches infinity due to the integrator contained in F_R; this consequently reduces Z_{OU} to zero, regardless of the numerator of (1). At high frequencies, T_I, T_L, and T_R reduce to zero, and Z_P approaches the equivalent series resistor (ESR) of the secondary filter capacitor (R_{C2} in Fig. 7(a)). Thus Z_{OU} approaches ESR of the secondary filter capacitor at high frequencies. Fig. 8 shows the unloaded output impedance of Converter 1. The output impedance decreases monotically at low frequencies and is limited by ESR of the secondary filter capacitor (2 mΩ = −54 dBΩ) at high frequencies.

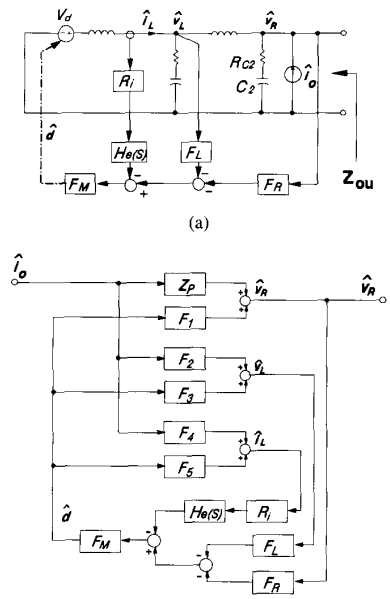


Fig. 7. Simplified small-signal model of converter: (a) Circuit model: In deriving the unloaded output impedance, $\hat{v}_{in}$ in Fig. 5 is assumed to be zero so $\hat{v}_{in}$, I_d, and the ideal transformer are not included. (b) Block diagram: Gain blocks Z_P and F_1 through F_5 represent various open-loop transfer function of the power stage. The other blocks are feedback compensations and small-signal model of the controller.

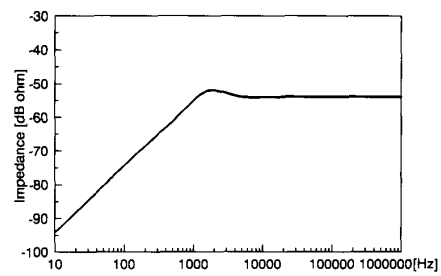


Fig. 8. Unloaded output impedance of Converter 1.

Based on the previous analysis, two resistors can be identified which approximate the asymptotic behavior of the load impedance of the converter:

- R_{eq}(low): low frequency approximation of Z_{AC} obtained by replacing the unloaded output impedance of each converter with a short circuit and replacing the load capacitor with an open circuit.
- R_{eq}(high): high frequency approximation of Z_{AC} obtained by replacing the unloaded output impedance with the ESR of the secondary filter capacitor and replacing the load capacitor with its ESR.

Using these definitions, R_{eq}(low) and R_{eq}(high) of three converters are calculated as follows:

Converter 1: $R_{eq}(low)$ =5.77 mΩ (-44.8 dB Ω), $R_{eq}(high)$ =2.29 mΩ (- 52.8 dBΩ);

Converter 2: $R_{eq}(low)$ =1.65 mΩ (−55.65 dBΩ), $R_{eq}(high)$ =1.26 mΩ (−55.99 dBΩ);

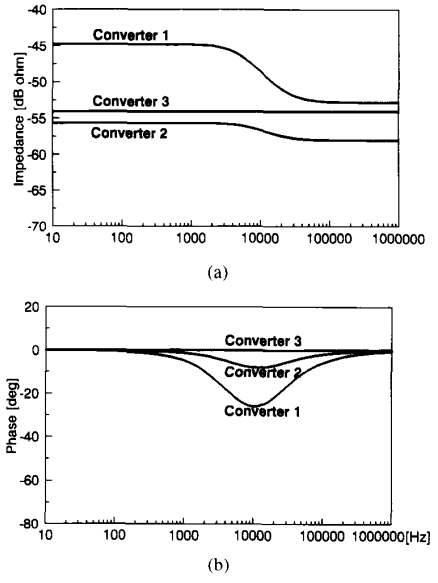


Fig. 9. Load impedance of converters: (a) Gain. (b) Phase.

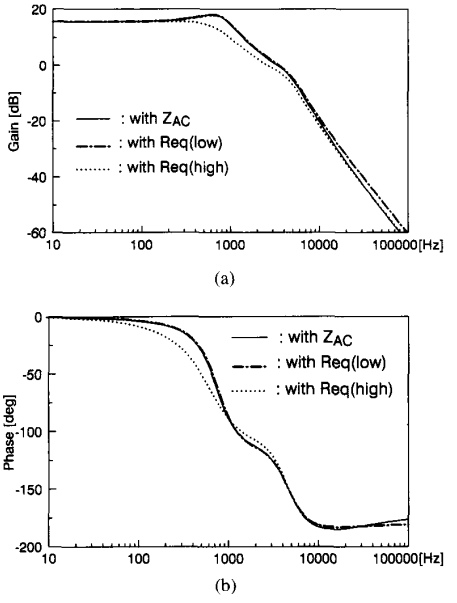


Fig. 10. Control-to-output transfer function of Converter 1 with three different loading conditions: (a) Gain. (b) Phase.

Converter 3: $R_{\rm eq}(low)$ =1.967 mΩ (−54.13 dBΩ), $R_{\rm eq}(high)$ = 1.972 mΩ (−54.10 dBΩ).

Fig. 9 shows the actual load impedance of three converters in the stacked power system. The low and high frequency asymptotes of $|Z_{\rm AC}|$ are in good agreement with the respective values of $R_{\rm eq}$(low), and $R_{\rm eq}$(high). The phase characteristics of the load impedance confirm that $Z_{\rm AC}$ behaves like a resistor at both low- and high-frequencies. For Converter 3, $R_{\rm eq}$(low) and $R_{\rm eq}$(high) are almost identical, and its load impedance is effectively a resistor.

B. Open-Loop Dynamics of Converter

The open-loop dynamics of the stacked converter can be characterized by $R_{\rm eq}$(low) and $R_{\rm eq}$(high). Fig. 10 shows the control-to-output transfer function of Converter 1 with three different loading conditions: the first with the actual load impedance, $Z_{\rm AC}$, the second with a load resistor of $R_{\rm eq}$(low), and the last with a resistor of $R_{\rm eq}$(high). As shown in Fig. 10, $R_{\rm eq}$(low) predicts the low-frequency behavior of Converter 1, and $R_{\rm eq}$(high) predicts the high frequency behavior of Converter 1. The dc gain of the transfer function is independent of the load impedance.

C. Control Loop Design Strategy

In general, the closed-loop performance of a converter is evaluated by stability margins of the loop gain, the peak value of audio-susceptibility and output impedance. Since these performance criteria are determined practically by high-frequency characteristics of a converter, $R_{\rm eq}$(high) can be used as an equivalent resistive load for control loop design purposes. Control design using the load resistor of $R_{\rm eq}$(high) offers a good closed-loop performance of a converter in the stacked power system. Furthermore, the proper design of three individual converters using their $R_{\rm eq}$(high) would result in a good performance of the entire system.

Detailed design procedures for a multimodule converter with a resistive load are given in [1]. Following those procedures, the control loop of three converters are designed individually using their equivalent resistive load, $R_{\rm eq}$(high).

D. Design Verification

To confirm the validity of using $R_{\rm eq}$(high) for the control loop design, Fig. 11 shows the loop gain of Converter 1 with two different loading conditions: one with the actual load impedance, $Z_{\rm AC}$, and the other with a load resistor of $R_{\rm eq}$(high). The converter shows very similar loop gain characteristics except for the discrepancy around the power stage resonance, where $Z_{\rm AC}$ behaves like $R_{\rm eq}$(low). Fig. 12 compares the loop gain (Fig. 12(a)) and output impedance (Fig. 12(b)) of Converter 2 with $Z_{\rm AC}$ and $R_{\rm eq}$(high). The converter shows almost identical closed-loop performance with two different loading conditions. Similar observations can be made from transfer functions of Converter 3.

V. Input Filter Design

This section addresses the use of $R_{\rm DC}$ in the input filter design. Fig. 13(a) shows the simplified block diagram of Converter 1, which has an input filter for each module. To avoid undesirable interactions between input filter and power stage, the output impedance of the input filter ($Z_{\rm OF}$ in Fig. 13(a)) should be sufficiently lower than the closed-loop input impedance of the power stage ($Z_{\rm IC}$ in Fig. 13(a)) for all frequencies.

For a converter with a high loop-gain crossover frequency, the minimum magnitude of the closed-loop input impedance of

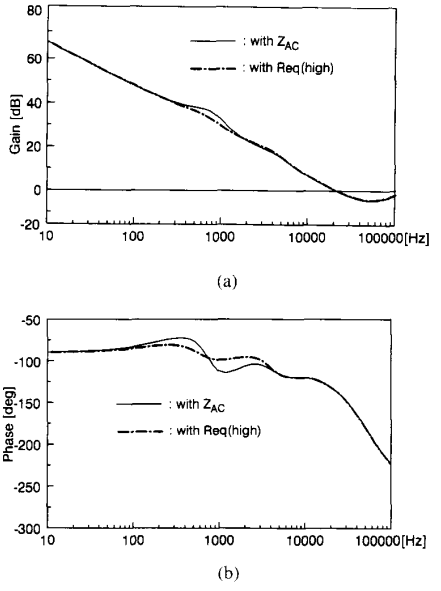


Fig. 11. Loop gain of Converter 1 with two different loading conditions: (a) Gain. (b) Phase.

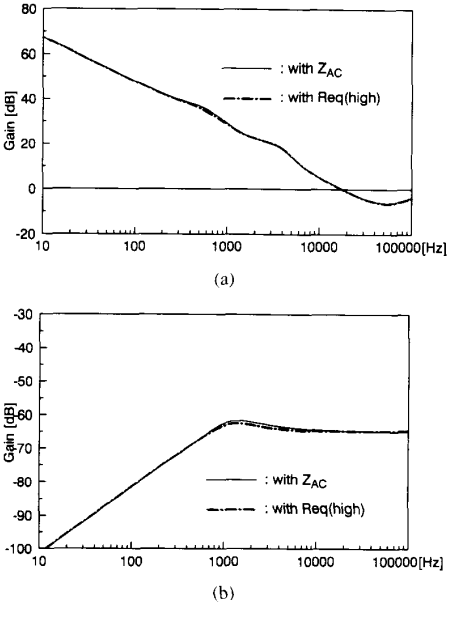


Fig. 12. Closed-loop performance of Converter 2 with two different loading conditions: (a) Loop gain. (b) Output impedance.

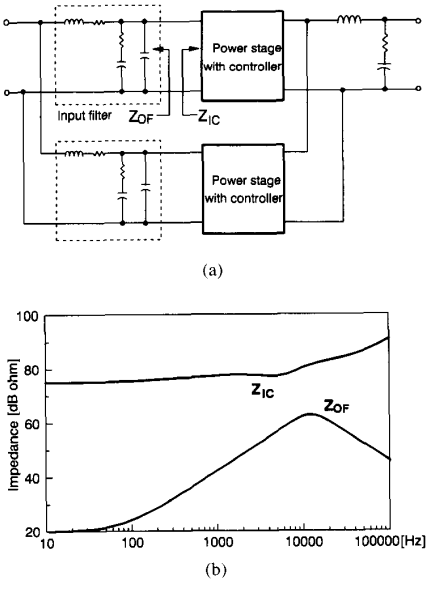


Fig. 13. Input filter design for Converter 1: (a) Simplified block diagram of Converter 1. (b) Impedance comparison at interface between input filter and power stage.

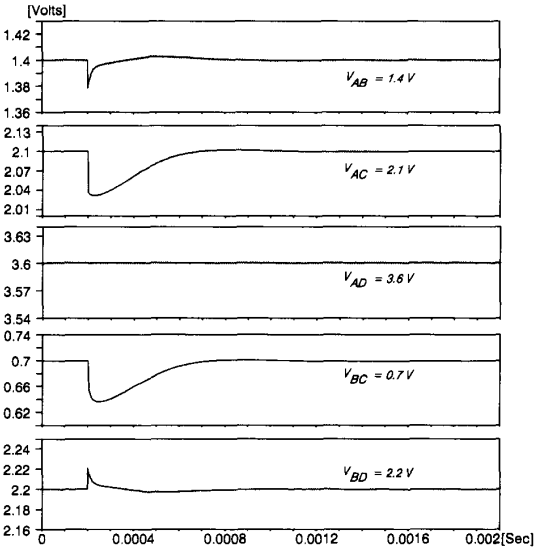


Fig. 14. Step load responses of system outputs.

the power stage ($|Z_{\mathrm{IC}}|_{\min}$) is determined by its low frequency value, which is directly related to the dc load R_{DC}[6]:

$$|Z_{\mathrm{IC}}|_{\min} \approx |Z_{\mathrm{IC}}|_{\mathrm{DC}} = k\frac{R_{\mathrm{DC}}}{n^2 D^2} \tag{2}$$

where

k : number of modules,
n : turns ratio of the power transformer,
R_{DC} : dc load of the multimodule converter, and
D : duty cycle.

Once $|Z_{\mathrm{IC}}|_{\min}$ is determined using R_{DC}, an input filter can be designed to offer a sufficient gap between $|Z_{\mathrm{IC}}|_{\min}$ and the maximum magnitude of its output impedance ($|Z_{\mathrm{OF}}|_{\max}$), using standard filter design techniques. Fig. 13(b) shows the input impedance of the power module and the output impedance of the input filter. The upper curve is the closed-loop input impedance of the power stage, whose minimum magnitude is calculated as 76 dB from (2). The lower curve is the

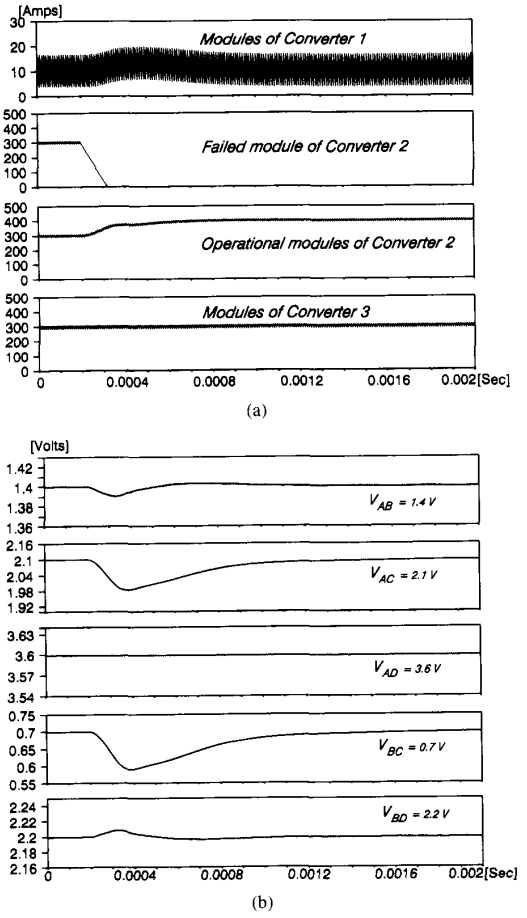


Fig. 15. Module-failure response of the system: (a) Inductor current of modules. (b) System outputs.

output impedance of the filter, designed to offer 13 dB margin between $|Z_{\mathrm{OF}}|_{\max}$ and $|Z_{\mathrm{IC}}|_{\min}$. The wide separation between the two impedances minimizes the undesirable interactions between the input filter and the power stage, which could result in the performance degradation or instability.

VI. Transient Responses of the Stacked Power System

Fig. 14 illustrates the transient response of five outputs of the system, due to a step change in the load current through R_{AC} (step size, $I_{\mathrm{STEP}} = 117$ A). The maximum undershoot ($V_{\min}$) and settling time (t_s) of V_{AC}, which is the output of Converter 2, can be predicted from the peak value ($|Z_O|_{\max} = -65$ dB) and the corner frequency ($f_p = 1$ kHz) of the output impedance of Converter 2 shown in Fig. 12(b) [7]:

$$V_{\min} = 2.1 - I_{\mathrm{STEP}} \times 10^{|Z_O|_{\max}/20} = 2.034\,\mathrm{V}$$

$$t_s = \frac{3}{2\pi f_p} = 0.48\,\mathrm{ms}.$$

To avoid the shut-down of the entire power system due to a single point failure, each converter employs a number of modules in parallel. Also, to minimize the disturbance in the system outputs when one module fails, each converter employs a feedback from the output capacitor of each module. Fig. 15 illustrates the transient response of the system, due to the switch-open failure of the fourth module of Converter 2. Fig. 15(a) shows the transient response of inductor currents of three converters in the system. The inductor current of the failed module of Converter 2 (the second curve) decreases linearly until blocked by freewheeling diodes. The inductor current of the operational module of Converter 2 (the third curve) increases to supplement the load current of the failed module. Fig. 15(b) shows the transient responses of five outputs of the system. V_{AC}, the output of Converter 2, experiences the maximum undershoot of 0.12 V. V_{BC}, the voltage difference between the outputs of Converter 2 and Converter 1, is directly affected by the module failure of Converter 2, and exhibits essentially the same disturbance as V_{AC}.

The large-signal simulations of Figs. 14 and 15 reveal the robustness of the system against some large-signal disturbances. The control system, designed for sufficient stability margins at one operating point, maintains the system stability at different operating conditions. Comprehensive large-signal simulations, which further demonstrate the robustness of the system against various changes of operating conditions, can be found in [8].

VII. Conclusion

A new power conditioning architecture for mainframe computer systems is presented. The power system employs a stacked configuration of standard multimodule converters, and could generate several ultra low voltage outputs at ultra high current levels with higher efficiencies.

The converter in the stacked power system has unique load characteristics. The ac load and dc load, which play two distinctive roles in designing the converter, are totally unrelated. Thus a clear distinction between the ac load and dc load is essential in designing the system. This paper established a design procedure for the system, which properly incorporates the unique load characteristics, and is simple enough to accommodate standard design techniques.

Acknowledgment

The authors express their gratitude to IBM-Kingston for the original proposition of the stacked power system, financial/technical support during the course of the research, and the generous permission to release information covered in this paper.

References

[1] B. Choi, B. H. Cho, F. C. Lee, and R. B. Ridley, "Three-loop control for multimodule converter systems," *IEEE Trans. Power Electron.*, vol. 8, pp. 466–474, Oct. 1993.

[2] B. Choi, "Dynamics and control of switchmode power conversions in distributed power systems," Ph.D. dissertation, Virginia Polytechnic Institute and State University, May 1992.
[3] International Business Machines Co., "ASTAP program reference manual [5796-PBH]," May 1984.
[4] Boeing Computer Services, "EASY5 dynamic analysis system user's guide," 1983.
[5] R. B. Ridley, "A new continuous-time model for current mode control," *IEEE Trans. Power Electron.*, vol. 6, pp. 271–280, Apr. 1991.
[6] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *IAS Conf. Rec.*, 1976, pp. 366–382.
[7] F. C. Lee, Y. Yu, and M. F. Mahmoud, "A unified analysis and design procedure for a standardized control module for dc-dc switching regulator," in *PESC Conf. Rec.*, 1979, pp. 284–301.
[8] B. Choi, B. Cho, R. B. Ridley, and F. C. Lee, "Modeling and design of parallel-module power supplies: Part II; Modeling and design of stacked power system," IBM-K Final Report (KGN-0022), Feb. 1990.

Byungcho Choi (S'89–M'92) received the B.S. degree in electronics from Hanyang University, Seoul, Korea, in 1980, and the M.S. and the Ph.D. degrees in electrical engineering from Virginia Polytechnic Institute and State University (VPI&SU), Blacksburg, in 1988 and 1992, respectively.

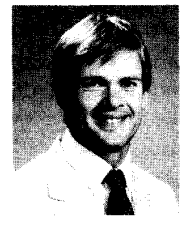
From 1980 to 1985, he was employed as a research engineer in the Agency for Defense Development, Seoul, Korea, where he developed switchmode power supplies for pulsed laser applications. From 1992 to 1993, he was a Research Scientist at the Bradley Department of Electrical Engineering, VPI&SU, working on the analysis of the performance and stability of the Space Station Freedom power system. In 1994, he joined the Power Electronics Team of the Samsung Electronics Co., where he is presently the leader of the Power System Group. His research experience includes modeling and design optimization of high-frequency power converters, space power systems, computer power systems, and distributed power systems. His current research is focused on power conversion and battery management for battery-powered electronics.

Bo H. Cho (M'89) received the M.S. and B.S. degrees in electrical engineering from California Institute of Technology and the Ph.D. degree, also in electrical engineering from Virginia Polytechnic Institute & State University.

Prior to his research at VPI&SU, he has worked for two years as a Member of Technical Staff of Power Conversion Electronics Department, TRW Defense and Space System Group, where he was involved in the design and analysis of spacecraft power processing equipment. He joined the Department of Electrical Engineering, VPI&SU in 1982, where he is presently an Associate Professor. His main research interests include power electronics, modeling, analysis and control of spacecraft power processing equipment, power systems for space stations and space platforms, and distributed power systems.

Dr. Cho was a recipient of the 1989 Presidential Young Investigator Award (YPI) from the National Science Foundation. He is a member of the IEEE Power Electronics Society and Tau Beta Pi.

Fred C. Lee (S'72–M'74–SM'87–F'90), for a photograph and biography, see this issue, p. 600.



Raymond B. Ridley (M'90) received the M.S. and Ph.D. degrees in electrical engineering from Virginia Polytechnic Institute and State University, with a thesis on parallel power supplies, and a dissertation on a new model for current-mode control.

Until 1991, he was the assistant director of the Virginia Power Electronics Center. He has published numerous papers in the areas of control, computer-aided design, topologies and circuits for power electronics applications. He is currently a power electronics consultant at Ridley Engineering, specializing in systems analysis, power supply design, computer-aided engineering for power systems, and power electronics training.