Short Summary on Stacked DC-DC Systems

1 Advantages of stacked DC/DC systems

Current reduction is the main purpose of on-die switching DC-DC converter. The total input current can be dramatically reduced to 3.4x smaller as shown in [1].

However, integration of on-die switching DC-DC converter in the way shown in [1] has the following drawbacks,

1. Due to the cost of on-die DC-DC converters, it is hard to implement multiple voltage domain by this method. As shown in [1], decap occupies around 10% of the chip area, and coupled inductor occupies 16% of the chip area. To implement a 2 voltage level domain, it requires half of the chip area.

2. Large current still need to be delivered from the on-die DC-DC converter to gates.

On the other hand, our proposed method has the following advantages.

1. The cost to implement multiple voltage domain is significantly reduced because on-die PFM DC/DC converter is just used to compensate the unbalance between blocks and voltage level setting. This cost reduction enables us to implement multiple voltage domain with on-die DC/DC converters. Note that multiple voltage domain has been widely accepted as a powerful technique to reduce the total power.

2. Due to current recycling, the current go through the whole chip is reduced. While in [1] only current between VRM and on-die DC/DC converter are reduced.

The overhead of the proposed scheme is the level shifter between different voltage domains. This is actually indispensible in a design with multiple supply voltage domain enabled.

2 Schematics of stacked DC-DC systems

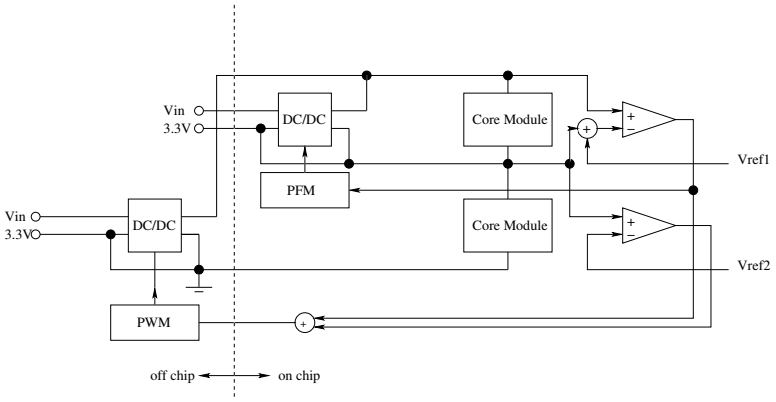

Figure 1: Schematic of 2-level stacked DC-DC converters

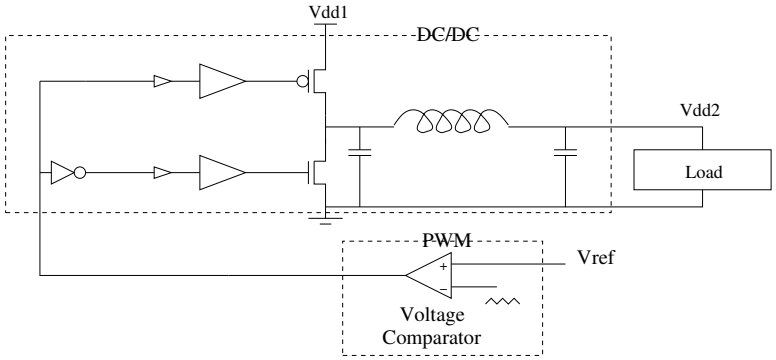

Figure 2: Schemattic of ZVS PWM Buck DC-DC converter.

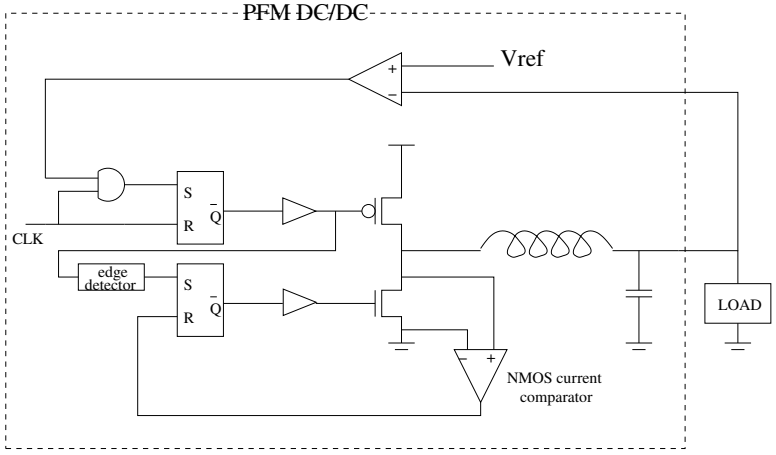

Figure 3: Schemattic of PFM Buck DC-DC converter.

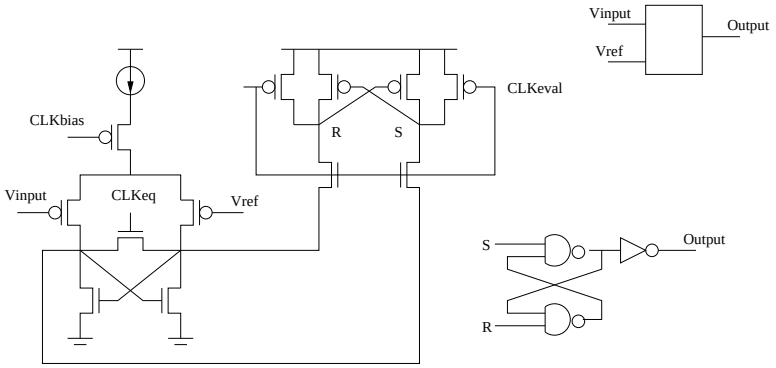

Figure 4: Voltage comparator.

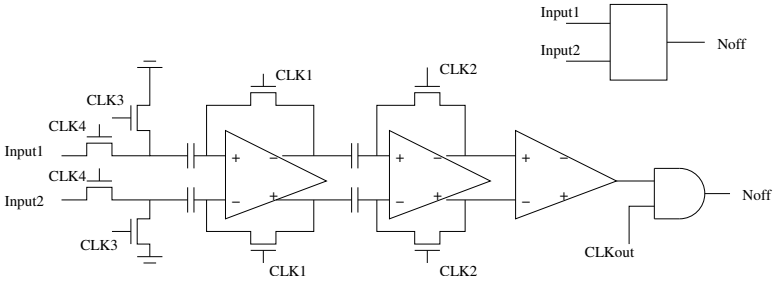

Figure 5: Current comparator.

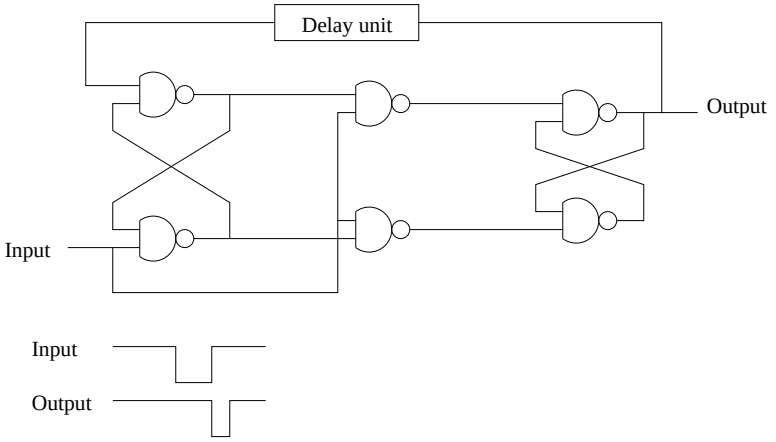

Figure 6: Edge detector.

3 Determination of design parameters

3.1 Buck DC-DC converters

3.1.1 zero voltage switching

Zero voltage switching (ZVS) means that the internal point of DC-DC converters switches under a zero voltage. [2] has detailed description on how to achieve zero voltage switching. My experiment results show

that under 5MHz operation frequency, without ZVS results in an over 15% additional power loss. It also increases with the operation frequency. Therefore, ZVS is critical if we want to use high operation frequency to reduce the area of LC filter.

3.1.2 Output voltage ripple

According to [3], the current ripple on the inductor and voltage ripple on the capacitor are

$$\Delta i = \frac{(V_{DD1} - V_{DD2})D}{2Lf_s} \tag{1}$$

and

$$\Delta V_{DD2} = \frac{(V_{DD1} - V_{DD2})D)}{16LCf_s^2} = \frac{\Delta i}{8Cf_s} \tag{2}$$

, respectively, where L is the filter inductance, C is the filter capacitance, f_s is the switching frequency, and D is the duty cycle. This formulas have been verified by SPICE simulations.

3.1.3 Power efficiency

The efficiency of a buck converter is

$$\eta = 100 \times \frac{P_{load}}{P_{load} + P_{buck}} \tag{3}$$

where P_{buck} is the average total internal power consumption of a buck conversion, which could be approximated by the total power loss of two power transistors. The total power loss of a MOSFET is a combination of conduction losses and dynamic switching losses, i.e.,

$$P_{MOS} = i_{rms}^2 R + \frac{\alpha}{\alpha - 1}(C_{ox} + C_{gs} + 2C_{gd} + C_{db})V_{DD1}^2 f_s, \tag{4}$$

where R is the equivalent resistance of the transistor, i_{rms} is the root mean square current passing through the MOSFET, α is the tapering factor of the power MOSFET gate drivers, C_{ox}, C_{gs}, C_{gd} and C_{db} are the gate oxide, gate-to-source overlap, gate-to-drain overlap and drain-to-body junction capacitances, respectively. The equvivalent resistance of the transistor can be calculated as

$$R = \frac{1}{\mu_n c_{ox}(V_{DD1} - V_{th})} \cdot \frac{L}{W}, \tag{5}$$

where μ_n is the electron mobility with a typical value of $0.05 m^2 V^{-1} s^{-1}$, and

$$c_{ox} = \frac{\epsilon_0 \epsilon_{SiO_2}}{T_{ox}} \tag{6}$$

$$= \frac{8.854 \cdot 10^{-14} \cdot 3.9}{2.5 \cdot 10^{-9}} \tag{7}$$

$$= 1.38 \times 10^{-4} (F/m^2) \tag{8}$$

Here, we use 100nm generation and assume T_{ox} equals to $2.5 \cdot 10^{-9} m$.

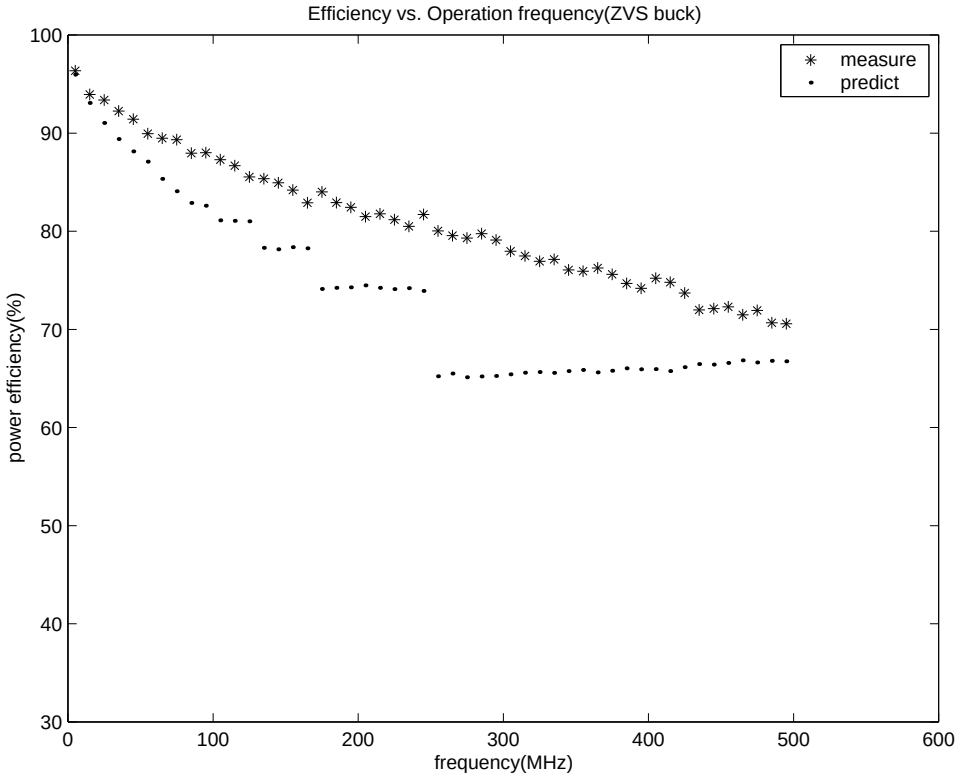

Figure 7: Power efficiency versus operation frequency in ZVS buck DC-DC converters.

3.1.4 Frequency versus efficiency

Design parameters are scalable w.r.t operation frequency. If we assume the same ratio between low-to-high dead time and high-to-low dead time, Δi should be fixed, which makes L of LC filter reversely proportional to f_s. Also, If we assume the same ΔV_{DD2}, C of LC filter is also reversely proportional to f_s. Also, the width of power transistors is reversely proportional to the square root of f_s.

Fig. 7 shows the curve of power efficiency versus operation frequency. Each point represents a design, which is obtained by scaling the design parameters w.r.t operation frequency. Note that at 500MHz, the LC filter has a capacitance of 8.08n, which is equivalent to around $1mm^2$.

3.2 PFM DC-DC converters

3.2.1 Output voltage ripple

In PFM DC-DC converters, energy is delivered from input voltage supply to output capacitor by opening the PMOS power transistors for a short time period. The NMOS power transistor is open once the PMOS power transistor is closed to maintain a current path. It is closed When the current going through decrease

to zero. This process provides a pulse of energy to supply to loading and also slightly increase the output voltage level.

Assuming the input voltage level is V_{DD} and output voltage level is V_O, we have

$$L \cdot \frac{di}{dt} = V_{DD} - V_O \tag{9}$$

$$i(t) = \frac{V_{DD} - V_O}{L} \cdot t, \tag{10}$$

where $i(t)$ is the current going through output inductor L. Assuming the time period to open $PMOS$ transistor is T, we can obtain that the peak current is

$$i(T) = \frac{V_{DD} - V_O}{L} \cdot T, \tag{11}$$

Assuming the current is triangle, we can obtain that this current pulse raise the output voltage by:

$$C \cdot \Delta v = \frac{1}{2} \cdot i(T) \cdot T \cdot (1 + \frac{V_{DD} - V_O}{V_O}) \tag{12}$$

$$C \cdot \Delta v = \frac{1}{2} \cdot i(T) \cdot T \cdot \frac{V_{DD}}{V_O} \tag{13}$$

$$\Delta v = \frac{V_{DD} - V_O}{LC \cdot D} T^2 \tag{14}$$

The maximum loading power the DC-DC converter can provide without lowing the output voltage level is

$$P_{max} = \frac{1}{2} \cdot V_O \cdot i(T) \tag{15}$$

$$= \frac{1}{2} \frac{(V_{DD} - V_O) \cdot V_O}{L} \cdot T \tag{16}$$

3.2.2 Power efficiency

The switching energy loss for a pulse is equal to

$$E_{switch} = \frac{1}{2} \cdot C_x (V_{DD} - V_O)^2 + \frac{1}{2} \cdot C_x V_{DD}^2 + \frac{1}{2} C_x V_O^2 \tag{17}$$

The conduct power loss of the PMOS power transistors is

$$P_{conduct} = \frac{1}{6} I(T)^2 \cdot (R_{PMOS} + R_{NMOS} \tag{18}$$

$$= \frac{1}{6} (R_{PMOS} + R_{NMOS}) \cdot (\frac{V_{DD} - V_O}{L} \cdot T)^2 \tag{19}$$

The total energy delivered to the output capacitor is

$$E_{deliver} = \frac{1}{2} I(T) \cdot V_O \cdot T \tag{20}$$

Therefore, the power efficiency is

$$\eta = 1 - \frac{E_{switch} + P_{conduct} * T * D}{E_{deliver}} \tag{21}$$

3.2.3 Loading versus efficiency

PFM buck converters have a relatively large power efficiency when the loading is low. We show this point in Fig. 8. This figure shows that the efficiency is still acceptable when the loading capacity is very low (less than 3%).

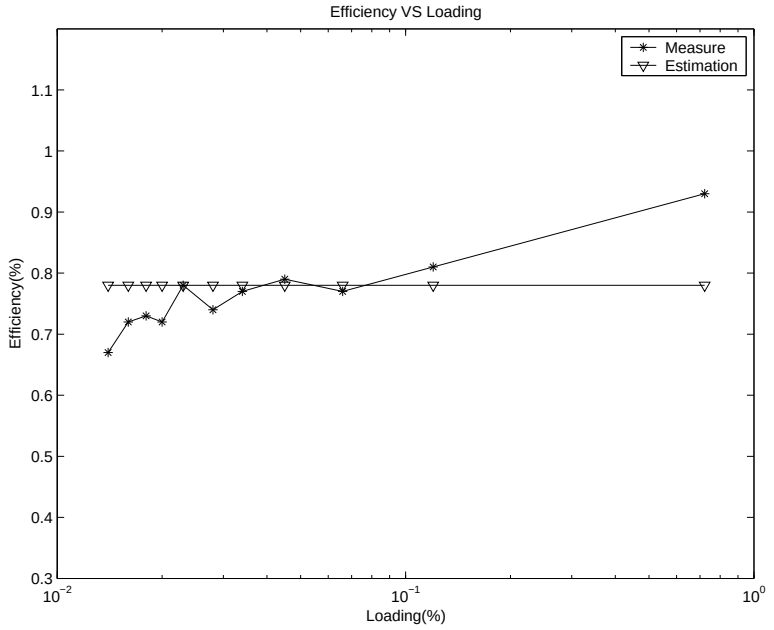

Figure 8: Efficiency versus loading in PFM.

3.3 Stacked buck DC-DC converters

3.3.1 Output voltage ripple

3.3.2 Power efficiency

3.3.3 Test cases

The first test case is to use a two-level stacked DC-DC converter to drive inverter chians. The schematic of this test case is shown in Fig. 9

Spice results shown that the loading power is 0.288W, power efficiency is 86which is around $20mm^2$.

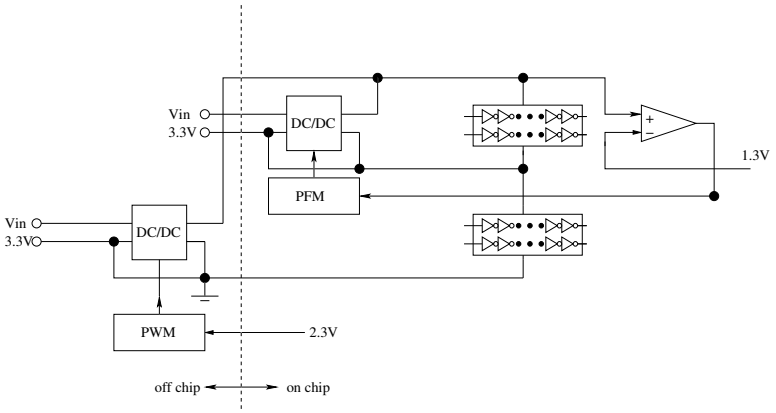

Figure 9: Two-level Stacked DC/DC with inverter chian as loading.

References

[1] G. Schrom, P. Hazucha, J.-H. Hahn, V. Kursun, D. Gardner, S. Narendra, T. Karnik, and V. De, "Feasibility of monolithic and 3d-stacked dc-dc converters for microprocessors in 90nm technology generation," in *Low Power Electronics and Design, 2004. ISLPED '04. Proceedings of the 2004 International Symposium on*, 2004, pp. pp. 619–626.

[2] A. Stratakos, S. Sanders, and R. Brodersen, "A low-voltage cmos dc-dc converter for a portable battery-operated system," in *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, June 20-25, 1994, pp. pp. 619–626.

[3] V. Kursun, S. Narendra, V. De, and E. Friedman, "Analysis of buck converters for on-chip integration with a dual supply voltage microprocessor," vol. 11, no. 3, pp. 514 – 522, June 2003.