Report on the Stack Power Supply Project

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1 Introduction

This report summarizes the most updated progress of the stacked power supply project. The first purpose of this report is to serve as a snapshot for the current status of the stacked power supply project. It is believed that the current status of the prototype of the stacked power supply is in a good shape and ready to start physical layout design without major modifications. However, iterations between physical design and prototype design may be needed in order to ensure the correct function of a test chip.

The second purpose of this report is to serve as a documentation on current designs which may help consecutive students to understand, improve, and fulfill the final goal of this project. For this purpose, the design is explained in as much details as possible and design guidelines are presented.

The detailed statement and background of the stacked power supply project could be found in [1] Chapter 4 and 5. This report is mainly about technical details. In essence, the stacked power supply is a new power supply design that is able to provide multiple supply voltage domains where each of them could be adjusted during run-time. One possible application of this new design of power supply is to employ run-time dynamic voltage scaling to reduce the power consumption of a chip. In addition, this power supply has some other advantages such as reduced input current. The DC/DC conversion method developed in this project could also be used independently for other purposes.

In the rest of this report, this report will present the details of the PWM and PFM DC/DC converter that are used in the stacked power supply in Section 2.1 and 3, respectively, with experiment results included. The details and experiment results of the whole stacked power supply will be presented in Section 4.1.

2 The PWM DC/DC converter

2.1 The schematics

The schematic of the PWM DC/DC converter with parasitic resistance, inductance and capacitance is shown in Fig. 1. The parasitic parameters are based on the Pentium pro model presented in [2]. Note that the frequency of the PWM is as large as 5 times of the VRM presented in [2] and the output inductor and capacitor of the LC filter are 10 times smaller than the VRM in [2]. Also, the Q factor of the output inductor is in a reasonable range. A commercial productor such as the power inductor in [3] could provide up to $500nH$ inductor at 2MHz operating frequency with DC resistance of $0.47m\omega$. Please refer to Section 2.2 for the discussion on the frequency of the PWM.

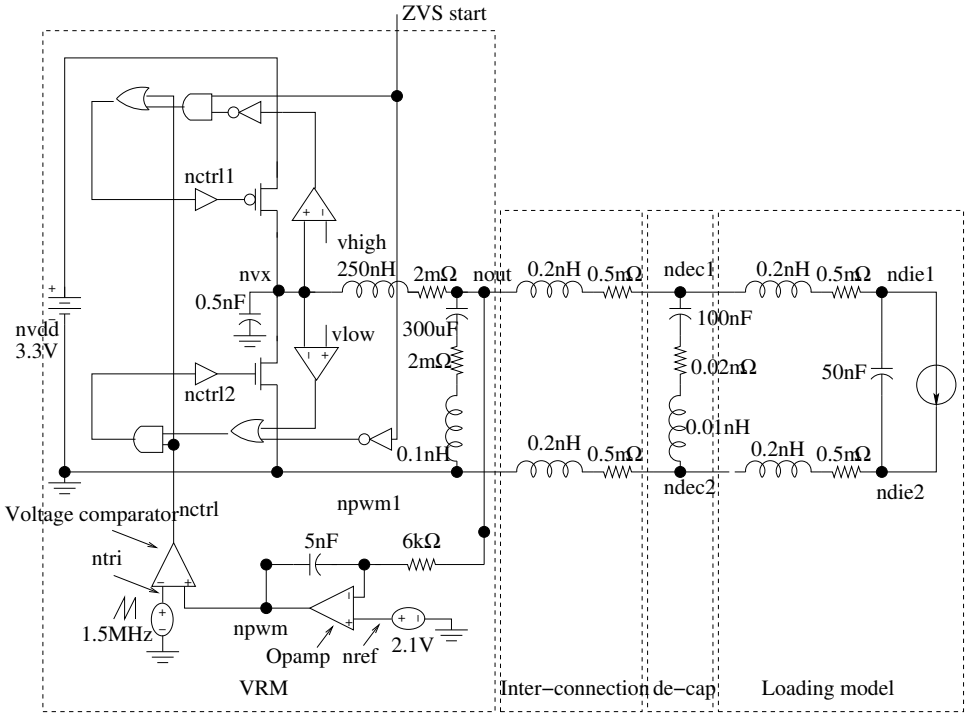

Figure 1: The PWM design with parasitic resistance, inductance and capacitance.

This PWM DC/DC converter follows the traditional design with an additional feature of automatic zero voltage switching, which is realized by a feedback loop to check if the voltage level of V_{nvx} satisfies zero voltage switching conditions and then decides to open/close the power transistors. For discussion on the principle of automatic zero voltage switching please refer [1].

The schematic of the voltage comparator used to generate the pulse signals that control the open and close of the power transistors is show in Fig. 2. This design is adopted from [4]. The good thing about this

comparator is that the frequency of the comparator could be very high. Actually the high frequency of this voltage comparator is crucial for correct operation of the whole PWM DC/DC converter. The opamp used for the RC integrator is a simple 2 stage design, which could be found from most Analog design textbooks.

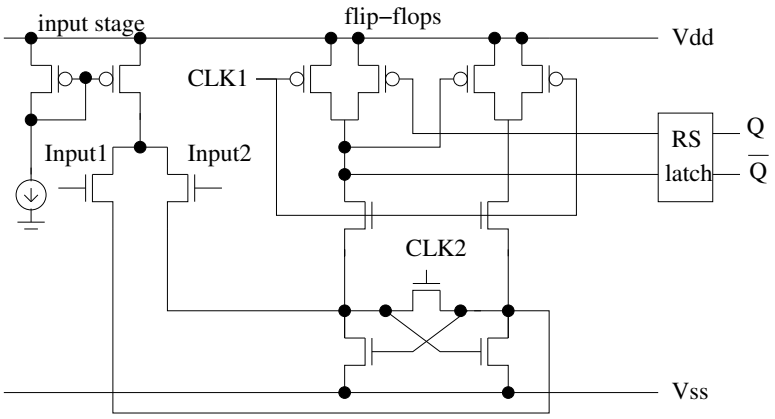

Figure 2: The voltage comparator.

2.2 Design considerations

2.2.1 Operating frequency of the PWM

The operating frequency of the PWM DC/DC converter determines the size of the LC filter, which is the most area consuming part of the converter. The size of the output inductor and capacitor has a rough linear relationship with the operating frequency. In traditional PWM DC/DC converters, the operating frequency of the PWM is around several kHz to several hundred kHz, which leads to a large size of the output capacitor and inductor. For example, in [2], the operating frequency of the PWM is 300kHz, and the output capacitor and inductor are $3.28mF$ and $2.0\mu H$, respectively.

There are some works trying to increase the operating frequency of the converter and thus reduce the size of the LC filter. For example in [5], a frequency as high as 477 MHz has been adopted and the output capacitance is 100nF, which is small enough to be integrated into the chip. However, a opened loop design is employed in [5]. In a closed loop design, such a high frequency could induce a huge output voltage ripple which may cause the converter to be unusable.

Assuming that the PWM operating frequency and the frequency of the voltage comparator that generates the pulse control signals to turn on/off the power transistors is f_{pwm} and f_{vc}. To ensure that the output ripple is less than X, we have

$$\frac{f_{pwm}}{f_{vc}} < X, \tag{1}$$

where $\frac{1}{f_{vc}}$ represents the smallest possible duty cycle change to the pulse control signal. Assuming $f_{pwm} = 477M$ and $X = 0.02$, we have $f_{vc} = 23.8GHz$, which is impossible. Assuming $f_{vc} = 1GHz$, we get the maximum operating frequency of the PWM to be $20MHz$. However, in reality, the actual frequency is smaller than $20MHz$. In our current design, this frequency is around $1 - 2MHz$. It is believed that with a careful design the operation frequency could go higher but should be less than $50MHz$, which is corresponding to an output inductor of $15nH$ to $1.5nH$, and an output capacitor of $20uF$ to $2uF$.

2.2.2 Outer feedback loop

Adjusting the values of the resistor and capacitor of the RC integrator is an effective way to adjust the closed loop gain of the outer feedback loop. As shown in Fig. 1, we have

$$v_{npwm} = -\frac{1}{RC}\int v_{out}dt, \tag{2}$$

where v_{npwm} controls the duty ratio of the control signals to the power transistors. To ensure that there is no oscillation in the outer feedback loop, RC has to be set big. However, a big RC value reduces the tracking speed of the converter. Therefore, there is a tradeoff between the tracking speed of the converter and the stability of the outer loop, which is controlled by the RC value of the integrator. In current design, the RC value has been set to have a similar frequency of the LC filter, which is a good tradeoff between tracking speed and stability.

2.2.3 Inner feedback loop

There is one condition to ensure the correct function of the adaptive ZVS technique which is implemented by the inner feedback loop: the current flowing over the output inductor can not be in one direction in one cycle. It has to switch directions during one cycle. Otherwise both power transistors would be turned off by the adaptive ZVS circuitry and the correct status of the circuit can not be recovered unless adopt some additional recovery circuitry.

The reason is that once the adaptive ZVS starts, the opening of the power transistors depends on v_{nvx}, which requires a positive-direction current (from output inductor to capacitor) to change it from high to low and a negative-direction current (from output capacitor to inductor) to change it from low to high. If the current is uni-direction, either one would fail and eventually v_{nvx} stay at the voltage level of v_{out} and both power transistors would be turned off. It is not hard to see that once the current is bi-direction, adaptive ZVS would be guaranteed to correct function.

There are several possible ways to cause the current to be uni-direction in one cycle: (1) the output inductor is too big which causes a small ripple of the current. (2) There is a low-frequency ripple in output voltage level and the current. If this is because the outer loop hasn't been stabilized yet, make sure that the

adaptive ZVS circuitry starts after the outer loop stabilized. If this is because there is a oscillation in the outer loop, make sure that the RC value in the integrator is big enough to eliminate oscillation.

2.3 Experiment results

The schematic in Fig. 1 has been simulated by HSPICE and the measure results show that the overall power efficiency is 85% and the output ripple is 2%. Fig. 3 shows the output voltage level of the PWM DC/DC converter where the reference voltage level is set to be 2.1 Volt. It can be seen from the figure that the output voltage level settle to 2.1 Volt with a small ripple (2%) after a startup period around $200\mu S$. Fig. 4 shows the total power consumption of the converter. It is clear that the the adaptive ZVS has significantly reduced the total power consumption of the converter. Note that the loading power almost keeps the same before and after turn on adaptive ZVS. Fig. 5 shows the details of the control signals of the power transistors versus V_{nvx}. From this figure we can see that zero voltage switch is always ensured.

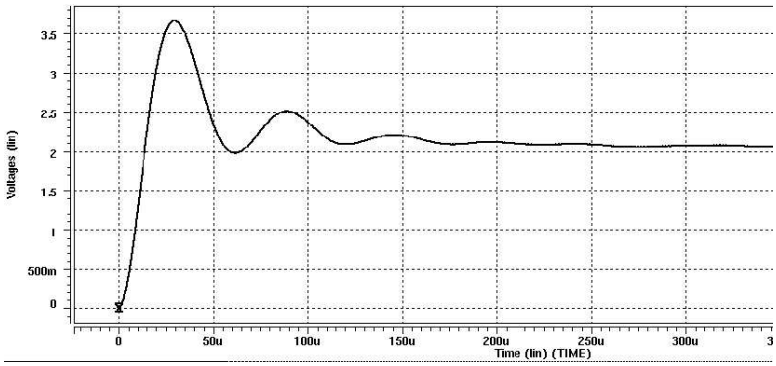

Figure 3: Output voltage.

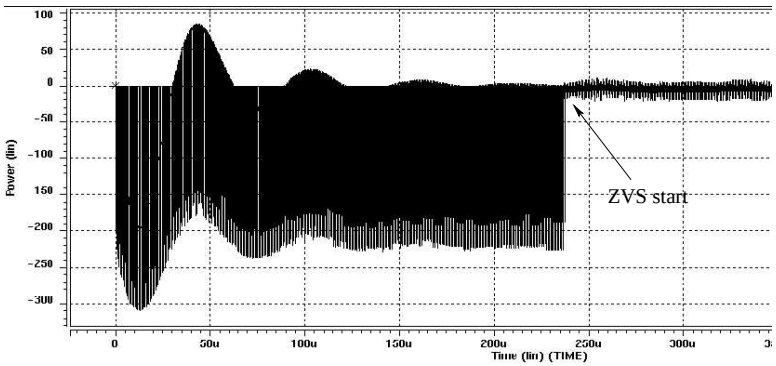

Figure 4: Total power consumption of the converter.

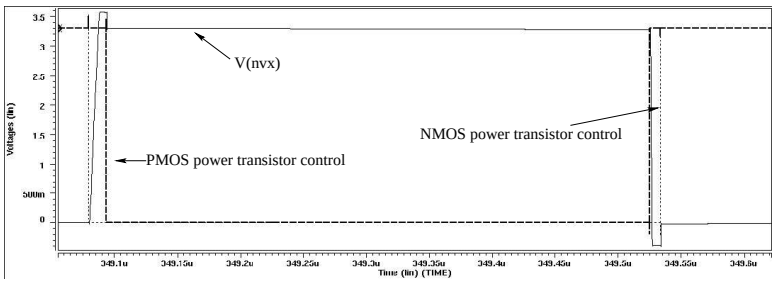

Figure 5: The control signals for power transistors versus voltage of nvx.

3 the PFM DC/DC converter

The schematic of the PFM DC/DC converter is shown in Fig. 6. This design has been adopted in [6] particularly for the cases that loading is light. In this PFM DC/DC converter, the power transistors open only when the output voltage level is smaller than a reference voltage level. When the loading is heavy, the frequency to open the power transistors is high, and when the loading is light, the frequency is pretty low. Because the power loss is associated with each switches of the power transistors, the PFM converter can maintain a relative high power efficiency when the loading is light.

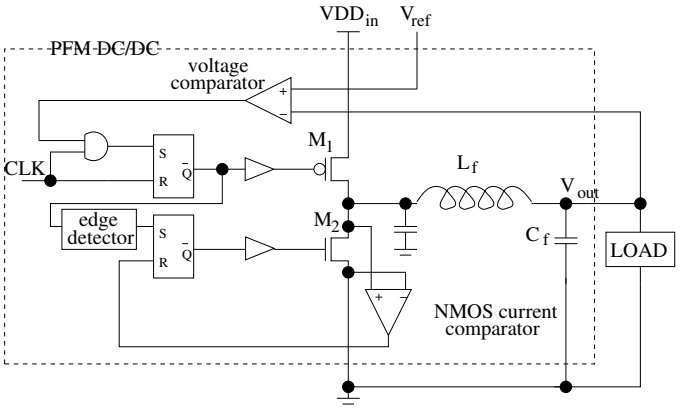

Figure 6: The PFM design.

To ensure a relatively high power supply ability, the opening time of the PMOS power transistor is expected to be long. However, a long opening time of the PMOS power transistor leads to a high output voltage ripple. A good way to achieve a high power supply ability and a low output voltage ripple is to adopt a multi-phase design. The concept of multi-phase design has been used in other DC/DC converters ,such as the hysteretic DC/DC converter in [7]. The schematic of a multi-phase PFM DC/DC converter is shown in Fig. 7. Note that a D flip-flop has been used to buff the enable signal to avoid incomplete turning on of the PMOS power transistor, which sometimes may cause malfunction of the whole converter.

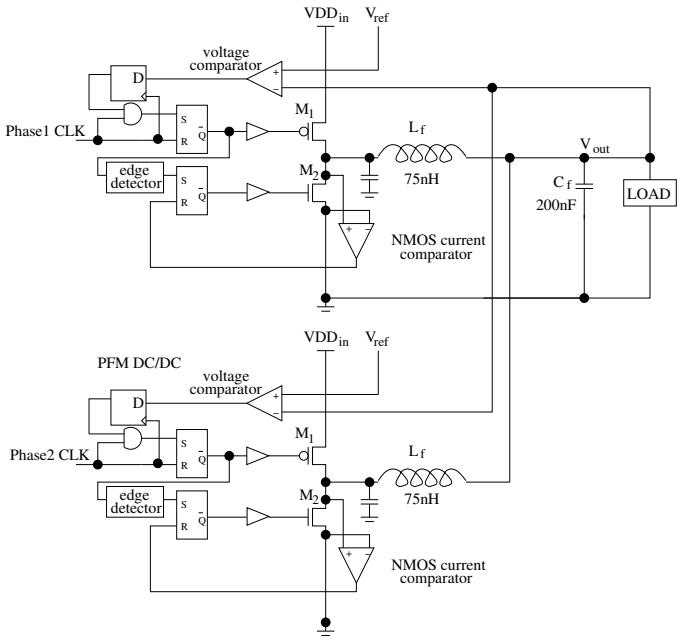

Figure 7: The multiphase PFM design.

3.1 Design considerations

3.1.1 Opening time and output inductance

The most important parameters in the PFM DC/DC converter design is the opening time of the PMOS transistors and the value of the output inductance. Together with the output inductance, the opening time of the PMOS power transistor determines the current going through the output inductance and these current is injected into the output capacitance to maintain the output voltage level. If this current is too big, the output capacitor will be charged by too large amount which leads to a high output ripple. To lower this current, a larger inductor or a smaller opening time of the power transistors need to be adopted. However, when the open time of the power transistor is too small, the NMOS power transistor can not be closed quickly which may degrade the power efficiency. Therefore, the best case is to take a high output inductor and a large opening time. Under current experiment setting, the opening time of the PMOS power transistors is assumed to be $18nS$ and the output inductor is 75nH to be put off-chip.

3.1.2 Phases of individual PFMs

The phases of the two PFMs has been taken as 0 and π. This setting has shown a good results in the experiments. It is not sure to what extend a different phase setting would affect the output voltage ripple. It's even a more interesting problem to study a design with multiple phase PFMs and the phase of each

individual PFM is random. It is believed that this study would find applications in a extremely distributed multi-phase PFM designs.

3.2 Experiment results

The multi-phase PFM DC/DC converter in Fig. 7 has been simulated and the results show that a power efficiency of 92.4% and an output voltage ripple of 2.8% has been observed. Shown in Fig. 8 is the output waveform of the PFM DC/DC converter.

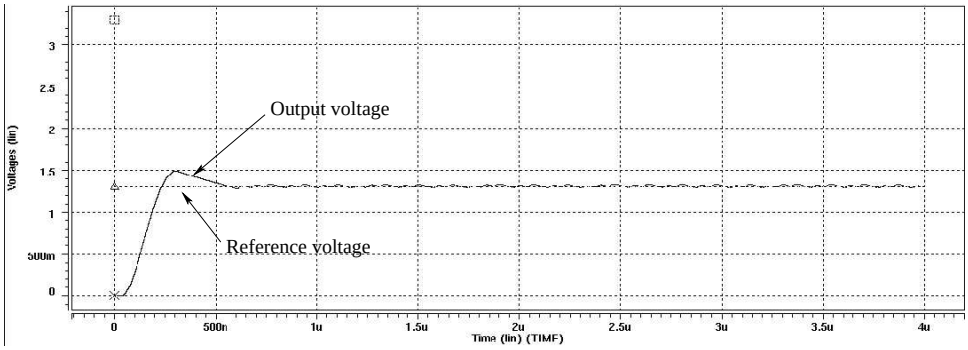

Figure 8: The experiment results of the multiple phase PFM.

4 the Stacked Power Supply

4.1 Schematics

The schematic of a 2-level stacked power supply is shown in Fig. 9. As shown in the figure, the stacked power supply includes an off-chip PWM DC/DC converter and an on-chip two-phase PFM DC/DC converter. The loading circuit modules are stacked instead of parallel connected as in conventional power supply system.

The off-chip PWM DC/DC converter has a large LC filter which supplies the majority of the power to the loading while the duty of on-chip PFM converters are used to quickly supply charges to the loading and stabilize the voltage level of the loading. The output voltage level of the on-chip PFM can be quickly changed which changes the supply voltage levels of the loadings and thus achieves run-time dynamic voltage scaling.

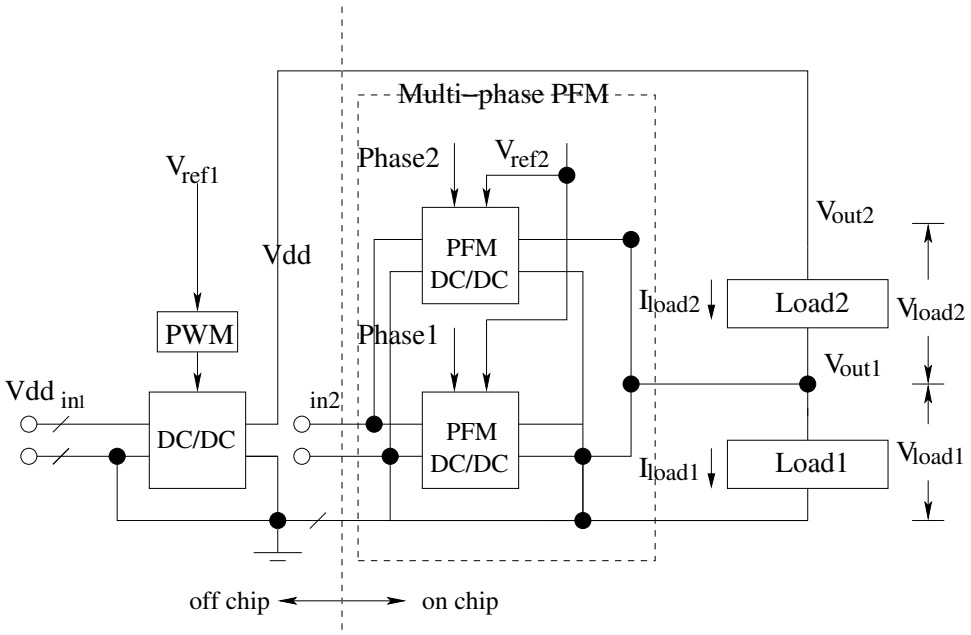

Figure 9: The overall 2-level stacked power supply design.

4.1.1 Experiment results

Fig. 10 shows the experiment results of the stacked power supply system where the reference voltage level of the PFM DC/DC converter is set to be 1.3 Volt, and the output voltage level of the PWM DC/DC converter is assumed to be 2.1 Volt. The measurement results show that the overall power efficiency of the whole system is 81%. The output voltage ripple of the PFM is 2.8%. Because the output voltage ripple of the PWM converter is 2.0%, the maximum voltage ripple on loadings is less than 5.0%.

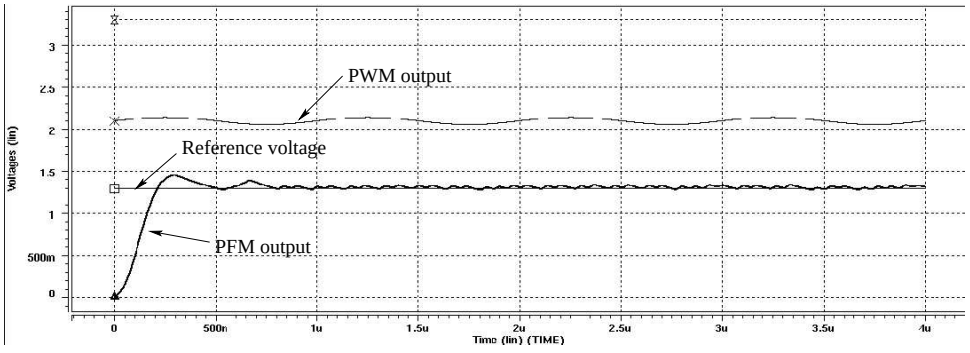

Figure 10: The output voltage waveforms of the stacked power supply.

Fig. 11 shows the output voltage waveforms for run-time dynamic voltage scaling. During the simulation, the reference voltage level of the PFM converter has been changed from 1.2 Volt to 1.5 Volt, which

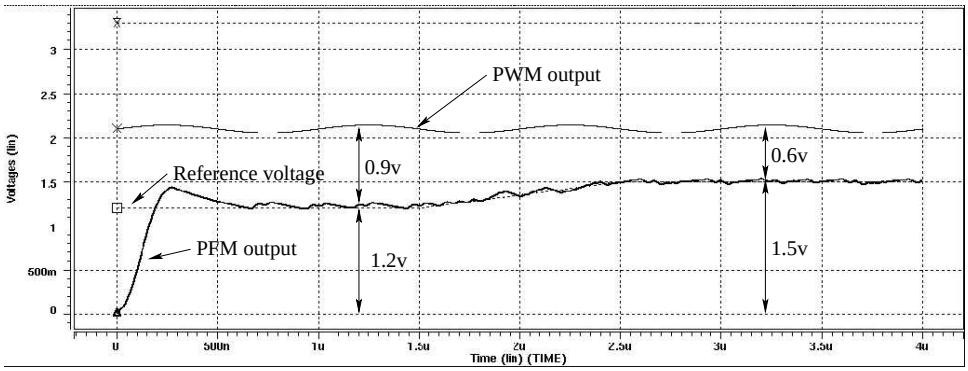

Figure 11: Runtime dynamic voltage scaling of the stacked power supply.

changes the voltage levels of the two loading accordingly. As we can see from the waveform, the output voltage level of the PFM tracks the reference voltage level quickly and precisely[1].

References

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[1]The transition has been finished within $1\mu S$.