Challenges of a Unified Approach to Complex System Packaging

Abstract

In 2004, consumer electronics became the largest slice of the electronic industry pie. Consumer applications, though, demand an ever increasing integration of very different silicon process technologies to meet their performance (power, clock), size and cost targets.

New packaging techniques are needed, such as Multi-Chip Modules (MCM) and System in Package (SiP), in order to develop each component of the application in its native process technology. It is then a matter of integrating them all, combined with the required active and passives components, into a single package.

This has had a dramatic impact on the EDA industry, which is too IC-centric. Schematic and layout editors must work in a 3D world while extraction and simulation tools must handle ICs, their packages and many diverse passive components simultaneously, also taking into account the board effect.

To solve this challenge, a brand new IC/package/board co-design and co-verification methodology, based on open standards, is required to address the intricacies of SiP.

1. Introduction

In September 2005, the two billionth worldwide mobile phone subscription was celebrated and the current forecast is that there will be three billion subscribers by 2010. This is possibly the largest market segment for the electronic industry today. Cost considerations, rules and all the players – from OEMs such as Nokia, Motorola and Samsung, to IDMs such as TI, Qualcomm and ST – are striving to reduce their cost in order to address the broadest possible customer base.

Although technologically feasible, a System-on-Chip (SoC) design at 65 nm or below is becoming economically unreasonable. Cost of fabrications, masks, poor yield, power and thermal limits and several other factors are playing against SoC. Mixing the necessary device technologies – logic CMOS, Analog and RF, DRAM, SRAM, FLASH, embedded memories – requires a large number of masks, bringing NRE (non recurring engineering) costs to a multi-million dollar level. Moreover, the poor integration of passive devices makes the term SoC itself an overstatement as no system is possible today without passive components. Mobile phones typically contain more than 50 passive components for each IC – there are more than 200 and only a handful of ICs.

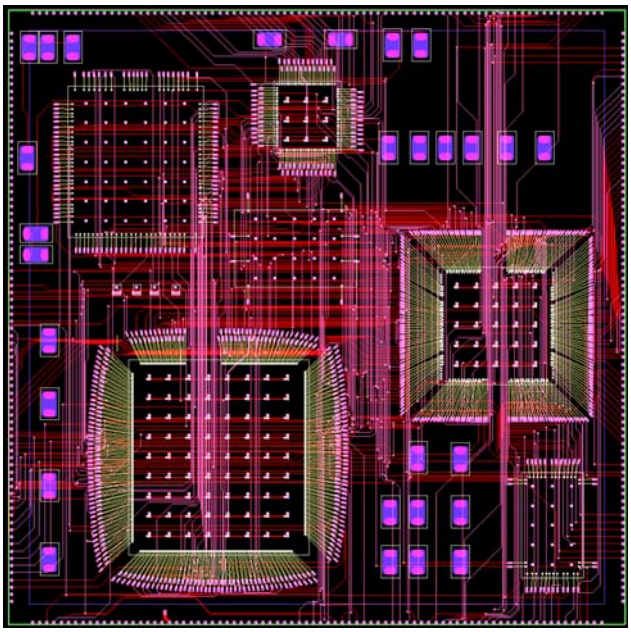

Figure 1: System-in-Package substrate design.

These challenges are driving the evolution of SoC into SiP. This trend is further accelerated by the technical difficulties of keeping the pace in the rush towards the atomic limits of Moore's Law.

2. Packaging Technology Evolution

In recent years, major innovations have occurred in packaging technology[1], which have led to the industrialization of several kinds of new packages – more powerful and more flexible – in the attempt to cope with the challenges posed by multi-million gates and multi-GHz SoCs. These designs demand higher integration, resulting in high packaging pin counts and density. High frequency designs require complicated flip-chip technologies to avoid the high inductance of wire bonding.

According to the latest update of the International Technology Roadmap for Semiconductors (ITRS 2004), at 65 nanometers a 500 million gate ASIC, with 4,400

pads and running at 10GHz, must be packaged in a giant, and yet very expensive ($1.61 /pin) flip-chip BGA, with 4,000 pins[2].

In contrast to the costly SoC, packaging technologies are evolving into SiP to keep up with the need for "smaller, faster, cheaper" products. Within one single package, multiple wire bonded or flip-chip ICs are integrated on a common substrate, including several passives – such as IPAD (Integration of Active and Passive Devices), SMD, and embedded passives – not achievable in IC technology. The ability to drastically simplify board-level design complexity by integrating large numbers of discrete elements into the interconnection structure as embedded components is one of the strongest points of the SiP approach.

Mixed signal communication products, such as mobile phones, require the digital, analog and RF portions of the design to work reliably and in close proximity to each other. This means a number of passives in both the analog and RF design sections, and integration leads to a substantial size reduction and performance improvements, solving issues such as signal noise, crosstalk, ground bounce etc.

The higher integration capacity of SiP reduces the number of components in the system, thus reducing both the size and the routing complexity of the printed circuit board (PCB). Eventually, the package forms a functional module that can be used as a standard component in board level manufacturing.

3. SiP Architecture: An Opportunity and a Challenge

3.1. The MCM Story

MCM is not a new concept. It has existed for many years in the computer and telecom industries, even if it was limited to expensive high end applications, driven by performance requirements. Today, after the extreme reduction of package size to Chip Scale Package (CSP) it is used for very high volume applications, where cost and real estate are the key drivers.

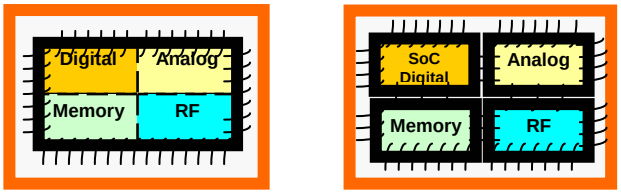

Figure 2: Evolution from SoC architecture into MCM architecture.

Partitioning of the SoC has led to a new design architecture, where all the modules can be designed in the most appropriate technology, and then placed and connected in the same package substrate. In addition, the designer selects IP components – logic, memory, analog, optimized cost ICs – from multiple sources that are optimized to minimize manufacturing costs and also to help shorten development time.

There are several advantages to this approach:

- 3-4 metal layer savings in stand alone SRAM memory vs. 'route over' layers required in embedded memory
- The memory portion of design is not burdened with defects in the logic portion which are not repairable
- Tester costs vastly reduced because a less expensive memory tester can be utilized
- The logic portion of the system is not 'sitting in test' while analog and special functions are tested

A higher level of integration is offered by stacking dice. A stacked die substrate has two basic structures, shown in figure 3.

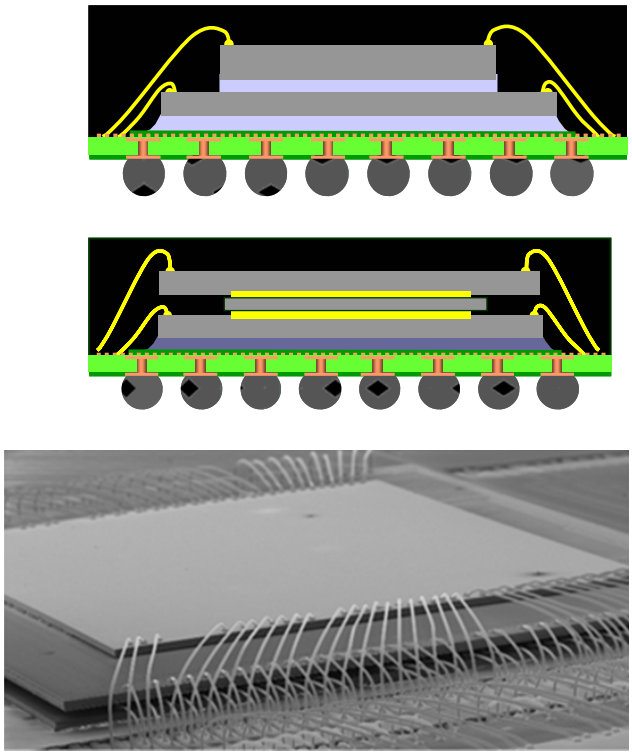

Figure 3: Multiple die stacking enables higher electrical performance through shorter interconnect architectures. The basic structures, from top to bottom are Pyramidal, Twin and a combination of them.

Interconnection can be realized with flip chip as well as wire bonding technologies[3], providing all the necessary die-to-substrate and die-to-die connections.

The stacked die BGA technological evolution is showing that the number of die is ever increasing – from four stacks in 2002 up to eight stacks in 2004 – while the package thickness is increasing only from 1.4mm for 4 stacks up to 1.6 mm for 8. The integration offered by the bigger stacked approach 8+7 BGA (8 stacks with 7 interposers) is 4.5 years faster than Moore's Law.

3.2. New Multi-Dimensional Integration

The 'real' SiP architecture is not only a MCM or a stacked die CSP but a combination of the two. After an intelligent partitioning of the system, the diverse functions can be placed in the package substrate side-by-side or in a stacked fashion with the appropriate interposer. They are then properly connected with wire bonding and/or direct chip attachment.

Wire bonding can be used to connect die-to-die and/or die-to-substrate, linear and/or staggered pads using a standard or a reverse bonding technology, even with tri-tier package configurations.

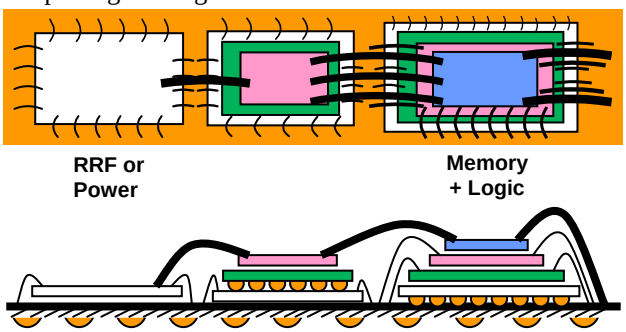

Figure 4: Multiple system or sub-system functions integrated in one single module, with wire bonding and/or direct chip attachment.

While offering a great deal of opportunities, complex SiP substrate design and verification requires an unprecedented level of integration between ICs and the package, along the lines of what has happened when logic synthesis and place-and-route merged into physical synthesis. The package is not only just a package anymore. Multiple ICs and a large number of passive components, such as resistors, capacitors and inductors, active devices such as ESD protection diodes, all into a single substrate, make the package substrate itself 'a system' that must be effectively co-designed and co-verified, to alleviate the burden and yet reducing the cost.

3.3. A Complex IC-Package Interface

The complexity of today's systems or sub-systems, combined with their high pin count and performance requirements, results in a more complex silicon-package interface than with traditional devices. Unfortunately, today's design methodologies result in a segregated relationship between IC and package design, making coordinated planning a difficult and time-consuming task.

The serial nature of the traditional silicon to package design flow limits the effectiveness of existing tools for concurrent planning. Both IC and package design tools lack the needed visibility into their respective environments. This serial approach may lead to a poor IC to package netlist, resulting in longer cycle times and sometimes preventing the co-verification of the entire system.

New methodologies and new tools are becoming a must in order to facilitate coordinated planning and sharing of data across the two domains of silicon and package. Having coordinated planning during the early stages of silicon floor-planning can result in an optimized silicon/package interface and in the process, lowering cost, reducing cycle-time and enhancing overall device performance.

4. Interface Planning

A multidisciplinary team cooperates to execute the SiP planning. SiP designers have to solve several optimization problems, including system I/O requirements, thermal and signal integrity constraints, die placement and orientation, stacking configurations, package substrate and interposer design, interconnect design, at IC plus package level, also taking into account the customers' constraints on the PCB.

4.1. A 3-Dimensional Problem

A new class of algorithms, with the ability to work in a 3D world not only limited to interconnects, must be available to properly place all the components of the system (not simply 'surface mounted' on the package) and to properly plan the interface between all the elements.

Moving from the 'planar' placement to the 3D one, the most appropriate stacking order must be decided, taking into account several constraints. The 3D placement algorithm should be automatically able to:

- Consider if an interposer, to properly separate two dice, is required, and if so, compute its dimension and thickness
- Prevent die stacking exceeding the maximum overhang value to avoid the risk of silicon-breaking during the wire bonding phase
- Prevent stacking configurations causing overall undesirable 'warpage' effects
- Comply with the wire looping manufacturing capabilities, making sure that the standard or reverse wire bonding of choice does not hit the next level die
- Adjust die orientations, for memories or IPs owning 'frozen' physical I/O locations, to locally optimize the periphery interface

4.2. Floor-planning of Heterogeneous Objects

Once the stacked parts are built, the complete floor-planning and placement of all the heterogeneous SiP elements must be realized. To properly manage power and ground signals, busses, high speed signals, differential pairs and off-chip distribution of very high-speed clocks, the overall physical periphery relationships, as well as all the electrical constraints, must be taken into account.

Bottom-up floor-planning (I/O placement of memories, Application Specific Standard Products

(ASSP) and IPs) is fixed and the physical data easily readable from standard formats like GDSII or LEF/DEF.

Top-down floor-planning (driven by signal assignment on the board and the package and by interconnection proximity with neighboring ICs) I/O placement can be created from scratch or incrementally from a pre-populated one, to provide place and route tools with a starting I/O placement seed.

Of course, SiP demands a combination of top-down and bottom-up – a more complex co-design process. Depending on the specific function, one or the other approach applies to obtain a global I/O configuration which, in conjunction with the customer's board assignment, may result in a routable netlist for the package[4].

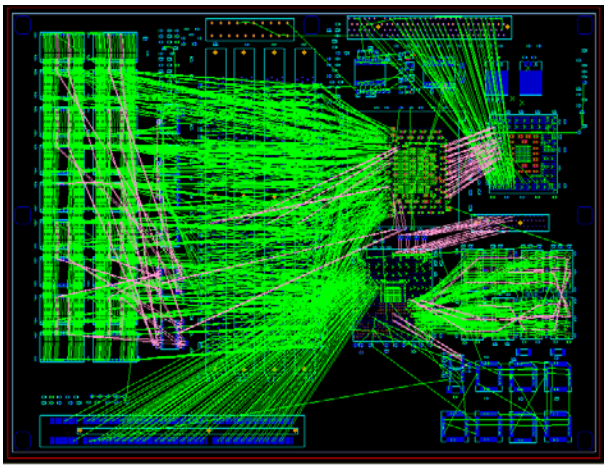

Figure 5: Global routing of a complex SiP substrate design.

Today, the vast majority of ICs are designed with peripheral I/O pads, linear, staggered, even mixed, and their placement is driven by both layout and wire-bonding constraints. An additional level of complexity is introduced by the use of flip-chip technology. With smaller pads/pitch, I/O placement may change from peripheral to area array, with the introduction of additional wafer processing covering 'redistribution' of the bond pads.

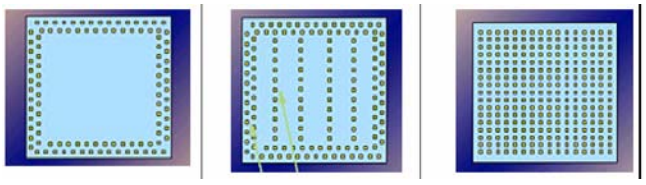

Figure 6: I/O pad configuration including: peripheral (left), peripheral + area (center), full area (right).

4.3. DRC and LVS

Once definitive physical information is available, a large variety of geometrical and electrical rules must be checked for sign-off purposes.

Even if DRC (design rule check) techniques at IC, package and board level are well consolidated, these hybrid configurations require a bottom-up extension of the IC level solution or a top-down extension of the board one.

Besides standard rules, to guarantee a full compliance to manufacturing, assembly and testing, user definable rules could be necessary, utilizing a scripting language.

LVS (layout v. schematic) technique must also be upgraded, in order to be applied on the complete SiP design. The signal to package/board assignment must be compared against the pad/bump assignment.

5. System Verification

To achieve optimum results, a unified 3D 'Super-Environment' is required. It must be able to read and write a top-level hierarchical netlist of all the heterogeneous pieces (ICs {digital and analog}, package, board) and to merge them all, even if coming from different design environments. It must also be able to compose schematics and generate the complete models.

Power and timing requirements amplify the effects of parasitics on the overall system. Extraction of IC parasitics, wire bonding or redistribution layer parasitics, and package substrate routing parasitics must be assembled for electrical characterization purposes and to detect signal integrity (simultaneous switching noise/cross-talk/timing) and power integrity (voltage drop and dynamic voltage drop) issues early.

6. Conclusions

A revolution is taking place in the marketplace, driven by high volume applications with fast innovation and a large variety of new options. The integration roadmap defined by Moore's Law and ruling SoC is no longer sufficient.

Packaging technology can integrate a number of heterogeneous functions in the same device. SiP is a modular design approach offering unprecedented flexibility in the development of systems. An intelligent partitioning of all the components of the electronic system is key to achieving greater functionality in a smaller area, combining dissimilar device types and high-yielding memory devices with similar size and wiring requirements.

A multi-disciplinary team has to execute the SiP design and verification, in order to solve the overall system optimization problems thus achieving all the requirements.

Design technology must be enhanced for SiP to be successful. A new class of tools must be conceived and developed at the interface of the three worlds – board, package and IC – and be able to understand all the languages and constraints while translating the relevant information and merging the results into a single whole.

8. References

[1] John H. Lau, *BGA Technology*, McGraw-Hill, Inc., 1995.

[2] *The International Technology Roadmap for Semiconductors, 2004*; www.itrs.com.

[3] George Harmon, *Wire Bonding in Microelectronics*, Second Edition, McGraw Hill, 1997.

[4] Takahiro Oka, *System-In-a-Package Stacked Flash Memory and Logic LSI*, Semicon Japan, 2000.

[5] Y. Fukui et al., *Triple-Chip Stacked CSP*, 50th Electronic Components & Technology Conference, 2000.

[6] Y. Yano et al., *Three-dimensional Very Thin Stacked Packaging Technology for SiP*, 52nd Electronic Components & Technology Conference, 2002.