# Design automation for RFSiP applications


## ABSTRACT
SiP solutions are fast growing while efficient design tools are still lacking. The footprint flow has been developed in the aim to allow multi technology design in Cadence environment. Its role is to collect information of the active die and to organize it to enable co-electrical simulation and complete Layout Versus Schematic (LVS) checks of both passive and active dies. The flow capabilities are presented and illustrated on a single example.



## Categories and Subject Descriptors
B.7.2 [**Integrated circuits**]: Design Aids – *layout, placement and routing, simulation, verification*; D.2.2 [**Software engineering**]: Design Tools and Techniques – *flow charts, object-oriented design methods.*

## General Terms
Design, Verification.

## Keywords
RFSiP, Design, Flow, Simulation, Verification.


## 1. INTRODUCTION
With the continuous growth of various wireless applications, there is an ever-increasing demand for electronic systems with more functionality, higher performance, smaller size and lower cost. In this context, Radio Frequency System-in-Package (RFSiP) products have developed rapidly in last years as an alternative to System-on-Chip (SoC). RFSiP is a powerful technology platform enabling the integration of digital and radio frequency integrated circuits (RFICs) into a single package. Thanks to reduced interconnections between ICs compared to standard Printed Circuit Board (PCB) solutions, SiP provides better RF performances.

Whereas classical designs only deal with one technology, SiP is a combination of several chips, active and passive, from different technologies. So it requires multi technology co-design tools that are not currently available. Indeed, when designing a passive die, designers need to get information from the active one (location of passivation shape, connectivity information…). The flow that has been developed guaranty enough robustness to work with several processes (i.e. design kits) at the same time.

This paper presents the general flow for multi technology co-design. The second chapter describes various SiP packaging technologies. In chapters 3 the generic flow for footprint creation is detailed for both input database format, DFII or GDSII. Chapter 4 illustrates the advantages of the flow, electrical co-simulation and LVS checks, on an application. Then an electrical model for bumps is proposed before concluding in chapter 5.

## 2. SIP PACKAGING TECHNOLOGIES
### 2.1 Interconnect technologies
Two methods are generally adopted to interconnect passive and active dies together: wire bonding method or bumping method. Wire bonding method uses gold wires to create the connection between the pads of different dies. Bumping is a method by which one chip is electrically connected to another one thanks to small metal balls. Although this process is more complicated than the previous one and its cost is higher, it allows the same package size as the chip size. Electrical RF performances are also much better since the interconnection length is smaller.

### 2.2 Assembly methods
There are generally two types of dies assembly: one is a planar type and the other is a stacked type. Both use either bond wires or bumps interconnection.

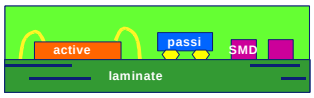
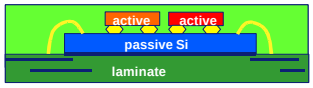
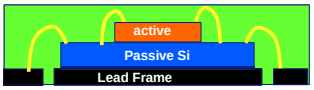
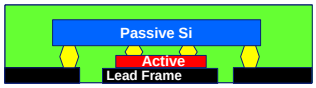
With the planar type each die is directly connected to a carrier (laminate, lead frame…) and the package size is relatively large. On another hand, the stack type can realize small packaging size. But when using wire-bonding connections, this method is influenced on the size of each upper and lower die, since it is difficult if two chips are almost the same size. On the contrary, flip chip attachment is not influenced on the chip sizes and can make package size smaller than wire bonding method. Table 1 presents some configurations examples for each type.

This table is not meant to be exhaustive and one can imagine many other configurations but these are the most commonly used. From the cross section views presented in the table it is possible to distinguish between two different types of interconnections:

- First level interconnections that connect dies together to form the stack.
- Second level interconnections that connect the whole stack to the carrier.

First interconnect elements are far smaller than second interconnect ones. For instance the height of a bump is respectively about 30µm and 150µm for first and second interconnect.

**Table 1. SiP packaging technologies**

| | Assembly technique | Cross section |
|---|---|---|
| Planar Type | Flip-Chip + Wire Bonding |   |
| Stack Type | Flip-Chip + Wire Bonding |   |
| | Wire Bonding |   |
| | Double Flip-Chip |   |

General considerations about SiP processes as well as the break through it represents are described in [1] and [2]. Another advanced three-dimensional stacking assembly that is not discussed in this paper is the Wafer Level Packaging (WLP). In WLP the die and package are fabricated and tested on the wafer prior to singulation. This process eliminates many of the packaging steps required when using conventional packaging. This results in a drastic reduction in manufacturing cost and package size [3].

# 3. FLOW DESCRIPTION

## 3.1 General overview

The footprint flow is based on Cadence software design tools. This flow is used for assembly of stacked dies and it enables the design of the whole stack. This flow deals with any combination of technologies (passive and active) and has been developed to be compliant with both packaging technologies: bumping and bonding. Several Graphical User Interface (GUI) have been developed to enable a friendly use of the footprint routines. Although the classical database format is DFII, the flow can be performed on GDSII database inputs.

## 3.2 Flow using as input a Cadence database

In that case the flow is performed in four steps. It starts to be executed from the top cell of the active design that will be part of the stack. This top cell must contain clean and consistent schematic and layout views.

### *3.2.1 Step 1*

During this step a symbol view of the top cell of the active die is created, copied as identical as possible from the layout view, in such a way that pins placement is exactly the same. Simultaneously with the symbol view creation, the Component Description Format (CDF) file of the component is also created under the working directory and automatically loaded in the Cadence environment in order to provide correct information during future simulations or LVS comparison. This CDF takes into account all the terminals for different simulators (DRACULA, ASSURA, SPECTRE, ADS). The top cell is declared as a sub circuit to enable the correct netlisting of the whole active die in the analog simulators: Spectre and ADS.

### *3.2.2 Step 2*

This step checks the consistency of the schematic, layout and symbol views. It makes sure that all pins are present in the three views with identical names. A report is issued after running this step to point out possible discrepancies that may exist between the three views. If any, errors must be corrected and then it is necessary to go back to step 1.

### *3.2.3 Step 3*

During this step a ghost layout view is created (in a library that is technology independent) and a report file is issued that points out possible design's errors and warnings. It is possible to select the active design passivation layer and a positive or negative passivation drawing. The routine is able to settle on the exact position of contact pads from passivation layer openings, and this for both drawing types. This step takes also into account keep out areas. A keep out area is an area where no component should be placed in order to avoid sensitive configurations in the dies stack (for example two inductors being face to face).
The ghost view is created in Cadence generic layers to be technology independent. It can be modified during the flow: as a matter of fact user can modify the shape of keep out areas, remove some passivation shapes or pins depending on its own application.

The report file gives the list of pins and pads of the input design layout view and the list of errors and warnings of the design. For instance a passivation shape without pin is just a warning and is acceptable, but a pin outside a passivation shape will be reported as an error that needs to be corrected. Warnings are allowed so it is possible to resume the flow even if there are any. At the opposite, it is mandatory to correct each error before going further. Once it is done the user has to go back to step 2 in order to check that all is still consistent.

### *3.2.4 Step 4*

This is the last step of the flow during which the final active design views are built. At this step it is possible to take into account shrunk processes. In that case, GDSII file sent to the foundry is shrunk before mask making and then processed. So design is done with a different scale between database and mask. To take that into account a shrink factor is available in our routine. The user needs also to provide the saw lane width because the active die footprint must obey to strict packaging rules. At this step, the flow depends on the interconnect method chosen: bond wires or bumps.

### 3.2.4.1 *Case of bumps interconnections*

Two cells levels are built in a new created library. Both levels have layout, schematic and symbol view. Cell Level1 is of internal use only and contains the symbol of the active die. Then it is placed in a cell level2 and connected to active side of bumps. Bumps are then connected to pins in cell level2.

First level description:

Cell level1 is necessary to translate terminals of active die into passive process interconnect layer.

The active die symbol is instantiated in the first level schematic view. Each terminal of this symbol is connected to pins that have the same name.

The layout view is generated from the ghost view. Pins and keep out areas are translated into the passive design dedicated layers and utilities are added: fiducials, active die boundaries, date and time. Fiducials are alignment marks that facilitate chips placement during the assembly process [4]. The date and time make it possible to check that the footprint really represents the latest version of the active design. Furthermore, others features are provided for later checking of the footprint orientation.

The symbol view is used in the second level. It uses the same "picture" as the active die symbol. A CDF file containing all necessary simulation information is created and automatically loaded.

Second level description:

This cell level is built simultaneously with the first level and is the one that will be then instantiated in a passive design. It is fully compliant with Virtuoso XL.

The level1 symbol view is instantiated in the schematic view and each terminal of this symbol is connected to passive pins via bump components.

Cell level2 layout view is generated from the ghost view and cell level1 layout views. Bumps instances are automatically placed between pins of cell level1 and pins of cell level2.

Regarding the symbol view, a CDF file is created and automatically loaded.

### 3.2.4.2 *Case of bond wires interconnections*

In that case only one cell level is created in a library. This cell contains a layout, schematic, symbol and auLvs view.

The symbol of the active die can directly be instantiated in the passive design.

The active die symbol is instantiated in the schematic view and the auLvs view is used only for LVS netlisting (to perform comparison at top level only).

The layout view is generated from the ghost view. Pins are drawn using a CAD layer and the same utilities as for the bump flow are added (fiducials, active die boundaries, date). In the passive design layout view, bond wires have to be drawn manually with a CAD layer. This enables users to check the connectivity between the dies. For LVS checks, this wirebond CAD layer is treated as interconnect layer. A second CAD layer is also used to enable the connectivity check between top metal of passive process and CAD interconnect layer.

The flow methodology is summarized in the bloc diagram of figure 1 (in that case of a DFII format).

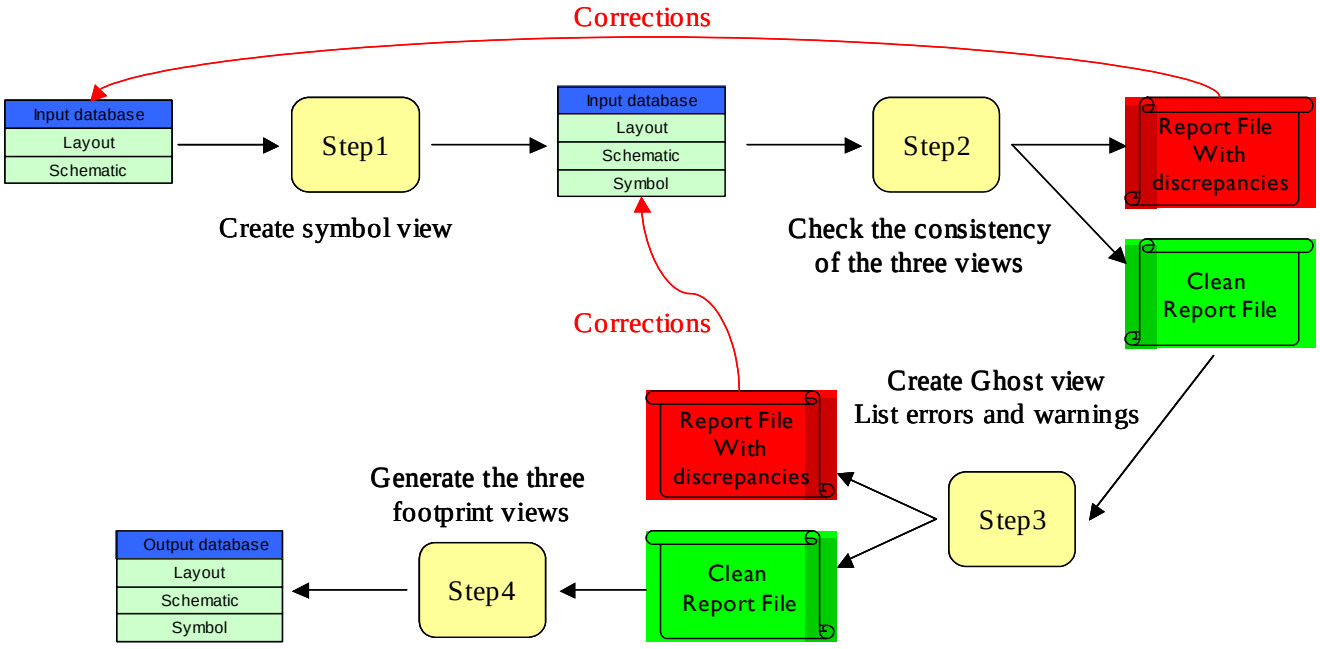



**Figure 1: Flow block diagram in case of a DFII database format**

## 3.3 Flow for a GDSII database

This flow is very useful in case of digital applications where a Cadence database is not available for the active IC. It has been successfully tested on very huge GDSII file (more than 330 staggered I/Os) using CMOS process. In the GDSII case, the flow doesn't enable electrical simulations but LVS comparison is still possible and packaging rules can be checked. It comprises only two steps.

### *3.3.1 Step 1*

During this step a ghost layout view is created together with a report file listing design's errors and warnings. The ghost view is built using generic cadence layers.

The flow takes Edtext and GDSII files as inputs. It is compliant with all formats of Edtext (ASSURA, DRACULA and CALIBRE). Furthermore it is necessary to give the GDSII passivation layers numbers and the coordinates of two corners of the die (lower left and upper right corners).

### *3.3.2 Step 2*

This step depends on the interconnection between active and passive dies: bumps or bond wires. Actually, the flow methodology is almost identical to the one described at Step 4 of the DFII database format case. The only, but major, difference is that, in the schematic view of the first level cell, the active die symbol is not instantiated. Pins are directly attached to a non-connect component and it is not possible to go down the hierarchy till the top cell of the active circuit.

This is the reason why this flow is not compliant with top-level electrical simulations. However LVS checks can be performed.

## 3.4 Physical checks

The footprint flow that has been developed enables DRC, packaging check and LVS comparison.
Regarding DRC, it is possible to check the distance between the active die pads together with the size of these pads.
From a packaging check point of view, the active die boundary, drawn with a CAD layer, makes it easier to verify some basic rules. Hence designers can, for example, measure the distance between two active dies in the passive design or the distance between an active chip and the side of the passive chip.
For LVS comparison, the first level cell of each active die must be declared as Black box cell as shown in figure 2. This way, connectivity is checked at top level and active designs themselves are not LVS checked (although it is possible to go down to the transistor level).

Furthermore, bumps are recognized as flat two ports components and bond wires as paths.

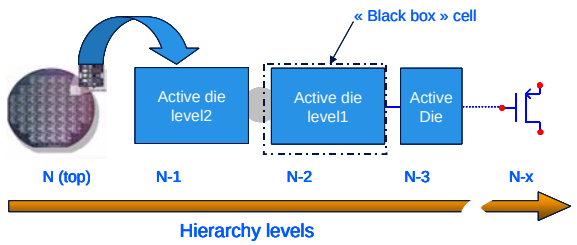



**Figure 2: Multi technology design hierarchy levels**

# 4. ILLUSTRATION ON A TEST VEHICLE

SmarterBoM is a CDMA (Code Division Multiple Access) transceiver demonstrator. Two active dies, one receiver and one transmitter, designed in advanced BiCMOS process are flipped on a carrier passive die. The super IC is also flipped on lead frame. Hence, the assembly process is a double flip-Chip on lead frame. A picture of the three dies stack is presented in figure 3.

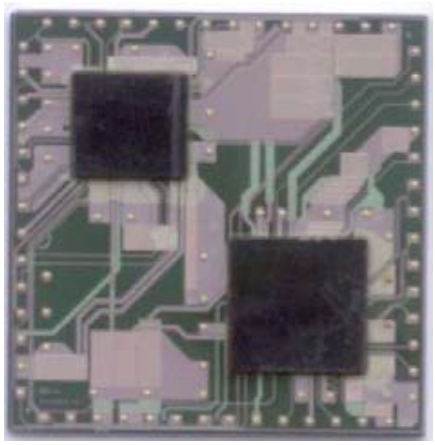


**Figure 3: SmarterBoM package**

It takes less than half an hour to apply the footprint flow on both dies and then it is possible to build top design schematic and layout views. From these views two major utilities of the flow are evaluated: electrical simulation and LVS check.

From the top schematic view of the super-IC, we are able to run electrical simulations in the same way as for a single technology design [5]. In order to reduce netlist complexity some simplified blocks are used (thanks to a config view). More details on how to perform system-level electrical simulations are available in [6].

Then a simple DC simulation enables to verify power and ground supply networks and a transient simulation will allow to check the functionality of the system. For example we can measure the signal power at the output of the transmitter cellular path. The signal versus frequency graph is plotted in figure 4.

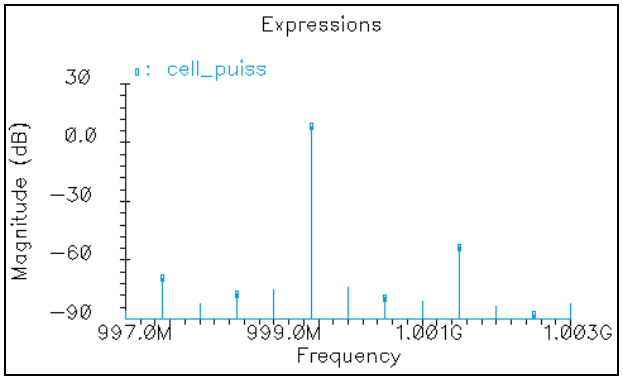



**Figure 4: Signal power at the TX cellular path output**

Furthermore, the SiP design has been LVS checked with success.

## 5. BUMP ELECTRICAL MODEL

Since the footprint flow can enable functional electrical simulations of the dies stack, a model for interconnections is needed. Currently, only bump components have been modeled and a bond wire model including arrays of bond wires (to take into account coupling effect) is planned for next release.

Regarding our flow, only first level interconnect bumps are relevant. The layers stack of such an interconnection is shown in figure 5. On both active and passive dies the passivation layer is opened so that a UBM (Under Bump Metallization) layer can connect the top metal layer. The connection is finalized by a solder bump.

This stack has been simulated with the MOMENTUM 2.5D EM simulator. As it is not possible to simulate spherical structures with this tool, a cylinder has been used to represent the bump. This approximation turned to be well correlated with real case theoretical results [7].

Substrate coupling, as well as coupling (either inductive or capacitive) between bumps, are negligible and then, bumps can be electrically modeled with a serial L, R circuit.
At 2GHz, values of inductance and resistance are respectively 28pH and 13mΩ.

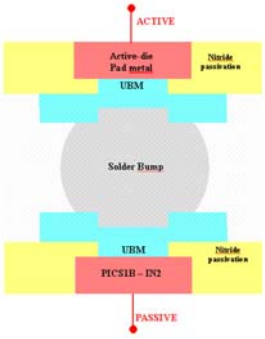



**Figure 5: Bump layers stack**

## 6. CONCLUSION

A general flow for RFSiP applications design was presented. This footprint flow is compliant with either DFII or GDSII active database format and, for both, each step was described depending on the interconnect technique used: bumps or bond wires. It was shown that the procedure could lead to the creation of a schematic, a symbol and a layout view of the super-IC. From these, it is possible to perform all necessary physical checks. The flow also enables electrical simulation and checks of the top-level design in case of a DFII active database format. Bumps are taken into account with their equivalent model and a bond wire model will soon be available. These utilities have been successfully evaluated on a test vehicle.

Hence, for the most common situation of a DFII active database input format, the Footprint flow enables full electrical simulation and layout versus schematic check of complete multi tech ICs.

In addition to bond wires electrical model implementation, several enhancements are planned for next release of the flow. Thus, the lead-frame connection with bumps of the super-IC will be automated. Besides, lead-frame and isolation walls as well as via hole will be implemented. Finally the flow will handle automatic real time synchronization between the active die and its footprint.

## 7. ACKNOWLEDGMENTS

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## 8. REFERENCES

[1] Jianhua, Wu., Anderson, M. J., Coller, D. and Guth, G. *RF SIP Technology Innovation Through Integration*. Electronic Packaging Technology Proceedings in Fifth International Conference (October 28-30, 2003), 484-490.

[2] Tai, K. L. *System-in-package (SIP): Challenges and opportunities*. Proceedings of ASP-DAC in Asia and south Pacific Design Automation Conference, 2000, 191-196.

[3] Koh, W.H. *Advanced area packaging – from CSP to WLP*. Electronic Packaging Technology Proceedings in Fifth International Conference (October 28-30, 2003), 121-125.

[4] Bose, C.B., Amir, J. *Design of fiducials for accurate registration using machine version*. Pattern Analysis and Machine Intelligence, IEEE Transactions (December, 1990), 1196-1200, vol. 12.

[5] Kundert, K. *Introduction to RF simulation and its application*. Bipolar/BiCMOS Circuits and Technology Meeting (September 27-29, 1998), 67-78.

[6] Yoon, P. *Electrical simulation and analysis of large complex electrical systems*. Proceedings of the 37th Midwest Symposium (August 3-5, 1994), 697-700, vol.1.

[7] Ebersberger, B., Bauer, R., Alexa, L. *Qualification of SnAg solder bumps for lead-free flip chip applications*. www.unitive.com/casestudies/pdfs/IFXSnAgqualpapers15p7.pdf