

Efficient Escape Routing for Hexagonal Array with High Density of I/Os

ABSTRACT

The chip/package I/Os count has continuously been growing as the systems become more complicated. High density I/Os interconnection and efficient escape routing with high performance and low cost will greatly benefit the whole electronic system. We analyze the properties of the hexagonal array, which can hold about 15% more I/Os compared with the traditional square grid array. We propose three escape routing strategies for the hexagonal array: column-by-column horizontal escape routing, two-sided horizontal/vertical escape routing, and multi-direction hybrid channel escape routing. We can escape I/Os in the hexagonal array in the same or less number of routing layers compared with square grid array. The practical examples show the efficiency of our strategies. Using hexagonal array, we can reduce the number of escape routing layers as well as increase the density of I/Os.

Keywords

Escape routing, flip chip, BGA, hexagonal array.

1. INTRODUCTION

As the feature size of microelectronic technology becomes smaller, the complexity of electronic systems grows proportionally. According to Rent's rule [1], the number of I/O signals of a module is a function of the number of gates in it:

$$N_p = K_p N_g^\beta \quad (1.1)$$

where, N_p is the number of external signal connections, N_g is the number of logic gates, K_p is a constant, and β is the Rent's rule constant which depends significantly on the kind of module considered. Today's high-performance ICs exhibit upwards of 2,000 I/O pins and require packages that sometimes exceed 100 layers and will go onto boards with more than 50 layers. New technologies, such as flip chip, CSP, BGA, etc., are developed for chip-level (first-level) and package-to-board (second-level) interconnections to accommodate the increasing demand of high I/O signals count. Area array interconnection is widely used in those advanced technologies. In order to connect the I/O signals in the array to the next level assembly, wires are routed to break I/O signals out which is referred as "escape routing" [2][3].

The high I/O signals count and density require an increase in the number of escape routing layers and make the signal integrity issue more serious. An efficient and effective escape routing strategy which achieves high performance with low cost will greatly benefit the electronic product.

Traditionally, the area array is a square grid and I/O signals are escaped row-by-row (column-by-column) from outside. Intuitively some dimensional changes will reduce the number of escape routing layers, such as decreasing wire width and spacing, while these changes expose the system to cost, yield and reliability issues. Gasparini et al. [4] suggested a specific

placement of bumps for C4 packages to minimize the package layers count with change in footprint. They sacrificed I/O density to increase wire density and this strategy was not good for the escape routing with multiple layers. Horiuchi et al. [5] proposed a preferential routing strategy, which created specific pad geometry resulting in a high wiring efficiency. This strategy was very practical for assembly of high I/O count flip chip, CSPs, and BGAs. But it was only suitable for the traditional square grid array. Titus et al. [6] presented a "balls shifted as needed" method, which adjusted and optimized I/Os placement in the array to accomplish the escape routing in one layer. They utilized the advantage of hexagonal array but their placement optimization and escape routing strategy were not suitable for multiple layers. In [8], we have discussed the importance of escape sequence for escape routing and proposed two strategies, central parallel and two-sided, which can reduce the number of escape routing layers effectively for square grid array.

In this paper, we analyze the properties of hexagonal array, which increases the density of I/Os in the array remarkably. We propose three escape routing strategies for the hexagonal array: column-by-column horizontal escape routing, two-sided horizontal/vertical escape routing, and multi-direction hybrid channel escape routing. The examples using practical parameters show that our strategies can escape the hexagonal array very efficiently. Thus we can reduce the number of escape routing layers as well as increase the density I/Os.

The rest of the paper is organized as follows. Section 2 describes the escape routing problem and defines related parameters. The properties of hexagonal array are analyzed in section 3 and detailed comparison between square grid array and hexagonal array is also given. Section 4 explains three escape routing strategies for the hexagonal array. We compare those strategies in section 5 and discuss the conclusions in section 6.

2. PROBLEM DESCRIPTION

In the escape routing problem, I/Os inside the area array are the objects; the corresponding pads are the obstacles and the spaces scattering among the pads in the area array are the routing resources. Fundamentally there are three basic guidelines which are described below.

(i) Spacing between two traces and the width of the trace. As shown in Figure 1, the trace width is W and the pitch is $(W+S_w)$, where S_w is the spacing between the two consecutive edges of the traces.

(ii) Minimum distance S_p between the edge of the pad and the edge of any metal, as shown in Figure 1.

(iii) Diameter of the pad, D , and pitch, P , between two consecutive pads, as shown in Figure 1.

Usually the spacing between two traces S_w and between pad and trace S_p are identical, we can use S to represent the spacing.

Escape routing breaks out I/Os in the array to the outside and the objective is to minimize the number of routing layers and to break out I/Os as many as possible.

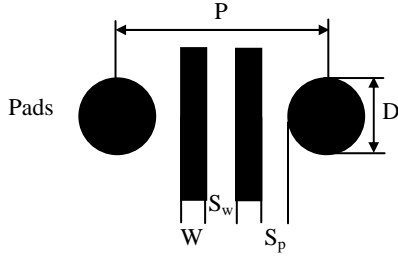


Figure 1. Fundamental parameters

3. HEXAGONAL ARRAY

The typical I/Os array is a square grid matrix and I/Os are located at the crossing points of the horizontal and vertical mesh. The neighboring four I/Os form a square grid unit. For an $n \times n$ square grid array, there are n I/Os in each row and column, n^2 I/Os in the array totally and the area of the array is $(nP+D)^2$. I/Os in the typical square grid array can be shifted and packed further to form a hexagonal pattern. The neighboring six I/Os form a hexagonal unit and one more I/O locates at the center. In a hexagonal array, the angle between the lines joining any adjacent two I/Os is always a multiple of 60° . Figure 2 and Figure 3 show the square grid array and the hexagonal array respectively. We observe that the square grid array is symmetric in horizontal and vertical directions, i.e. if the square grid array is rotated 90° clockwise; it is superposed on the original array. However the hexagonal array doesn't have this properties, it is symmetric in 0° , 60° , and 120° directions, i.e. if the hexagonal array is rotated 60° or 120° clockwise; it is superposed on the original array.

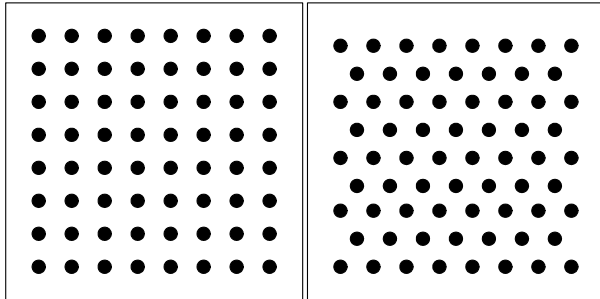


Figure 2. Square grid array Figure 3. Hexagonal array

3.1 Increasing the Number of I/Os

The hexagonal array can hold more I/Os under the same area usage constraint, compared with the square grid array. The area of an $n \times n$ square grid array is $(nP+D)^2$. Using the same area, the hexagonal array will have n and $n-1$ I/Os in each row alternately. The number of rows in the hexagonal array is

$$m = \left\lfloor \frac{2}{\sqrt{3}}(n-1) \right\rfloor + 1 \quad (3.1)$$

The number of I/Os in the hexagonal array is

$$TotalNum(hexagon) = \begin{cases} mn - \frac{m}{2} & m = \text{even} \\ mn - \frac{m-1}{2} & m = \text{odd} \end{cases} \quad (3.2)$$

Plug the formula (3.1) into (3.2), we can prove that the number of I/Os in the hexagonal array is larger than the number of I/Os in the square grid array using same area for any $n \geq 1$. The number of I/Os increased can be approximated as

$$\begin{aligned} & \frac{TotalNum(hexagon) - TotalNum(square)}{TotalNum(square)} \\ & \geq \frac{mn - m/2 - n^2}{n^2} \\ & \geq \frac{\frac{2}{\sqrt{3}}n^2 - \sqrt{3}n - n^2 - \frac{1}{\sqrt{3}}}{n^2} \\ & = \frac{2 - \sqrt{3}}{\sqrt{3}} - \frac{\sqrt{3}}{n} - \frac{1}{\sqrt{3}n^2} \\ & \geq 15.5\% - \frac{\sqrt{3}}{n} - \frac{1}{\sqrt{3}n^2} \end{aligned}$$

For array with large size, the hexagonal array has more advantage. Table 1 shows their comparison for different size of arrays.

Table 1. Square grid array vs. Hexagonal array using same area, minimum pitch

Size n	Square grid array		Hexagonal array		Increase
	# rows	# I/Os	# rows	# I/Os	
10	10	100	11	105	5%
15	15	225	17	247	9.78%
20	20	400	23	449	12.25%
25	25	625	28	686	9.76%
30	30	900	34	1003	11.44%
35	35	1225	40	1380	12.65%
40	40	1600	46	1817	13.56%

3.2 Increasing the Spacing between I/Os

The hexagonal array can increase the average I/Os pitch under the similar number of I/Os and same area constraint, compared with square grid array. In an $n \times n$ square grid array, the pitch of the adjacent horizontal or vertical I/Os is the minimum pitch P . Holding the same number of I/Os in same area, i.e. n^2 I/Os in area $(nP+D)^2$, the corresponding hexagonal array can separate the I/Os loosely.

We assume the hexagonal array has k and $k-1$ I/Os in each row alternately, and then according to (3.1) the number of rows in this hexagonal array is

$$l = \left\lfloor \frac{2}{\sqrt{3}}(k-1) \right\rfloor + 1 \quad (3.3)$$

The number of I/Os in the corresponding hexagonal array is

$$TotalNum(hexagon) = \begin{cases} lk - \frac{l}{2} & l = even \\ lk - \frac{l-1}{2} & l = odd \end{cases} \quad (3.4)$$

Therefore the I/Os pitch P' in the hexagonal array can be solved from the following equations

$$\begin{cases} TotalNum(hexagon) = n^2 \\ kP' = nP \end{cases} \quad (3.5)$$

Plug the formula (3.3) and (3.4) into (3.5), we can prove that the pitch P' in the hexagonal array is larger than the minimum pitch P for large n . Table 2 shows their comparison for different size of arrays.

Table 2. Square grid array vs. Hexagonal array using same area, holding similar number of I/Os

Square grid array			Hexagonal array			Increase
n	# I/Os	Pitch	k	# I/Os	Pitch	
25	625	P	24	635	1.04P	4.17%
30	900	P	29	941	1.03P	3.45%
35	1225	P	33	1235	1.06P	6.06%
40	1600	P	38	1613	1.05P	5.26%
45	2025	P	43	2083	1.05P	4.65%
50	2500	P	47	2511	1.06P	6.38%

4. ESCAPE ROUTING FOR HEXAGONAL ARRAY

4.1 Column-by-Column Horizontal Escape Routing

The traditional escape routing strategy for the square grid array is to break out the I/Os row-by-row/column-by-column from outside to inside as shown in Figure 4. The spacing between two consecutive I/Os constrains the number of wires going through and limit the number of I/Os escaped for one layer.

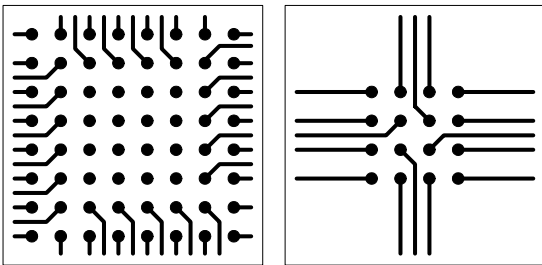


Figure 4. Traditional escape routing for square grid array

The hexagonal array is not symmetric in horizontal and vertical directions. In the compact hexagonal array, in which the pitch of adjacent I/Os is the minimum pitch, the vertical routing channel, as shown in Figure 5, is the edge of the hexagonal unit and the number of wires that can be escaped through is

$$Num(wires)_{verticalChannel} = \left\lfloor \frac{P - D - S}{S + W} \right\rfloor \quad (4.1)$$

However the horizontal routing channel, as shown in Figure 5, is a diagonal of the hexagonal unit and has larger capacity:

$$Num(wires)_{horizontalChannel} = \left\lfloor \frac{\sqrt{3}P - D - S}{S + W} \right\rfloor \quad (4.2)$$

Therefore the horizontal escape routing can be more efficient than the vertical escape routing. Similar as the traditional escape routing method for the square grid array, the hexagonal array can be treated as zigzag column array and I/Os can be escaped column-by-column through the horizontal routing channels as shown in Figure 6 and Figure 7.

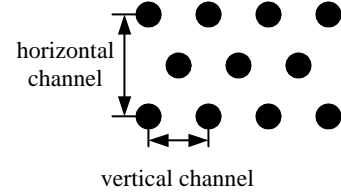


Figure 5. Vertical/horizontal channels

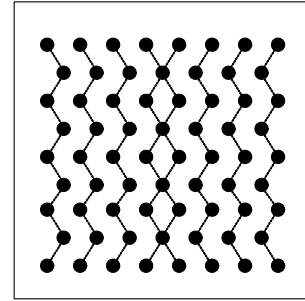


Figure 6. Zigzag columns in hexagonal array

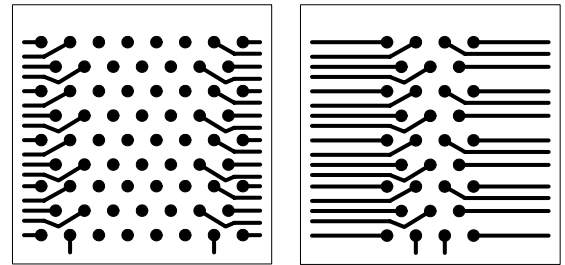


Figure 7. Column-by-Column horizontal escape routing for hexagonal array

Using this column-by-column horizontal escape routing method, under some conditions, we can accomplish the escape routing for the hexagonal array with the same number of routing layers as the square grid array although the hexagonal array holds more I/Os.

We assume the number of wires that can go through the vertical routing channel, i.e. the channel between adjacent I/Os with minimum pitch, is A . Thus for the square grid array, $A+1$ rows and columns can be escaped in one routing layer and the number of routing layers for breaking out an $n \times n$ square grid array using the tradition method is

$$Num(layers)_{square} = \left\lceil \frac{n}{2(A+1)} \right\rceil \quad (4.3)$$

The hexagonal array with same area also has n zigzag rows. If we assume to use the same number of routing layers as the square grid array, the number of wires that can go through one horizontal routing channel should satisfy

$$Num(wires)_{horizontalChannel} \geq 2A + 1 \quad (4.4)$$

Combine (4.1) (4.2) with the assumptions, we can derive the condition is

$$\begin{cases} Num(wires)_{verticalChannel} = \left\lfloor \frac{P - D - S}{S + W} \right\rfloor = A \\ Num(wires)_{horizontalChannel} = \left\lfloor \frac{\sqrt{3}P - D - S}{S + W} \right\rfloor \geq 2A + 1 \end{cases}$$

$$\Rightarrow D \geq (2 - \sqrt{3})P + W \quad (4.5)$$

As long as the array's parameters satisfy the condition (4.5), I/Os in the hexagonal array can be escaped within the same number of routing layers as square grid array and the hexagonal array has the same area as the square grid array but holds more I/Os. Table 3 shows the practical parameters for flip chip interconnect and fine pitch BGA/CSP, which is provided by ITRS (International Technology Roadmap for Semiconductors) [7]. The condition is usually satisfied.

Table 3. Practical Parameters for condition, unit: μm

Year	Flip Chip		FBGA/CSP	
	2005	2018	2005	2018
Pitch	130	75	400	100
Pad Diameter	65	35	120	40
Line Width	27.8	15	36	12
Line Spacing	27.9	15	36	12
Condition (4.5)	✓	✓	✓	✓

We take an 8×8 square grid array as a simple example, as shown in Figure 2. The pitch of every two adjacent horizontal/vertical I/Os is the minimum pitch. This square grid array has 64 I/Os totally. The hexagonal array, which uses same area, can have 68 I/Os as shown in Figure 3 and the pitch of any two adjacent I/Os is also the minimum pitch.

The following values for feature sizes are used in this example and they satisfy the condition (4.5).

- 1) Minimum pitch (P_{min}) = $240\mu\text{m}$
- 2) Diameter of I/O (D) = $110\mu\text{m}$
- 3) Wire width (W) = $43\mu\text{m}$
- 4) Wire spacing (S) = $43\mu\text{m}$

The vertical routing channel can route 1 wire and the horizontal routing channel can route 3 wires. Therefore we can use two layers to break out I/Os in that square grid array as shown in Figure 4. We can also use two layers to escape I/Os in the hexagonal array as shown in Figure 7. The number of routing layers for the square grid array and the hexagonal array is same although the hexagonal array has more I/Os.

4.2 Two-sided Horizontal/Vertical Escape Routing

We have proposed the two-sided escape routing approach for square grid array in [8]. This approach breaks out I/Os in the outside and inside rows/columns simultaneously. It can maintain the outline of the array in a good shape and I/Os are escaped on different routing layers equably.

In the column-by-column horizontal escape routing strategy for the hexagonal array, the number of zigzag columns in the array constrains the number of routing layers. The two-sided idea can also be used in hexagonal array to reduce the number of routing layers. I/Os in the middle zigzag columns can be escaped through vertical routing channels at the same time as I/Os in the outside zigzag columns are escaped through horizontal routing channels.

We take a 10×11 hexagonal array as an example, which has the same area as a 10×10 square grid array. The pitch of any two adjacent I/Os is the minimum pitch and there are 105 I/Os totally. The values for feature sizes are same as the example in section 4.2.

Using the column-by-column horizontal escape routing method, we need three layers as shown in Figure 8. However we only use two layers in two-sided horizontal/vertical escape routing approach as shown in Figure 9.

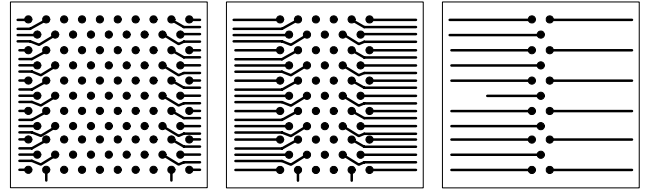


Figure 8. Column-by-column horizontal escape routing

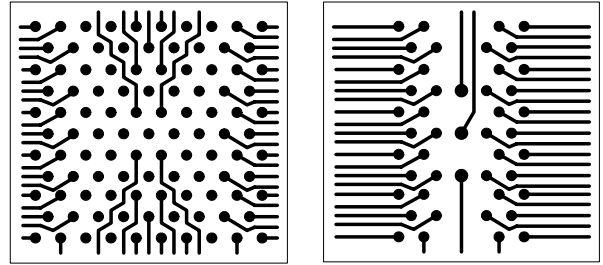


Figure 9. Two-sided horizontal/vertical escape routing

The two-sided approach utilizes the routing channels sufficiently and increases the number of I/Os escaped in every routing layer because it breaks out I/Os inside and outside simultaneously. Compared with the column-by-column horizontal escape routing, it can decrease the number of routing layers efficiently.

4.3 Multi-direction Hybrid Channel Escape Routing

4.3.1 Array Partition and Hybrid Channel

The hexagonal array is symmetric in 0° , 60° , and 120° directions. It can be treated as many nested hexagons as shown in Figure 9. The array can be divided into six partitions and I/Os can be escaped to the outside following six directions. Figure 10 shows this escape routing style.

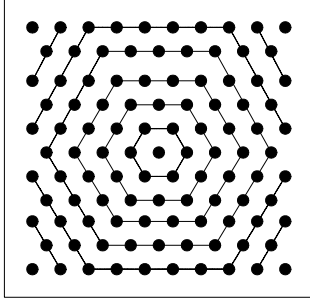


Figure 9. Nested hexagons

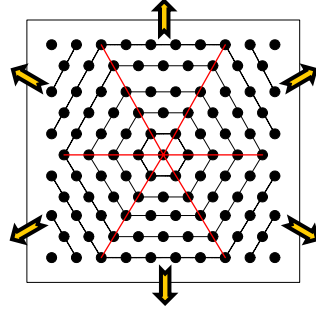


Figure 10. partition

For each partition, the adjacent I/Os in the same row have the minimum pitch. Instead of breaking out I/Os row by row, we can escape the I/Os selectively to form indented outline and hybrid routing channels as shown in Figure 11.

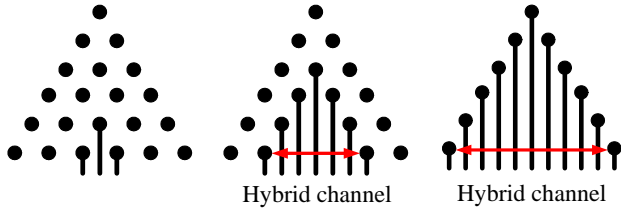


Figure 11. Indented outline and hybrid channel

Because the hybrid routing channel has larger capacity, i.e. it can allow more wires going through, this escape strategy can increase the number of I/Os escaped for one routing layer and potentially reduce the number of routing layers. The number of wires going through the hybrid routing channel, which consists of k vertical channels, is

$$Num(wires)_{hybridChannel} = \left\lfloor \frac{kP - D - S}{S + W} \right\rfloor \quad (4.6)$$

4.3.2 Escape Routing through Hybrid Channel

Using this multi-direction hybrid channel escape routing strategy, the hexagonal array can be treated as consisting of many indented rows as shown in Figure 12.

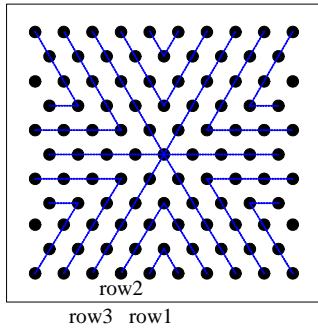


Figure 12. Indented rows in hexagonal array

For an $n \times m$ hexagonal array, the number of indented rows is

$$I = \left\lfloor \frac{m+1}{4} \right\rfloor \quad (4.7)$$

We assume the number of wires that can go through the vertical routing channel is A . Thus

$$Num(wires)_{verticalChannel} = \left\lfloor \frac{P - D - S}{S + W} \right\rfloor = A \quad (4.8)$$

$$\Rightarrow P - D - S \geq A(s + W)$$

The condition for routing I/Os in A indented rows through the hybrid routing channel, which consists of k vertical channels, is

$$Num(wires)_{hybridChannel} = \left\lfloor \frac{kP - D - S}{S + W} \right\rfloor = A(2k - 1) \quad (4.9)$$

$$\Rightarrow kP - D - S \geq A(2k - 1)(s + W)$$

Plug (4.8) into (4.9), the condition can be simplified as

$$D + S \geq A(s + W) \quad (4.10)$$

Table 4. Practical Parameters for condition, unit: μm

Year	Flip Chip		FBGA/CSP	
	2005	2018	2005	2018
Pitch	130	75	400	100
Pad Diameter	65	35	120	40
Line Width	27.8	15	36	12
Line Spacing	27.9	15	36	12
A	0	0	3	2
Condition (4.10)	✓	✓	×	✓

The condition is generally satisfied for small A . Under this condition, we can maintain the indented outline of the array and escape at least A indented rows on every routing layer. I/Os in large array can be escaped very efficiently though the hybrid channel.

4.3.3 Automatic Escape Routing Procedure

The hybrid escape routing approach organizes I/Os in the array regularly. The escape routing rules for each partition are identical and the routing for every partition is independent of each other. Furthermore the wires breaking out I/Os go through the hybrid channel orderly. Thus escape routing program can be implemented straightforwardly to accomplish this kind of escape routing for any given hexagonal array automatically.

The automatic procedure of the multi-direction hybrid channel escape routing is illustrated as follows:

Partition:

Divide the hexagonal array into six partitions.

Labeling:

Identify the indented rows in each partition.

Label I/Os using partition ID and indented rows ID.

Assignment:

For each partition {

Determine the number of indented rows that can be escaped in the first routing layer according to the vertical channel capacity.

Determine the number of indented rows that can be escaped in each following layer according to the hybrid channel capacity.

}

Routing:

```
For each partition {  
  Escape I/Os on the first layer symmetrically through vertical  
  channel.  
  Escape I/Os on each following layer directly through the  
  hybrid channel.  
}
```

Post processing refinement:

Refine the escape routing for I/Os located at special positions, e.g. center, corner, partition boundary, etc., to further reduce the number of routing layers.

4.3.4 Test cases

For the 10×11 hexagonal array example in section 4.2, we only need two layers using this multi-direction hybrid channel escape routing strategy as shown in Figure 13.

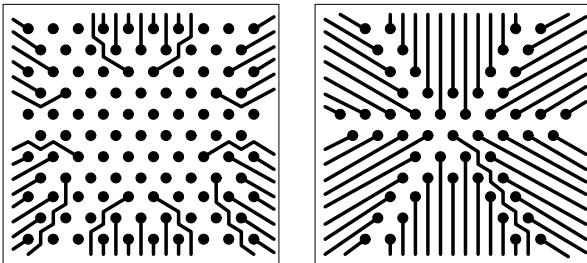


Figure 13. Multi-direction hybrid channel escape routing

5. DISCUSSION

The hexagonal array can hold more I/Os than the traditional square grid array using same area, i.e. the hexagonal array has larger I/Os density. For complicate ICs and packages, the hexagonal array can provide more external interconnection. The approximate increase of I/Os count for large array is 15%.

The column-by-column horizontal escape routing strategy is very straightforward for the hexagonal array. Using this strategy, I/Os in hexagonal array can be escaped in the same number of routing layers as the square grid array which has same area although more I/Os are packed inside. However, the vertical routing channels are wasted in this strategy.

The two-sided horizontal/vertical escape routing strategy overcomes the shortcoming of that straightforward strategy. I/Os in the outside zigzag columns are escaped through horizontal channel and simultaneously the I/Os in the middle zigzag columns are escaped through vertical routing channels. All the routing channels are utilized sufficiently and the number of escape routing layers is reduced. Nevertheless, there is no simple routing rule for the wires breaking out I/Os in the middle zigzag columns, so it's hard to implement in automatic program and those wires need to go through many other I/Os, thus crosstalk is an important issue to be considered.

The multi-direction hybrid channel escape routing strategy uses the symmetric property of hexagonal array to divide it into

six partitions and exploits hybrid channels to increase the escape efficiency. The hybrid channels increase the number of escape routing wires on every layer and consequentially decrease the number of layers. I/Os in each partition are escaped independently which makes the problem simpler and the wires routing through hybrid channels are very ordered, so this strategy is easy to be implemented in automatic program.

In summary, hexagonal array can be escaped very efficiently as well as providing high density of I/Os.

6. CONCLUSIONS

In this paper, we discuss the advantages of the hexagonal array and propose three escape routing strategies for it. Using same area, hexagonal array holds about 15% more I/Os compared with square grid array and our strategies can escape the I/Os in the hexagonal array in the same or less number of routing layers. The practical examples show the efficiency of our strategies. Using hexagonal array, we can reduce the number of escape routing layers as well as increase the density of I/Os. We will continue working on the automatic escape routing program for the hexagonal array and the related crosstalk issues will also be investigated.

7. REFERENCES

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