# Yield Prediction for 3D Capacitive Interconnections


## ABSTRACT

Capacitive interconnections represent a promising technology for high-speed and low-power signaling in 3D packages; since the performance of AC links, in terms of Band-Width and Bit-Error-Rate (BER), depends on assembly and synchronization accuracy, a statistical analysis is required.

We present a yield prediction method for 3D capacitive links: starting from the analysis of the communication circuits and BER measurements, we discuss stacking variability to predict the statistical behavior of reliability and performance. Parametric yield methodology is applied to a test case: yield prediction is performed with a constrained inter-electrode coupling and operating frequency.



## Categories and Subject Descriptors

B.8.2 [**Hardware**]: Performance and Reliability—*Performance Analysis and Design Aids*; B.4.4 [**Hardware**]: Input/Output and data communications—*Performance Analysis and Design Aids*

## General Terms

Reliability, Performance

## Keywords

3D Integration, Capacitive Interconnections, Parametric Yield.


## 1. INTRODUCTION

The cost of Systems-on-a-Chip (SoC's) is dramatically increasing due to the requirements to integrate digital logic with memory and analog functions. Moreover, the reliability and performance of today's SoC's are far more affected by interconnect networks rather than by logic blocks both in terms of clock frequency and of power consumption. High-speed 3D chip-to-chip communication could represent a solution to these problems: active layers are stacked within the same package and made to communicate by means of an efficient vertical interconnect scheme. In this scenario, contactless communication allows forwarding the interconnection effort from Back-End Of the Lines (BEOL) to the packaging step. This characteristic enables the vertical connection of standard-manufactured dies and, consequently, it reduces process development costs. In the last few years, several prototypes have been presented, demonstrating capacitive [12][13][14] and inductive [8][9][10][11] signaling: these demonstrate how Gbps/pin bandwidth can be achieved while maintaining low power consumption.

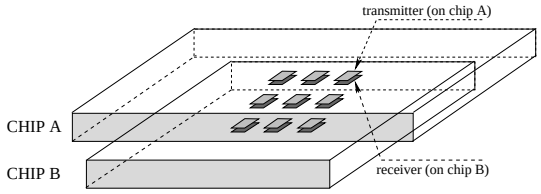


**Figure 1: Capacitive interconnection concept.**

In this paper, we present a study of contactless communication in terms of process variability, leveraging our previous work on 3D capacitive interconnections [14]. This technology allows Gbps band-width but the reduced coupling (8x8$\mu m^2$ electrodes) between the communication circuits induces an increased error sensitivity. For this reason, a statistical analysis is necessary to evaluate the quality of communication along 3D channels and to investigate the most proper implementation of digital systems. We begin with an analysis of capacitive interconnection behavior and Bit-Error-Rate (BER) measurements. The BER measurements will be fitted by the interconnection analytical description and the presented conditions will be applied to a parametric yield analysis methodology [4].

Since the stacking procedure for this 3D technology does not affect the silicon manufacturing process, die and stacking parameters are decoupled, so we can focus only on the latter. In this paper, a parametric yield model is presented, with the focus on the interconnection reliability and performance: the former refers to the probability that the capacitive coupling is so poor that the interconnect is not reliable, even at low operating frequencies; the latter takes into consideration the effects of stacking parameters on delays along the vertical paths. To compute the parametric yield as a function of these delays, a statistical timing analysis methodology [5][6] is applied and a complete physical characterization of capacitive interconnections has been carried out.



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The paper is organized as follows: in Section 2 we briefly review the 3D contactless technology; in Section 3, the conditions for correct operations are discussed; in Section 4 we present BER measurements and we fit the experimental results; in Section 5 we describe the yield prediction methodology by performing physical (Section 5.1) and timing (Section 5.3.1) analyses. Finally, conclusions and results will be presented (Section 6).

## 2. CONTACTLESS 3D TECHNOLOGIES

Three-dimensional integration technologies play an essential role in avoiding some of the pains of deep sub-micron (DSM) integration [1] [2] [3]. The advantages of this approach are manifold:

- Efficient 3D channels can be allocated over the entire surface of a chip, thus resulting in a richer chip boundary with respect to standard perimetral IO rings;
- Dies manufactured in different technologies can be collocated in the same package so that the most appropriate fabrication flow can be chosen for each portion of the system;
- Logic can be partitioned in different chips so that denser and shorter routing can also be achieved.

Many 3D fabrication flows have been investigated in recent years, differing for *method of assembly, number of layers available, impact on system geometry* and *the related parasitic load* [7]. In the sequel, we focus on the contactless approach.

This approach is based on inductive or capacitive coupling for communication between layers. No modification to a standard technology process is required; assembly is at the chip level so that chips can be validated before the assembly process. Furthermore, AC coupled interconnects are more reliable than DC interconnects that suffer from mechanical stress and the parasitic load is much reduced when compared to wire bonding and micro bumps. The feasibility of inductive [8][9][10][11] or capacitive coupling [12][13][14] has been proven with a few prototypes. Inductive-based 3D communication allows interconnecting more than two layers (stacked face-to-back) within the same package, but it requires transmitter and receiver cells with a large pitch as well as high power consumption. For capacitive communication (Figure 1), receivers and transmitters are implemented on each device and they are coupled through capacitive electrodes, realized in the upper metal layer; in this case, chips are stacked face-to-face. Capacitive communication through inter-chip electrodes provides high bandwidth (over 900Mbps/pin for the 8x8$\mu m^2$, 14$Mbps/\mu m^2$) with very low power consumption (0.14$mW/Gbps$)[14].

## 3. INTERCONNECT ANALYSIS

The equivalent circuits for capacitive interconnects are shown in Figure 2. The transmitter cell samples data for transmission and performs level-to-edge encoding: on the rising edge of TX clock, the sampled data is propagated to the transmitter output; on the falling edge, the transmitter electrode switches to the inverted value performing the required conversion. The receiver cell biases the receiver node in the high-gain state and samples the received data: during the high phase of the receiver clock, a CMOS switch biases

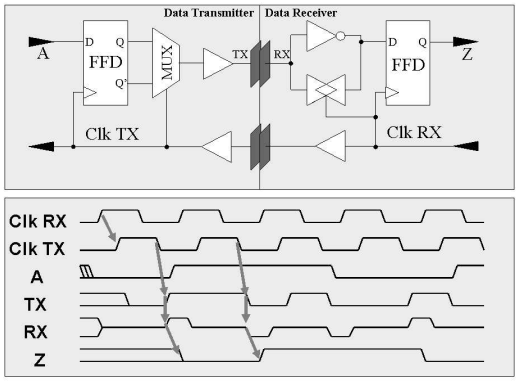


**Figure 2: Communication circuits for AC interconnection.**

the electrode on the logic-threshold of the input inverter; during the low phase of the clock, the electrode is left in high-impedance state, ready to amplify the transmitted signal. The synchronization between receiver and transmitter is provided by a clock signal propagated from the receiver chip to the transmitter one; one single clock interconnection is used for the synchronization of a large number of data connections. The full functionality is shown in Figure 2.

For the interconnect to work properly, three conditions must be satisfied:

- sufficient inter-electrodes coupling:

$$\Delta V_{RX} = \frac{C_{3D}}{C_{3D} + C_{GND}} V_{DD} > V_m \quad (1)$$

  where $C_{3D}$ is the capacitive coupling between electrodes, $C_{GND}$ is the parasitic capacitance on the receiver electrode and $V_m$ represents the noise immunity margin;

- timing margins for the correct sampling of the received data:

$$\Delta T_{TX} = (1-\delta)T - T_{D,TX} - T_{CLK,F} - T_{SU} > T_{TX,m} \quad (2)$$

  where $T_{D,TX}$ represents the data delay from the falling edge of transmitter clock to the input of receiver flip-flop, $T_{CLK}$ is the skew between transmitter and receiver clock (respectively R for the rising edge or F for falling one), $\delta$ is the clock duty-cycle and $T_{TX,m}$ represents additional timing margin;

- synchronization margins for the preset-evaluation phases of both RX and TX:

$$\Delta T_{PRESET} = \delta T - T_{D,PRE} - T_{CLK,R} > T_{PRE,m} \quad (3)$$

  where $T_{D,PRE}$ represents the data delay from the rising edge of the same clock to the transmitter electrode (required during preset); $T_{PRE,m}$ is introduced as additional timing margin.

These conditions are the basis for both the Bit-Error-Rate model and the parametric yield one.

## 4. BIT-ERROR-RATE MODEL

To calibrate our model, test-chips have been manufactured in $0.13\mu m$ technology and assembled face-to-face [14]. The design includes a dedicated test interface, enabling testing-at-speed of the capacitive interconnection. Test-patterns are provided from an acquisition-board that performs the BER measurement as well. Figure 3 presents the measured Bit-Error-Rate for 8x8$\mu m^2$ and 15x15$\mu m^2$ capacitive interconnects respectively as well as the values predicted by our proposed model. The plots of the BER vs. frequency clearly show essentially no error on more than $10^{+13}$ measurements in a wide frequency spectrum; moreover, the BER is different in the case of transmitting a '0' or a '1' and it increases orders of magnitude in the range of few MHz. Our model will reflect these observations. First, since condition (1) is frequency independent[1], it does not contribute to the measured BER of the interconnections under-test.

Assuming that $T_{TX,m}$ and $T_{PRE,m}$ are stochastic variables with Gaussian distribution, zero mean uncertainties, the probability that condition (2) and (3) are met can be calculated as $P = 1 - 0.5erfc(\Delta T/\sigma\sqrt{2})$ where $\Delta T$ is the required value, and $\sigma$ is the standard deviation. To compute a first-order BER model, the following definitions of error-probability are used:

$$EP_{tx} = \frac{1}{2} erfc\left(\frac{\Delta T_{TX}}{\sigma_{tx}\sqrt{2}}\right); \quad (4)$$

$$EP_{pre} = \frac{1}{2} erfc\left(\frac{\Delta T_{PRESET}}{\sigma_{preset}\sqrt{2}}\right); \quad (5)$$

Condition (3) yields soft-errors in case the transmitted bit is equal to the previous one, since in this case the preset phase of transmitter is required. The error-probability due to condition (2) applies to each transmission, since it represents the arrival constraints required for data sampling. Assuming total correlations between the source of uncertainty, our first order BER model is:

$$BER = BER_{switch} + BER_{const},$$

where

$$BER_{switch} = P_{switch} EP_{tx};$$

$$BER_{const} = P_{const} MAX(EP_{tx}, EP_{pre});$$

where $P_{switch} = P(A[nT] \neq A[(n-1)T])$ and $P_{const} = P(A[nT] = A[(n-1)T])$; A is the transmitter input.

The propagation delays in (2-3) are obtained by nominal SPICE simulations. The timing uncertainties and duty-cycles in (4-5) are numerically computed to optimize the fit of the model with the measured data. Since propagation delay significantly differs for transmission of a '0' or a '1', the model takes into consideration the two cases separately; the fitted model is shown in Figure 3 for 8x8$\mu m^2$ and 15x15$\mu m^2$ interconnections.

The BER model together with the measured data show that BER is of little concern for the 3D capacitive interconnect scheme: a BER-aware design can improve working frequency of just few MHz.

## 5. PARAMETRIC YIELD PREDICTION

[1]Resistance and inductance of the interconnect are negligible; for this reason the inter-electrode transfer function is a constant capacitance ratio.

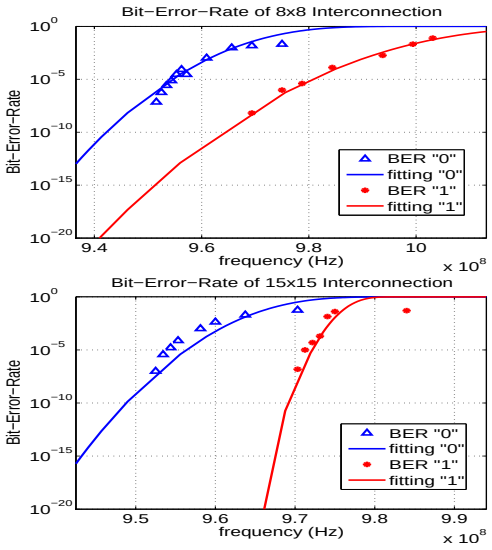


**Figure 3: BER: Measured results and fitted model for 8x8 and 15x15 interconnections.**

The actual number of samples we have access to and the relative maturity of the technology do not allow for a meaningful statistical analysis of catastrophic yield. We focus on parametric yield as it can be estimated using mathematical modeling and simulation. Parametric yield is particularly important at this early stage of the technology since it can provide a design guideline not only for circuit implementation but also for assembly development. The yield model we propose consists of two parts: the first part, that we call interconnect reliability ($Y_R$), is the probability of meeting the capacitance constraints that is required by condition (1); the second part, that we call interconnect performance ($Y_T$), is the probability that the timing constraints expressed in conditions (2-3) are satisfied.

In this analysis, we consider only the statistical variations that affect the 3D capacitive coupling and depend on the assembly technology. The main assembly parameters are two:

- Alignment accuracy. The alignment variability depends primarily on the accuracy of the flip-chip bonder that provides a known alignment accuracy of $1\mu m$, with Gaussian distributed uncertainties.

- Inter-chip dielectric thickness. The present number of available samples does not allow for a full statistical characterization of dielectric thickness. We can extract corner-case conditions, with best and worst cases at $0.5\mu m$ and $1.1\mu m$ respectively. We then assume a Gaussian distribution, with $\pm 3\sigma$ corresponding to the corners.

Based on these hypotheses and data, we infer the statistical characteristics of the vertical path capacitances by running Monte Carlo analysis and we analyze their effects on conditions (1-3) to obtain the parametric yield of the 3D assembly.

### 5.1 Extracting capacitance values

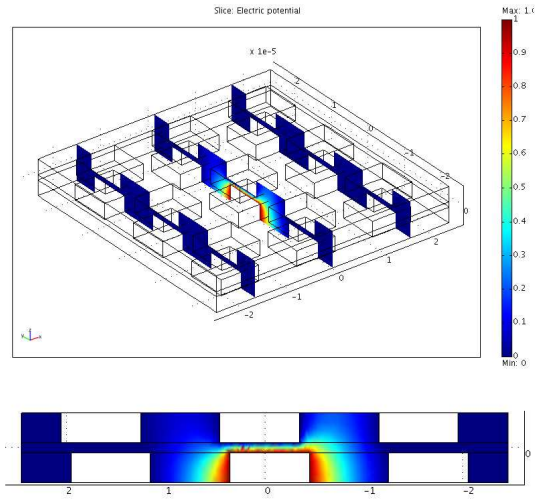


**Figure 4: Physical model for parasitic extraction.**

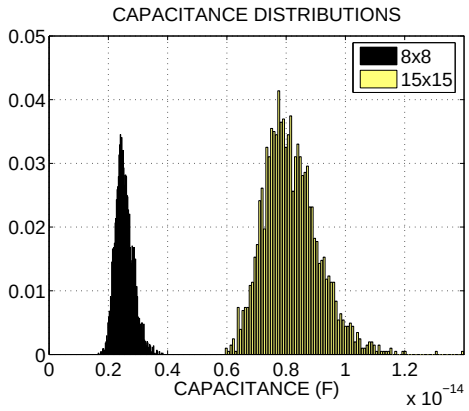


**Figure 5: Capacitance Distributions for 8x8$\mu m$ and 15x15$\mu m$ electrodes.**

To compute the capacitances related to chip-to-chip stacking, a 3x3 electrode geometry has been implemented in a FEMLAB-MATLAB environment [16][15] (Figure 4). This geometry is fully parametric: size, pitch and thickness of electrodes, inter-chip distance, adhesive parameters and misalignment can be specified at execution time, enabling the evaluation of all design and technology parameters.

In our test-case, the interconnection pitch is equal to twice the electrode size: from simulation experiments, we note that RX-TX coupling is at least two orders of magnitude larger than the capacitances among adjacent communication channels. Exploiting these experimental data, execution time for extraction can be significantly reduced evaluating the statistical variability of interconnection capacitance (with a single-channel geometry) while keeping the nominal value for inter-channel capacitances.

The Monte Carlo iteration-time of our method is reported in Table 3; capacitance distribution for the 8x8$\mu m^2$ and 15x15$\mu m^2$ interconnections are presented in Figure 5; mean and standard deviation values are summarized in Table 1. Given the non-linearity of the relation between stacking parameters and capacitance, the resulting distributions is not exactly normal. Nevertheless, in order to speed up the estimation process, in the following sections we approximate the distribution with a Gaussian process.

| | Data 8X8 | Data 15X15 | Data 25X25 |
|---|---|---|---|
| $C_{3D}$ min. | 2.2fF | 3fF | 5.5fF |
| $\overline{C_{3D}}/\sigma_C$ | 2.53fF/0.3fF | 8.17fF/0.99fF | 21.5fF/2.1fF |
| $1 - Y_R$ | 0.136 | 8.3E-8 | 1.3E-14 |

**Table 1: Mean and standard deviation of inter-electrode coupling, minimum required capacitance and relative fault probability.**

## 5.2 Computing Interconnect Reliability

Condition (1) determines the minimum coupling requirements to have a functional interconnect: if the propagated voltage is low, the noise sensitivity is increased and the capacitive interconnection becomes unreliable. Thus, the 3D interconnection meets the requirements if the receiver input swing is larger than $V_m$. To perform this analysis, we choose $V_m = V_{DD}/2 - V_t$, where $V_t$ is the transistor threshold: this means that the noise-immunity margins of the receiver input are respected. The minimum coupling for different interconnection size has been calculated with SPICE simulations (including all on-chip parasitics). The capacitance constraints are summarized in Table 1. Considering a normal distribution for the inter-electrode capacitance, the probability of meeting the required coupling can be calculated:

$$Y_R = \frac{1}{2} erfc\left(\frac{C_{min} - \overline{C_{3D}}}{\sigma_C \sqrt{2}}\right)$$

$C_{3D}$ and $\sigma_C$ are the mean and standard deviation of the interconnect coupling. For results, see Table 1: larger electrodes imply a more reliable communication.

## 5.3 Computing Interconnect Performance

Conditions (2-3) represent constraints on bandwidth per pin. The propagation delay distribution through the vertical link will be analyzed in Section 5.3.1: $T_{3D,-} = T_{D,-} + T_{CLK,-}$ will account for data propagation and for the inter-chip clock skew during transmission and during preset as well ($T_{3D,TX} = T_{D,TX} + T_{CLK,F}$ and $T_{3D,PRE} = T_{D,TX} + T_{CLK,F}$ respectively). Variability on setup time and clock duty-cycle are not related to 3D capacitive coupling, thus they are not included in our analysis. The timing uncertainty (such as clock jitter) will be accounted in the additional margins $T_{TX,m}$ and $T_{PRE,m}$.

### 5.3.1 *Statistical Timing Analysis for the Vertical Link*

Since the signal path is completely embedded in the RX-TX structure, a complete statistical analysis with Monte Carlo SPICE simulations is used. The statistical variations are applied to the communication capacitance ($C_{3D}$) (as mentioned in Section 5.1, inter-channel cross-talk is taken into account with nominal coupling parameters). All on-chip parasitics are extracted with standard CAD tools and they are embedded in the receiver and transmitter sub-circuits. No parameter variations are introduced for standard manufacturing parameters, such as gate length and wire size, as we consider here only the impact of 3D technology. Figure 6 presents the timing distribution for the data propagation delays, referred to 8x8$\mu m^2$ electrode size; Table 2 summarizes

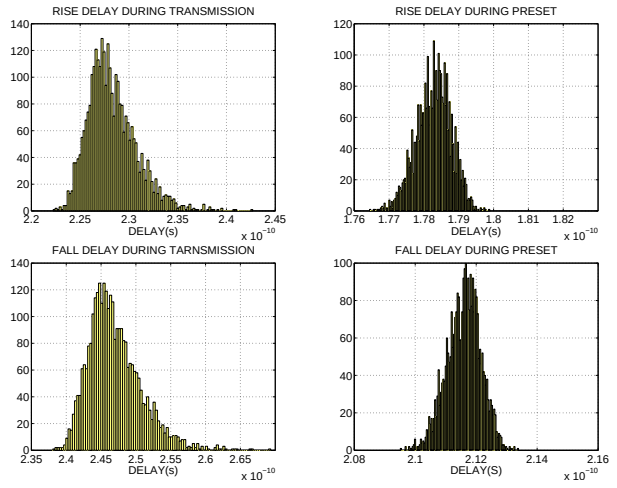


**Figure 6: Delay distributions for propagation along 8x8$\mu m^2$ capacitive interconnections.**

| | $T_{TX,F}$ | $T_{TX,R}$ | $T_{PRE,F}$ | $T_{PRE,R}$ |
|---|---|---|---|---|
| 8 | 247/3.45ps | 228/2.5ps | 212/0.56ps | 178/0.49ps |
| 15 | 229/1.2ps | 242/2.4ps | 231/0.48ps | 198/0.61ps |
| 25 | 239/1ps | 267/1.2ps | 261/0.79ps | 232/0.44ps |
| | $T_{CLK,F}$ | | $T_{CLK,R}$ | |
| clk | 66/4.1ps | | 22.7/2.7ps | |

**Table 2: Propagation delays of capacitive interconnections, mean and standard deviation.**

the simulation results. The distribution of the inter-chip delay does not exhibit a Gaussian characteristic, since the impact of communication coupling on transmitter-receiver delay is non-linear. To compute the overall uncertainty on the 3D link, the convolutions of all gate variability on the vertical path have to be evaluated. To simplify and speed up the analysis, a linear approximation is applied to the relations between delays and inter-electrode capacitance. By applying the principal component decomposition presented in [5] and [6], the propagation delay can be expressed as:

$$d = d_0 + k_{3D} C_{3D,norm} + \sum_i k_i p_i;$$

where $d_0$ is the expected value of propagation delay, $C_{3D,norm}$ is the normalized inter-chip capacitance (normally distributed with zero mean and unit variance) and $p_i$ are the orthogonal principal components of the silicon-manufacturing process-parameters: $C_{3D,norm}$ is statistically independent from the single-die parameters[2], and it can be separated from the other contributions.

The delay statistical analysis is performed on the vertical signal path: $TX, CLK \Rightarrow RX, CLK \Rightarrow TX, D \Rightarrow BUFFER \Rightarrow RX, D$ Figure 7.
The overall propagation time can be expressed as:

$$T_{3D,-} = \sum_j d_{0,j} + \sum_j k_{3D,j} C_{3D,norm} + \sum_j \sum_i k_{i,j} p_i;$$

[2]The variability of inter-electrode coupling due to chip variations are negligible with respect to the impact of assembly technology.

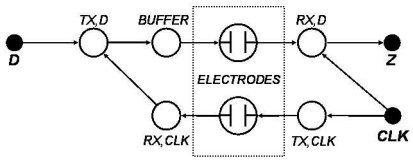


**Figure 7: Block representation of vertical signal path.**

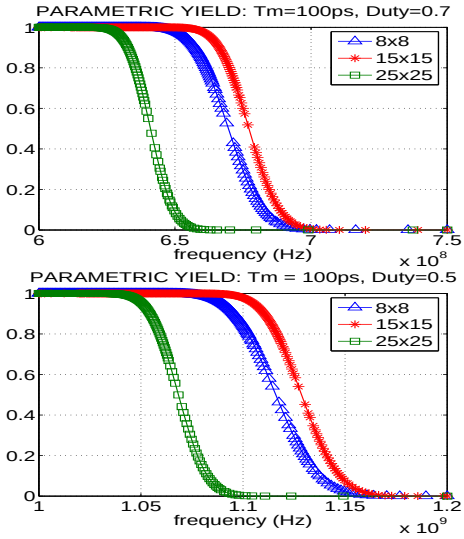


**Figure 8: Parametric yield of different interconnections as a function of clock frequency. Simulations have been carried out with $T_m = 100ps$ and duty-cycles 0.7 and 0.5 respectively.**

$$\overline{T_{3D,-}} = \sum_j d_{0,j}; \tag{6}$$

$$\sigma^2_{3D,-} = \sum_{i,j} k^2_{i,j} + \sum_j k^2_{3D,j}. \tag{7}$$

where $j$ indicates the $j$-th block of the path.

For the signal path analysis, two vertical propagation are considered: clock and data. The presented definitions are strictly valid under the assumption of a full correlation among the coupling variations of all the vertical interconnections: this corresponds to the conditions of placing all the interconnections in a small area with respect to chip size; if this assumption is not realistic, $C_{3D,norm}$ differs for all the interconnections and must be decomposed in principal components as well [5][6]. By assuming total correlation and limiting the analysis to the 3D parameters we can express equation (7) as a function of the variances of propagation delays: $\sigma^2_{3D,-} = \sigma^2_{DATA,-} + \sigma^2_{CLK,-} + \rho_{D-,CLK}\sigma_{DATA,-}\sigma_{CLK,-}$, where $\rho_{3D,-}$ is the correlation coefficient between $T_{DATA,-}$ and $C_{CLK,-}$ and can be $\pm 1$.

### 5.3.2 Results

Two different conditions on the inter-electrode coupling arise from (2-3):

$$r_{3D,-}\sigma_{3D,-}C_{3D,norm} > \overline{\Delta T_-} - T_{-,m}; \tag{8}$$

where $r_{3D,-}$ is the sign of the correlation coefficient of $T_{3D,-}$

| | Extraction | | Characterization | |
|---|---|---|---|---|
| | SINGLE | CROSS | SINGLE | CROSS |
| 8x8$\mu m^2$ | 13.5s | 154s | 8s | 16.5s |
| 15x15$\mu m^2$ | 66s | 487s | 8s | 16.5s |
| 25x25$\mu m^2$ | 308s | 3430s | 8s | 16.5s |

**Table 3: Iteration-times of Monte Carlo analysis related to parasitic extraction and circuit characterization (SPICE). The timings are shown for a single channel and for cross-talk simulations as well.**

and $C_{3D,norm}$, $\pm 1$ are its possible values. In the 3D connect application, $r_{3D,TX} = -1$ and $r_{3D,PRE} = 1$ so that yield can be analytically expressed as:

$$Y_T = \frac{1}{2} erfc\left(\frac{T_{TX,m} - \overline{\Delta T_{TX}}}{\sigma_{3D,TX}\sqrt{2}}\right) + \\ -\frac{1}{2} erfc\left(\frac{\overline{\Delta T_{PRE}} - T_{PRE,m}}{\sigma_{3D,PRE}\sqrt{2}}\right) \quad (9)$$

when

$$\frac{\overline{\Delta T_{PRE}} - T_{PRE,m}}{\sigma_{3D,TX}} > \frac{(T_{TX,m} - \overline{\Delta T_{TX}}}{\sigma_{3D,TX}};$$

$Y_T = 0$ otherwise. If $r_{3D,TX} = r_{3D,PRE}$, $Y_T$ can be similarly computed with just the worst case condition between both relations summarized in (8).

Results for 8x8$\mu m^2$, 15x15$\mu m^2$ and 25x25$\mu m^2$ capacitive channels are presented in Figure 8: the results are related to $T_{TX,m} = T_{PRE,m} = 100ps$ and clock duty-cycle equal to 0.5 and 0.7. Figure 8 points out the relation between electrode-size and performance: in order to get the maximum performance we have to exploit the trade-off between large inter-electrode coupling (25x25$\mu m^2$) and small parasitics (8x8$\mu m^2$); the intermediate electrode (15x15$\mu m^2$) shows the best parametric yield.

## 6. CONCLUSIONS AND FUTURE WORK

A statistical analysis for 3D capacitive interconnects has been presented in this paper. Data were extracted from a sample of manufactured 3D capacitive interconnect assemblies and compared with the analytical analysis. Since the vertical path is fully embedded in the transmitter-receiver sub-domain, the analysis can be limited to the vertical link. The assembly procedure does not affect the standard manufacturing process, so the inter-electrode capacitance can be decoupled from all others sources of variation. A statistical timing analysis was applied to evaluate bit-rate constraints. Conditions on capacitance variability were given to offer reliable interconnections.

Future work will involve reducing extraction time for inter-electrode parasitics and a more accurate variance estimation by exploiting analytical models and optimized Monte Carlo methods, and improving yield prediction by including non-linearities.

## 7. ACKNOWLEDGMENTS

Acknowledgments omitted for blind review.

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