System Level Signal and Power Integrity Analysis Methodology for System-In-Package Applications

ABSTRACT

This paper describes a methodology for performing system level signal and power integrity analyses of SiP based systems. The paper briefly outlines some new modeling and simulation techniques that have been developed to enable the proposed methodology. Some results based on the application of this methodology on test systems are also presented.

Keywords

Causality, modal decomposition, nodal admittance matrix method, power integrity, signal integrity, System-In-Package (SiP), finite difference method.

1. INTRODUCTION

The increasing performance and miniaturization requirements in the electronics industry have resulted in an underlying trend towards convergent systems. Such systems bring about functional integration and reduction in size through a variety of technology platforms like system-on-chip (SoC), multi-chip modules (MCM), system-in-package (SiP) etc., depending on which is most suitable for the application. Among these technologies, SiP provides a platform for integration of multiple dies and passives onto a single package using a range of technologies from new materials and processes to novel designs and techniques. Figure 1 shows the schematic diagram of a SiP with integrated RF / Digital, embedded passives and Electromagnetic Band Gap (EBG) structures. Such SiP based structures considerably increase the system complexity thereby giving rise to new signal and power integrity problems. To deal with these issues requires new EDA tools and techniques that can: 1) accurately model and analyze complex SiP structures, 2) accurately simulate the parasitic effects in the system, and 3) efficiently handle large sized problems so as to enable system level analysis and simulation. This paper describes a methodology for performing system level signal and power integrity analyses of SiP based systems. The paper also briefly outlines some new modeling and simulation techniques that have been developed that enable the proposed methodology.

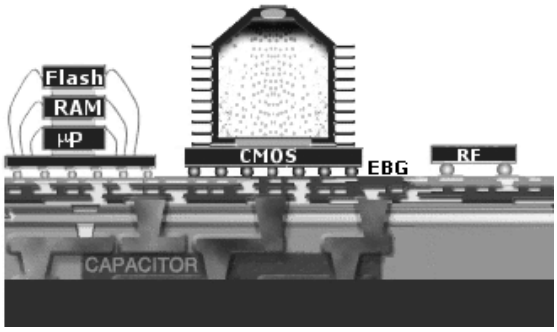

Figure 1. Schematic diagram of a system- in-package (SiP)

Section 2 outlines a novel methodology for Signal – Power Co-simulation. Section 3 describes the analysis of PDN using a modified circuit based modeling technique. The technique is successfully used in analyzing an EBG structure to obtain its response and the results are validated with measurements. Section 4 describes the integration of the PDN and the SDN using the nodal admittance matrix and modal decomposition techniques. Section 5 describes the delay extraction technique and the simulation of the integrated system response using signal flow graphs. The results obtained using the proposed methodology on a

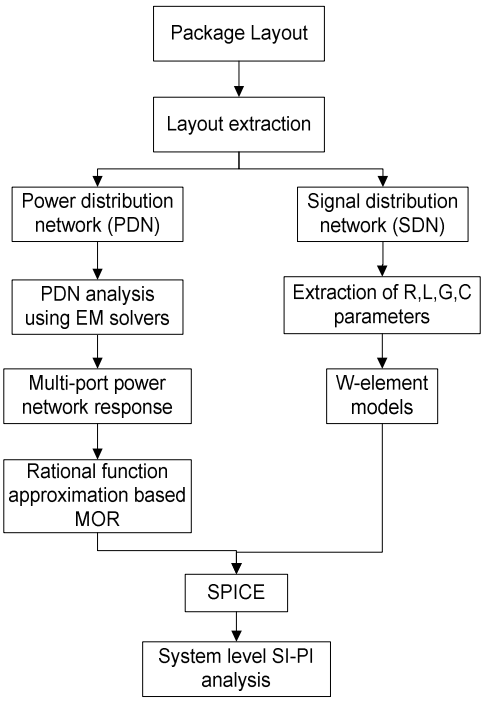

Figure 2. Flowchart for system level SI-PI analysis

variety of test structures are discussed in section 6. Finally, the conclusion along with some considerations is presented in section 7.

2. PROPOSED METHODOLOGY

Traditionally, in packaged systems the analyses of the signal distribution network (SDN) and the power distribution network (PDN) have been carried out independently. Once the layout of a system is available, geometrical information is extracted to obtain models for the PDN and the SDN separately. However it is known that effects like simultaneous switching noise (SSN) that occur in the PDN can affect the quality of the signal that propagates through the SDN. Analyzing the two networks separately fails to account for these effects accurately and hence compromises on the quality of the SI analysis. One possible solution for this problem is using macro-modeling [1] along with model order reduction (shown in Figure 2) to convert the frequency domain response of a PDN into a SPICE compatible format that can be combined with SPICE based SDN models to carry out a system co-simulation. Although this addresses some of the issues concerning the system parasitics, macro-modeling has its own limitations. Typically macro-modeling requires some function based approximation of the frequency response data which limits the size of the problem (in terms of ports and bandwidth) that can be handled. Furthermore, macro-models obtained using bandlimited frequency response data are unable to accurately capture distributed effects like delay leading to causality violations in the transient simulations [2]. Another problem with the flowchart shown in Figure 2 is that the PDN analysis is typically done using EM solvers. This is extremely time consuming and limits the size of the structures that can be simulated. To address this problem, several circuit based modeling techniques have been proposed in literature to reduce the PDN simulation time [3]. However with increasing complexity of SiP based structures, like electromagnetic band gap (EBG) structures that are used to provide isolation, EM effects like fringing fields and gap discontinuities become increasing dominant. Some of these modeling methods are unable to accurately capture these effects. Hence there is a need for a SI-PI analysis methodology for SiP based applications that can effectively address the above issues. The methodology proposed in this paper (shown in Figure 3) provides an efficient and reliable way of analyzing SiP structures by using novel modeling and simulation techniques. The initial steps in the methodology (shown using shaded boxes) are the same as those shown in Figure 2 and use existing techniques for layout extraction and interconnect modeling. However the proposed methodology uses a modified modeling approach for analyzing the PDN. The approach accurately models structural discontinuities and is able to extract multi-port response of the PDN. The PDN and SDN responses are then integrated using the Nodal Admittance Matrix (NAM) method and modal decomposition techniques. This ensures that all the coupling between the SDN and the PDN is accurately captured in the simulation. The integrated system response is then transformed to obtain a reduced-order model of the system. This reduced order model captures all the system parasitics and can be efficient simulated using signal flow graphs. The signal flow graph formulation includes a delay extraction technique that enables the enforcement of causality on the transient simulation.

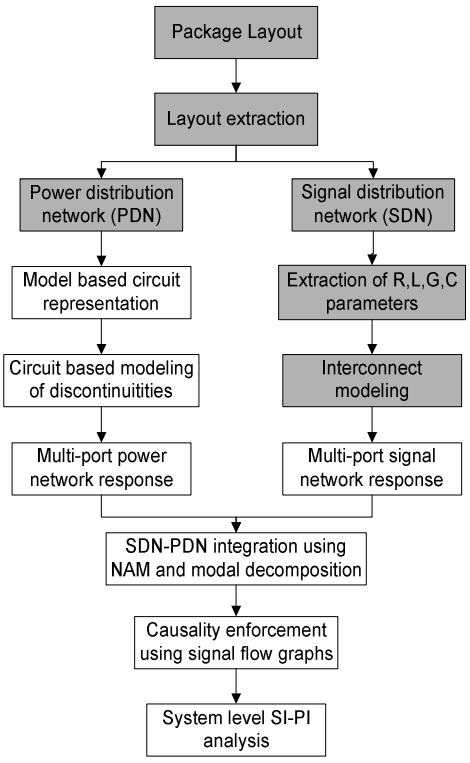

Figure 3. Proposed methodology for system level SI-PI analysis

3. ACCURATE NAM BASED MODELING OF THE PDN

In the past circuit based techniques have been proposed as a replacement to 3D full wave analysis of package PDNs [3], which is computationally expensive. These circuit techniques are based on the Finite Difference Frequency Domain (FDFD) solution of the Helmholtz equation. A given PDN structure can be meshed into a grid of square "unit cells", with an equivalent circuit representation for each cell, as shown in Figure 4. From the lateral dimension of a unit cell (w), separation between planes (d), permittivity (ε), permeability (μ), loss tangent of dielectric (tan (δ)), metal thickness (t), and metal conductivity (σ_c), the equivalent circuit parameters of a unit cell can be computed from the following equations:

$$C = \varepsilon_o \varepsilon_r \frac{w^2}{d}, L = \mu_o d, R_{dc} = \frac{2}{\sigma_c t}, R_{ac} = 2\sqrt{\frac{\pi f \mu_o}{\sigma_c}}(1+j), G_d = wC\tan\delta \quad (1)$$

In the above equation, ε_o is the permittivity of free space, μ_o is the permeability of free space, and ε_r is the relative permittivity of the dielectric. The parameter R_{dc} is the total resistance of both the power and ground planes for a steady DC current, where the planes are assumed to be of uniform cross-section. The AC resistance R_{ac} accounts for the skin effect on both conductors. The shunt conductance G_d represents the dielectric loss in the material

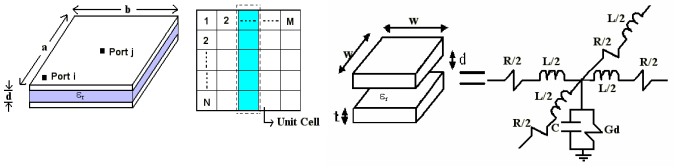

Figure 4. Circuit model generation for the package PDN

between planes. This FDFD based approach converts an electromagnetic problem into a much simpler circuit problem, which can be solved by existing techniques such as the Nodal Admittance Matrix method (NAM) or the Transmission Matrix method (TMM)[3].

FDFD is efficient for analyzing large continuous metal planes, and can be extended to take into account second order effects such as fringe and gap fields. Accurate modeling of such effects can be important in the context of structures employed for isolation. Isolation of subsystems in SiPs is becoming more and more important with increased RF - digital integration. Split planes and Electromagnetic Band Gap (EBG) structures are being increasingly employed to provide this isolation. An edge discontinuity results in fringing fields, the effect of which is not captured by the parallel plate formula for capacitance given in (1). The fringe effect is especially pronounced when there are narrow connections (comparable to the dielectric thickness) between two metal patches. Also, the gap effect leads to coupling between two physically isolated metal planes on the same layer. The gap effect becomes important as the distance of separation between two metal patches becomes smaller. The basic TMM technique does not capture the effect of coupling across a gap, and will show perfect isolation between two separated metal patches. In reality, there can be significant coupling, especially at a frequency when the patches resonate. With the EBG structure, the existing method will overestimate both bandwidth and isolation. Hence, both these effects become important for accurate analysis of package PDNs.

The fringe effect can be modeled by adding a fringe capacitor, C_f, and a fringe inductance, L_f, to unit cells that lie along an edge. The total per unit length capacitance (C_T) including fringing capacitance (C_f) along a given cross section of the structure can be calculated by employing the empirical formula for the per unit length capacitance of a microstrip line described in the paper [4] given by:

$$C_T = \varepsilon_o \varepsilon_{eff}\left[\left(\frac{W}{d}\right) + 0.77 + 1.06\left(\frac{W}{d}\right)^{0.25} + 1.06\left(\frac{t}{d}\right)^{0.5}\right] \quad (2)$$

where ε_{eff} is the effective dielectric constant given by

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + 12\frac{d}{W}}} \quad (3)$$

,W is the width of the metal along the cross section, t is the metal thickness and ε_r is the dielectric constant of the substrate. The first term in (2) represents the parallel plate capacitance, while the remaining three terms represent the additional fringing capacitance. In order to maintain a physical phase velocity, the per unit length inductance must be reduced from the parallel-plate inductance in accordance with

$$\sqrt{LC} = \sqrt{\mu\varepsilon} \quad (4)$$

This reduction is accomplished by adding an inductance in parallel between two adjacent nodes on the edge of the structure. The gap capacitance can be modeled by including a gap capacitance, Cg, between nodes across a gap. The addition of the fringe and gap elements is shown in Figure 5. The gap capacitance can be extracted from a 2-D solver such as Ansoft Maxwell™. For example, the gap capacitance per unit length extracted from Maxwell for the Alternating Impedance-EBG (AI-EBG) structure in Figure 6 was 6.7 pF/m.

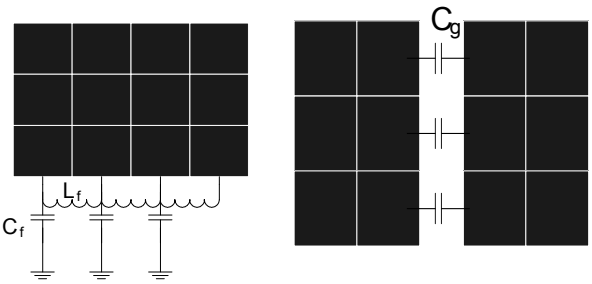

Figure 5. Circuit models for the fringe and gap effects

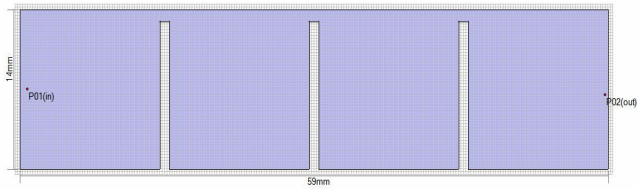

Figure 6. Example AI-EBG structure

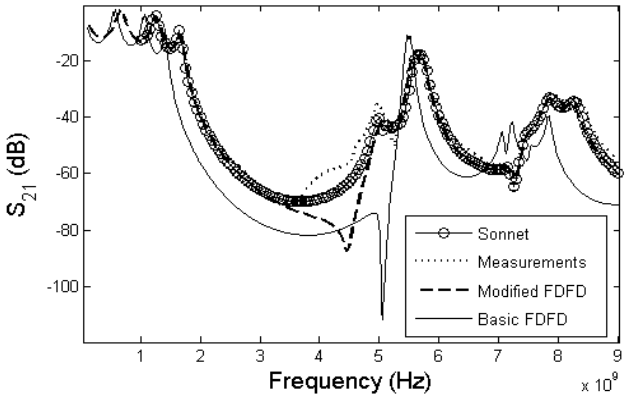

Figure 7. Simulated and measured S21 for EBG

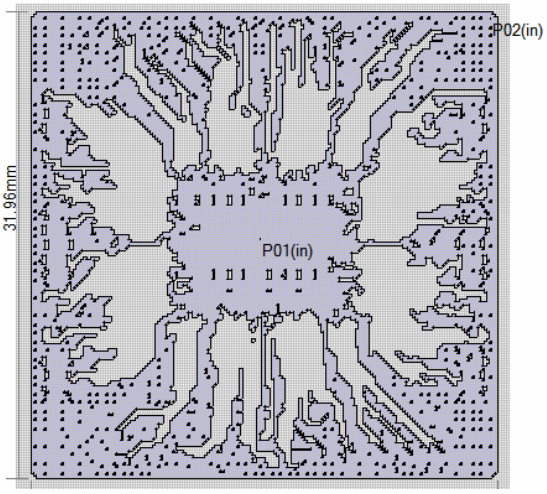

Figure 8. Example FDFD model of a package structure

The simulated and measured S-Parameters for this EBG structure are shown in Figure 7. FDFD including fringe and gap fields

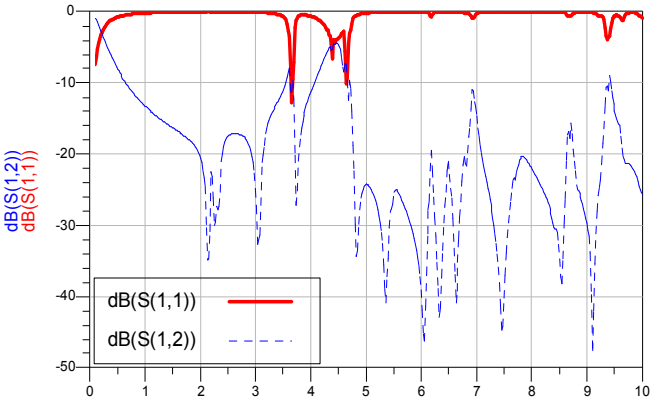

Figure 9. Simulated S parameters for the Package layer of Fig. 7

gives excellent correlation with measurements. The time required for simulation of 300 data points was 172 seconds in an Intel Xeon 3.2 GHz workstation with a system memory of 3.5 GB. It can be seen that the basic FDFD overestimates bandwidth of the stop band. Comparable simulations with the full wave method of moments based EM solver, Sonnet, required 19 hours of simulation time. This circuit method also scales well with problem size. This is because the nodal admittance matrix is sparse and can be solved for the impedance parameters efficiently with sparse solvers. A real-world example is shown in Figure 8, which is the meshed model for a package layer from Altera Corp. This example contains approximately 25,000 nodes and the entire frequency response, from 0.1 GHz to 10 GHz was obtained in 84.3 seconds. The S parameters between ports 1 and 2, defined between the center and one of the corners of the layer, are shown in Figure 9.

4. INTEGRATION OF THE SDN AND THE PDN

Since separate analyses of the SDN and the PDN fails to account for the coupling between the two modules, the two responses need to be integrated to perform an accurate system level analysis. This integration can be performed using the admittance matrices of the two modules along with the stamp rule [5]. The process involves conversion of the SDN response into its equivalent model which is then stamped onto the admittance matrix of the PDN. For example, in Figure 10, a microstrip transmission line referenced to non-ideal power ground planes is replaced with the model shown in Figure 11. This model is then stamped on to the admittance matrix of the power/ground planes by taking into consideration the appropriate modal decomposition technique. This ensures that all parasitic effects between the PDN and the SDN are accurately accounted for in the integration process. For example in a simple microstrip interconnect referenced to non-ideal power ground

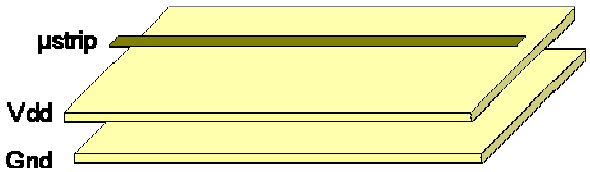

Figure 10. A microstrip-line referenced to a non-ideal power-ground plane

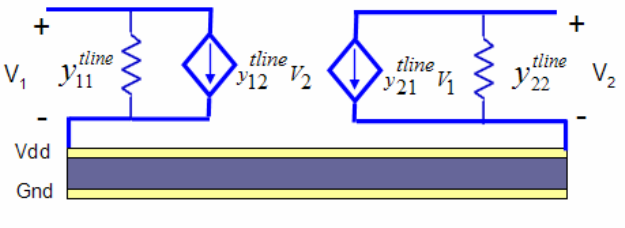

Figure 11. Equivalent two port model of microstrip line

planes (see Figure 10), since the transmission line and parallel-plate modes are not coupled, the integration of the SDN and the PDN responses can be carried out simply by combining the two Y-matrices as given by

$$\begin{bmatrix} I_p^i \\ I_p^o \\ I_m^i \\ I_m^o \end{bmatrix} = \begin{bmatrix} Y_p & 0 \\ 0 & Y_m \end{bmatrix} \begin{bmatrix} V_p^i \\ V_p^o \\ V_m^i \\ V_m^o \end{bmatrix} \quad (5)$$

where Y_p and Y_m are the Y-matrices of the power/ground planes and the microstrip interconnect (considering ideal reference) respectively, while I and V are the vectors defining the currents and the voltages at the input and output ports. However if the current on the signal line excites both modes, like in the case of a stripline interconnect referenced to non-ideal power/ground planes, additional considerations [6] are required to integrate the SDN and the PDN responses. For the stripline case, the SDN and the PDN responses can be integrated as given by

$$\begin{bmatrix} I_p^i \\ I_p^o \\ I_m^i \\ I_m^o \end{bmatrix} = \begin{bmatrix} k^2 Y_s + Y_p & kY_s \\ kY_s & Y_s \end{bmatrix} \begin{bmatrix} V_p^i \\ V_p^o \\ V_m^i \\ V_m^o \end{bmatrix} \quad (6)$$

where Y_p and Y_s are the Y-matrices of the power/ground planes and the stripline (considering ideal reference) respectively, and k is constant determined from the layout.

Once the integration is complete, line terminations and other lumped components in the system can be added to the overall system matrix using the stamp rule. Since the transient response is often required only at particular locations in the system, the overall system matrix can be reduced to include ports only at those locations where the system is being excited or probed. For a m-port overall system matrix that needs to be reduced to n (external) ports, the m-port Y-matrix is reordered such that the desired n port locations appear in the top left corner of the matrix. This is shown in Equation 7 where Y_{ee} and Y_{ii} refer to the internal and external (required) ports respectively.

$$\begin{bmatrix} Y_{11} & \cdots & Y_{m1} \\ \vdots & \ddots & \vdots \\ Y_{1m} & \cdots & Y_{mm} \end{bmatrix} \rightarrow \begin{bmatrix} [Y_{ee}]_{nxn} & [Y_{ei}]_{nx(m-n)} \\ [Y_{ie}]_{(m-n)xn} & [Y_{ii}]_{(m-n)x(m-n)} \end{bmatrix} \quad (7)$$

From this reordered Y-matrix, the reduced n-port representation of the system is obtained using the Equation

$$[Y]_{nxn} = Y_{ee} + Y_{ei}(-Y_{ii}^{-1} Y_{ie}) \quad (8)$$

The reduced-order system matrix thus obtained is then used for estimating the port-to-port delays in the system to enforce causality on the transient response.

5. CAUSAL TRANSIENT SIMULATION USING SIGNAL FLOW GRAPHS

The reduced multi-port Y-parameters are converted to S-parameters for simulation using signal flow graphs (SFGs). A novel technique for extracting port-to-port delay from the frequency response of a passive structure is proposed in [2]. The technique makes use of the minimum-phase property of passive systems in conjunction with the Hilbert Transform and involves the separation of the transfer responses of a system into minimum phase and all-pass components. Based on the theory described in [2], if Td is the port-to-port delay for a 2-port passive network described by its S-parameters, the delay extraction process can be described as follows:

$$|S12_{\min}(j\omega)| = |S12(j\omega)| \tag{9}$$

$$\arg[S12_{\min}(j\omega)] = -\frac{1}{2\pi}\mathrm{P}\int_{-\pi}^{\pi}\log|S12(j\theta)|\cot\left(\frac{\omega-\theta}{2}\right) \tag{10}$$

$$S12_{AP}(j\omega) = \frac{S12(j\omega)}{S12_{\min}(j\omega)} = e^{-j\omega Td} \tag{11}$$

$$Td = -\frac{\arg(S12_{AP}(j\omega))}{\omega} \tag{12}$$

where S12 is the transfer response of the network under consideration, and $S12_{min}$ and $S12_{AP}$ are its minimum phase and all-pass components respectively such that S12 = $S12_{min}$*$S12_{AP}$. Equation 9 follows from the unity magnitude property of the all-pass component while Equation 10 is obtained using the Hilbert Transform for minimum phase systems. The methodology described in this paper uses the delay thus extracted to obtain causal signal flow graph equations for transient simulation of passive networks.

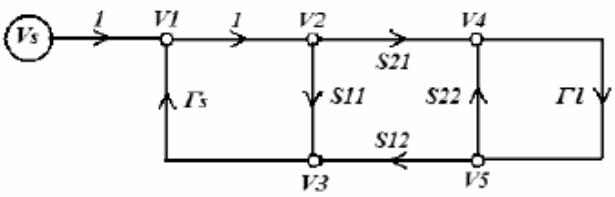

Figure 12. A sample signal flow graph

Signal flow graphs (SFGs) have been previously used in the transient simulation of passive systems [7]. One of the key advantages they provide is that it is possible to perform transient simulation without any kind of approximation/interpolation of the frequency response data. Since this approximation step is a key bottleneck for the scalability of macro-modeling techniques, signal flow graphs are capable of handling larger sized simulation problems. To demonstrate the enforcement of causality on transient simulation using signal flow graphs, a simple SFG shown in Figure 12. The SFG results in a system of equations which need to be solved in order to generate the transient response of the circuit. These equations are given as

$$V_1(t) = V_S(t) + V_3(t) \otimes \Gamma_S \tag{13}$$

$$V_2(t) = V_1(t) \tag{14}$$

$$V_3(t) = V_2(t) \otimes s11(t) + V_5(t) \otimes s12(t) \tag{15}$$

$$V_4(t) = V_2(t) \otimes s21(t) + V_5(t) \otimes s22(t) \tag{16}$$

$$V_5(t) = V_4(t) \otimes \Gamma_L \tag{17}$$

Now if the port-to-port delays of the system are known, via the extraction process described above, Equations 15 and 16 can be re-written as

$$V_3(t) = V_2(t) \otimes s11(t) + V_5(t - Td) \otimes s_{min}12(t) \tag{18}$$

$$V_4(t) = V_2(t - Td) \otimes s_{min}21(t) + V_5(t) \otimes s22(t) \tag{19}$$

This new system of equations explicitly enforces the delay and the resulting solution enforces causality on the transient simulation.

One of the disadvantages of the SFG approach is that convolution needs to be performed at each time step. Since convolution is a computationally expensive procedure, requiring $O(N^2)$ operations, it reduces the simulation efficiency of the proposed methodology. One solution to this problem is the implementation of a fast convolution technique that is described in detail in [8]. This technique proceeds by decomposing a convolution integral $y(t) = x(t) \otimes h(t)$, whose discrete time equivalent is

$$\tilde{y}(t_n) = \sum_{i=1}^{n-1} h(t_n - t_i)\alpha_i \tag{20}$$

where $\alpha_i = x(t_i)\Delta t$, into two summations in the form

$$\tilde{y}(t_n) = \sum_{i=1}^{s} h(t_n - t_i)\alpha_i + \sum_{i=s+1}^{n-1} h(t_n - t_i)\alpha_i \tag{21}$$

Of these two summations, the one on the right is evaluated directly while the one on the left is evaluated using an interpolation technique based on Lagrange basis functions (shown in Figure 13). For any lossy system response which essentially decays with time, the number of basis functions required for interpolation is considerably few. If *s* in Equation 21 is sufficiently large as compared to *n*, convolution performed using this technique requires *O(NlogN)* operations. This considerably reduces the simulation time of the proposed methodology.

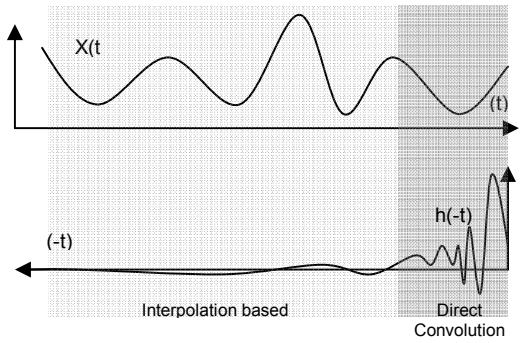

Figure 13. Fast convolution using Lagrange interpolation

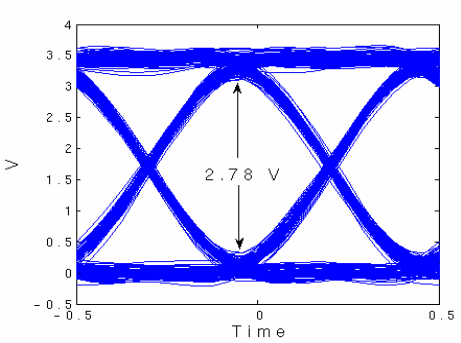

Figure 14. Causal 64-bit bus simulation

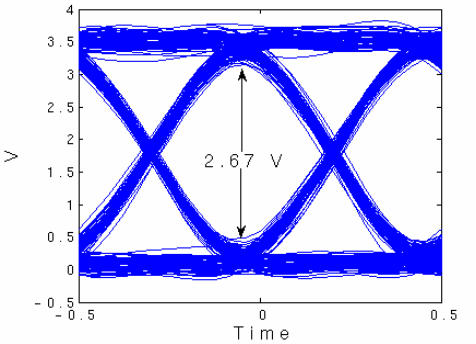

Figure 15. Non-causal 64-bit bus simulation

6. RESULTS

The methodology proposed in this paper was tested to perform SI-PI analysis on a number of packaged systems. In the first case a 64-bit interconnect bus referenced to non-ideal power/ground planes was simulated using random bit pattern excitations on each of the lines. The system output was observed in terms of an eye-pattern obtained on one of the lines. The PDN of the system was modeled using NAM to give a 128 port admittance matrix. The SDN was modeled using the Advanced Design System (ADS) from Agilent. This SDN was then integrated with the PDN using the stamp rule and the consolidated system admittance matrix was reduced to give a 130-port response. Using the SFG based simulation approach this system was simulated to obtain the required eye-pattern. The results are shown in Figure 14.

To demonstrate the effects of causality violations on the signal integrity analysis of a system, the above system was re-simulated without delay extraction and causality enforcement. The results are shown in Figure 15. It can clearly be seen that causality violations result in an artificial eye-closure; in this case of about 110 mV. In the future, as system rise-time increases this problem is expected to worsen.

The other test-case was the simulation of the interconnect network in an IBM HyperBGA package. The signal layer on this package is shown in Figure 16. The aim of the simulation was to analyze the coupling between the SDN and the PDN in the region indicated by the box in Figure 16. As described in this paper, the package layout for the above system was extracted to separate the SDN and the PDN. The PDN was modeled using NAM while the SDN was analyzed using ADS. The two responses were then integrated using modal decomposition given by Equation 6. Finally the consolidated system response was simulated using SFG to perform the required analysis. Figure 16 also shows the

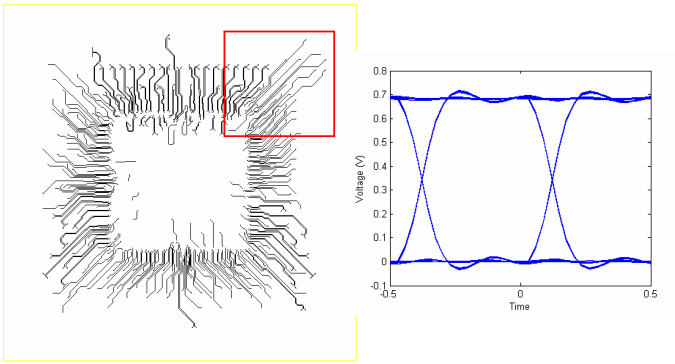

Figure 16. Signal layer on IBM HyperBGA package (left) and the eye-pattern on one of the nets (right)

eye-pattern obtained on one of the signal nets with causality enforcement. For this case, as the SDN is electrically short, the causality violations did not result in a significant eye closure.

7. CONCLUSION

The transition of future systems towards integration and miniaturization based on SiP, has given rise to new SI and PI problems at the system level that include fringing fields, gap discontinuities and causality violations. This paper proposes a system level SI-PI analysis methodology and briefly describes the techniques that have been developed to address these problems. The proposed methodology has been successfully tested on a variety of test-cases including EBG structures, chip packages etc.

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