SiP Activities in ITRI

ERSO/ITRI
廖 錫 卿
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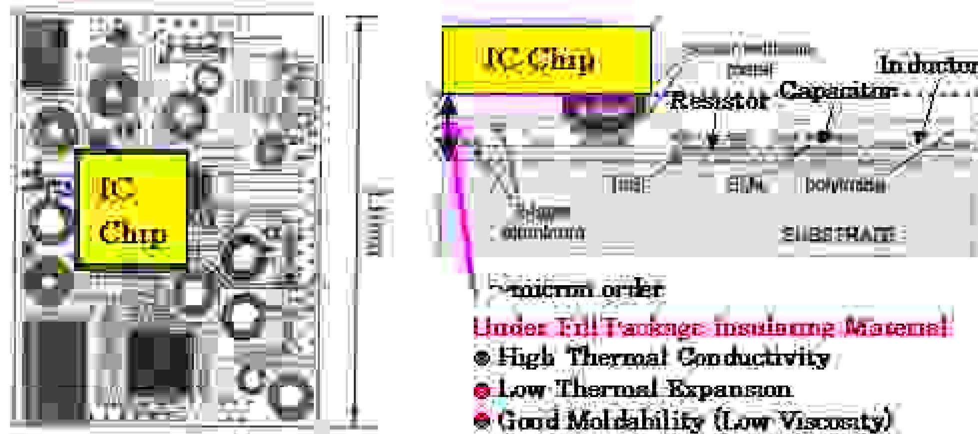
Outline

- SiP Product/Technology Trends & Opportunities
- Bottlenecks & Breakthrough
- SiP Activities in ITRI
- Design Flow & Environment
- Accomplishment in SiP for RF Applications
- Complete Infrastructure of IC Industry
- SiP Consortium
- Strategy
- Action Plan

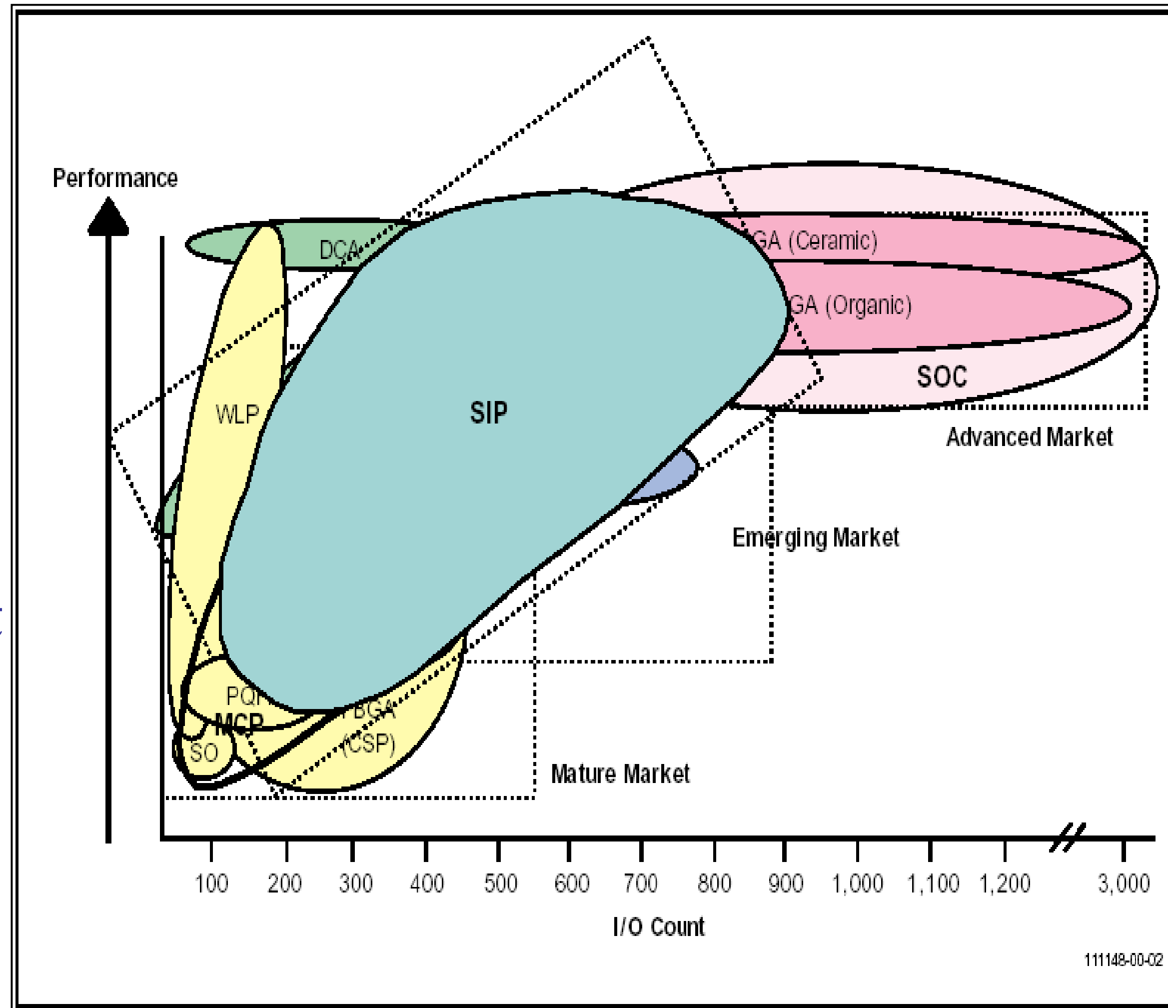
System-in-Package (SiP)

Example (University of California, Santa Cruz)



Why SiP?

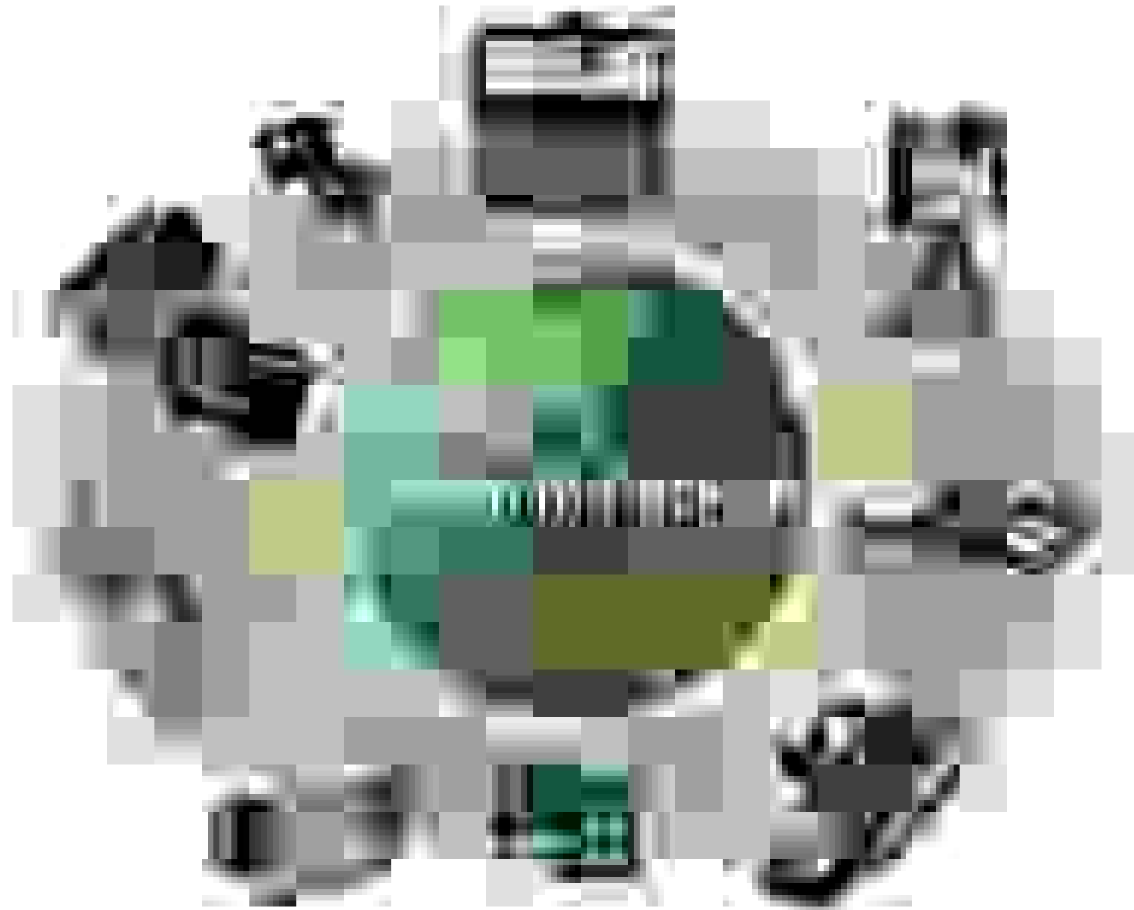
- Product Trends
- Compact in Size
- Highly Integration
- Alternatives for SoC
- Quick Time-to-market



Source: Dataquest 2002

Driving Force: Size, Cost, Performance

More in Handheld Devices :



Technology Trend in Semiconductor Packaging Industry

Chip Protection → *System Integration*

IC Packaging Industry

Production Value: ~US$2.68 B (2002); W-W Market Share: ~32%; Ranked:Top

QFP

TCP

MCM

BGA

Flip Chip

CSP, WLCSP

Carrier Stacking

Chip-in-Film (Flexible)

Chip-in-Substrate (Rigid)

O/E Substrate

3D Packaging

(SiP)

Advanced Integral Substrate

Built-in Functional Substrate

Build-Up Substrate

IC Packaging Substrate

Multi-Layer PCB

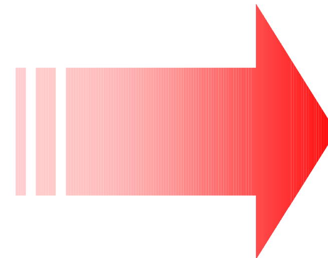
PCB Industry

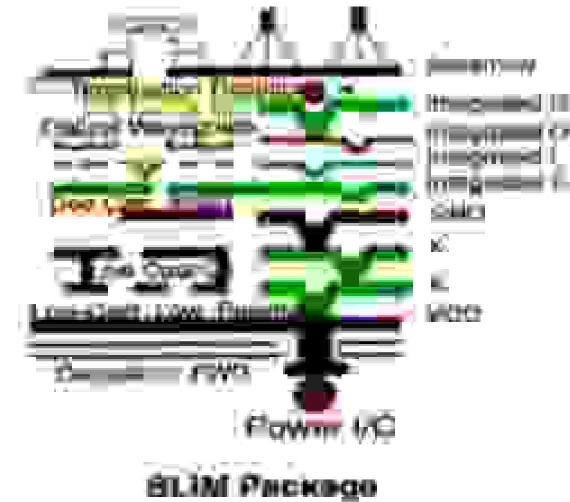
Production Value: ~US$4.27 B (2002); W-W Market Share: ~10%; Ranked: 4th.

1995 2000 2005 2010

Integration of Passives

PRC/GIT Packaging Roadmap	2002	2008	2012
	8%	40%	80%





Dupont Material Roadmap

COST PERFORMANCE PRODUCT SECTOR(PC)	Metric	1999	2001	2003	2009
Total Passives	Elements	1,600	2,100	3,800	5,000
Discretes	%	60%	50%	40%	25%
Arrays/Networks	%	35%	40%	45%	25%
IPDs		5%	7%	9%	10%
Integral Passives		0%	3%	6%	40%

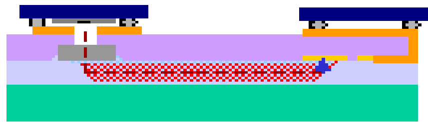
Key Parameters for Passive Components in Hand Held Products

Bottlenecks & Break Through Solutions

Bottleneck		Solution
KGW/KGD	→	CSP/WL-CSP
Hi-Dk/Low Df Material	→	New Material
Form Factor	→	JEDEC Std. vs. Customized
Testing Methodology	→	DFT
EDA Compatibility	→	SiP/SoC EDA Environment
Basic Element Modeling	→	BEM & Characterization
3D Interconnections	→	3D IC Stacking
Thermal Management	→	ex. TE-BGA
Green Package	→	Lead Free
Reliability	→	DFR
Infrastructure	→	Vertical Distribution

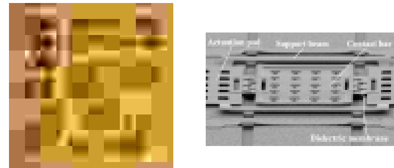
SiP in ITRI

EO Substrate

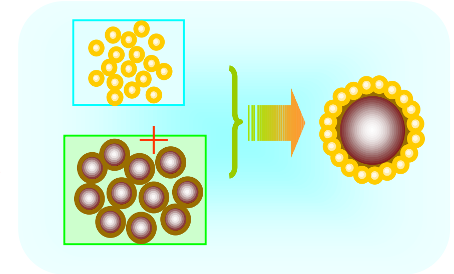


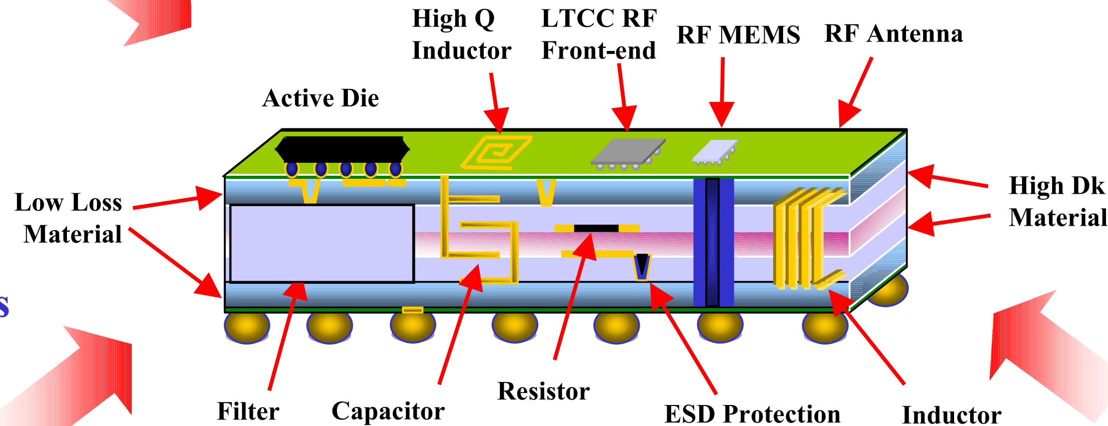
- Optical WG
- Chip in Substrate
- Chip-in-Film
- Polymer Electronics

LTCC/RF-MEMS

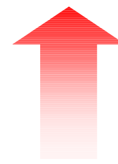


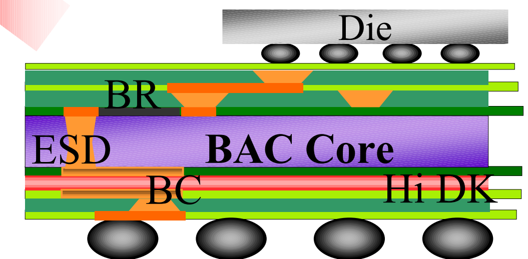
Advanced Material





- Build-in R, L, C
- BAC Core
- Build-in ESD Protection
- Build-in EMI Filter



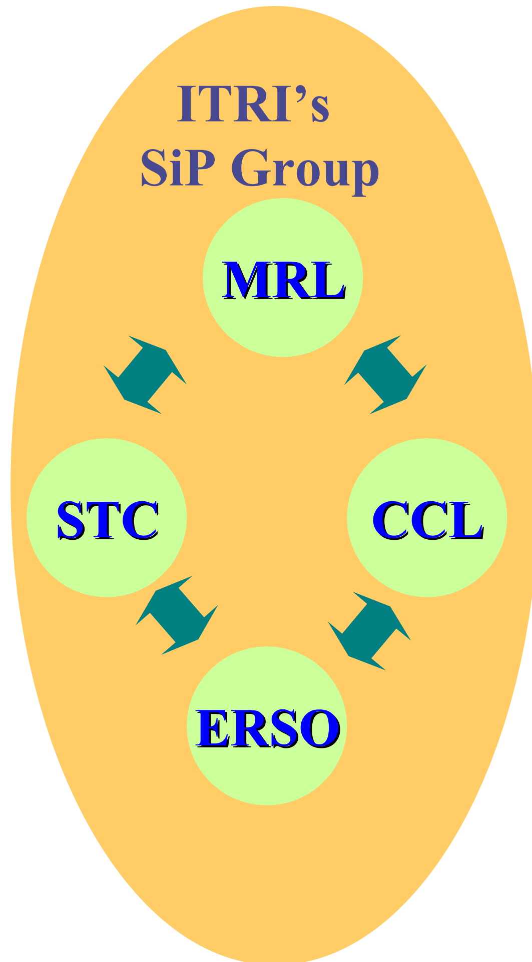


3D/Embedded Actives

Green Packaging

Organic Integral Substrate

SiP in ITRI



MRL: Organic/Polymer/Ceramic Material

STC: SoC Design/Testing

CCL: Protocol, System Partition/Integration

ERSO: SiP Design/Process/Testing, BEM,
Design Environment, Green Packaging,
Thermal/Stress Analysis/Measurement

Advanced Packaging Center/ERSO

Packaging Design

Thermal & Stress Design
- Thermal enhanced packages
- Advanced cooler--TE cooler, heat-pipe
- Low stress packages--Low Dk chip

Electrical Design
- High speed digital application-- Low Noise De-Cap. / Module
- RF application-- RF- SiP & RF-MEMS

Rapid Prototyping
- Physical Engineering & Prototyping
- PCB & substrate layout & Fabrication
- SiP prototyping

Micro-Module Design
- Opto Module design & assembly
- BIO Packaging

→ ITRI/台南科學園區

Packaging Process Technology

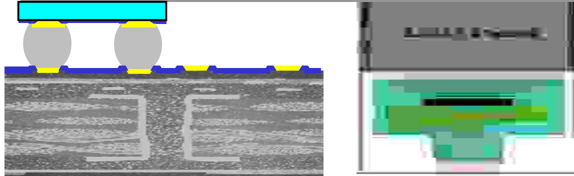
Advanced Process Technology
- Cu and Al Wafer Level Package
- Low cost bumping,Organic Optical waveguide

Micro Structure Analysis
- Failure Mode Analysis
- Substrate Materials evaluation
- Manufacturing Consultant

Assembly Process Technology
- COF, COG
- Flip Chip, 3D Package

Core Packaging Process Lab.

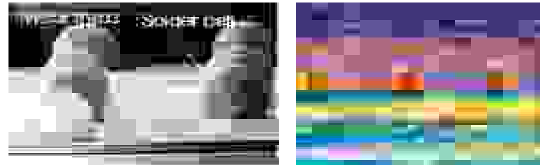
Assembly Process



■ MAJOR EQUIPMENT
- COF bonder
- COG bonder
- OLB bonder
- Flip Chip Bonder
- Dispenser,Cleaner.

■ Application
• COF, COG package
• Flip Chip, 3D Package

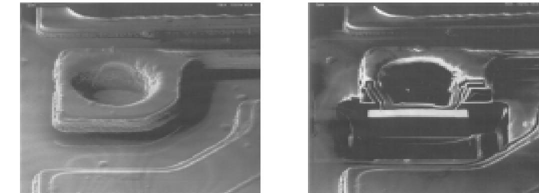
Advanced Process



■ MAJOR EQUIPMENT
• PR Coater / PI Coater / Developer
• Aligner, Sputter, Plater, Printer
• Etcher / Stripper

■ Application
• Cu and Al Wafer Level Package
• Low cost bumping,
• Organic Optical waveguide

μ-Structure Analysis

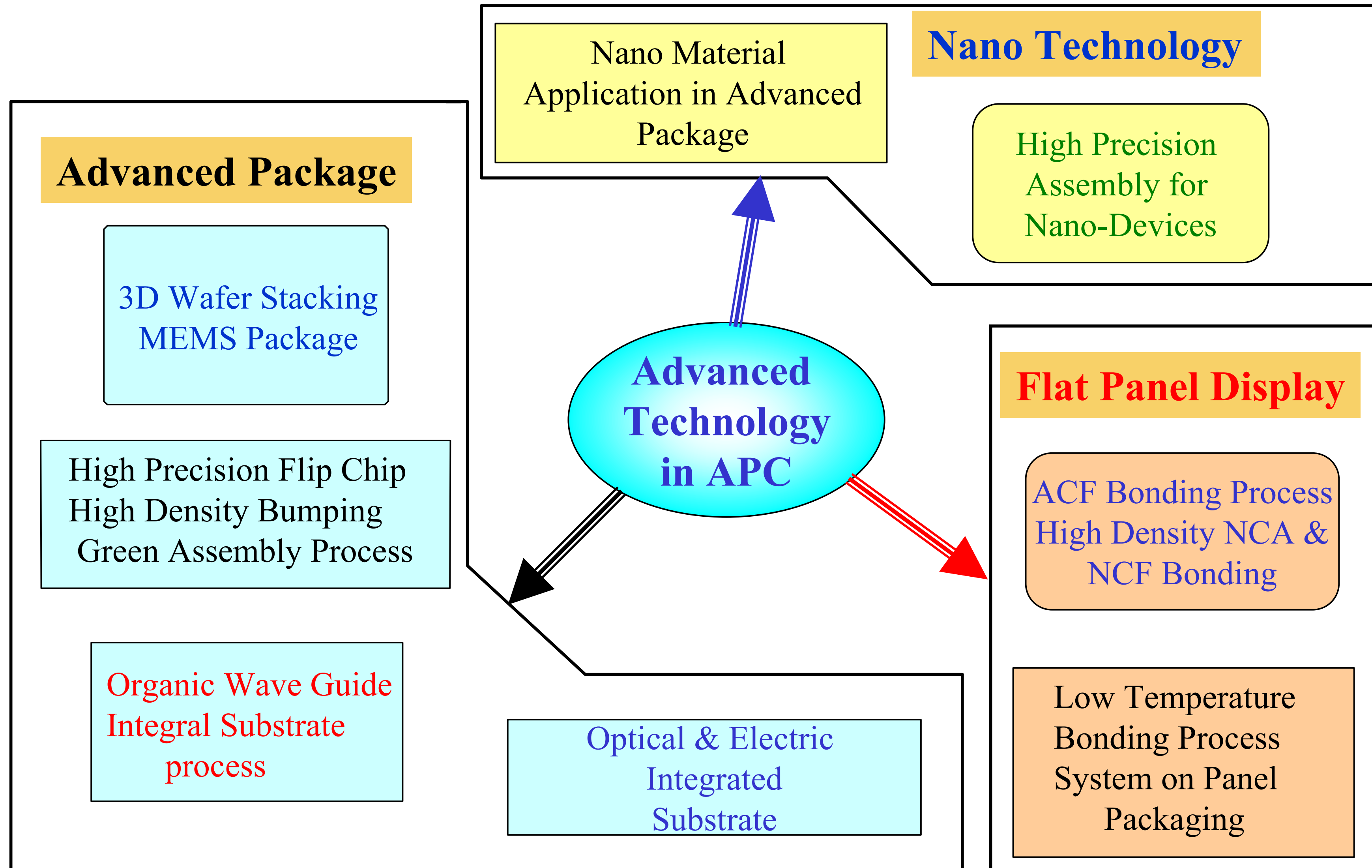


■ MAJOR EQUIPMENT
• TEM / EDS
• FIB
• Auger/ESCA
• SEM / EDS
• SIMS

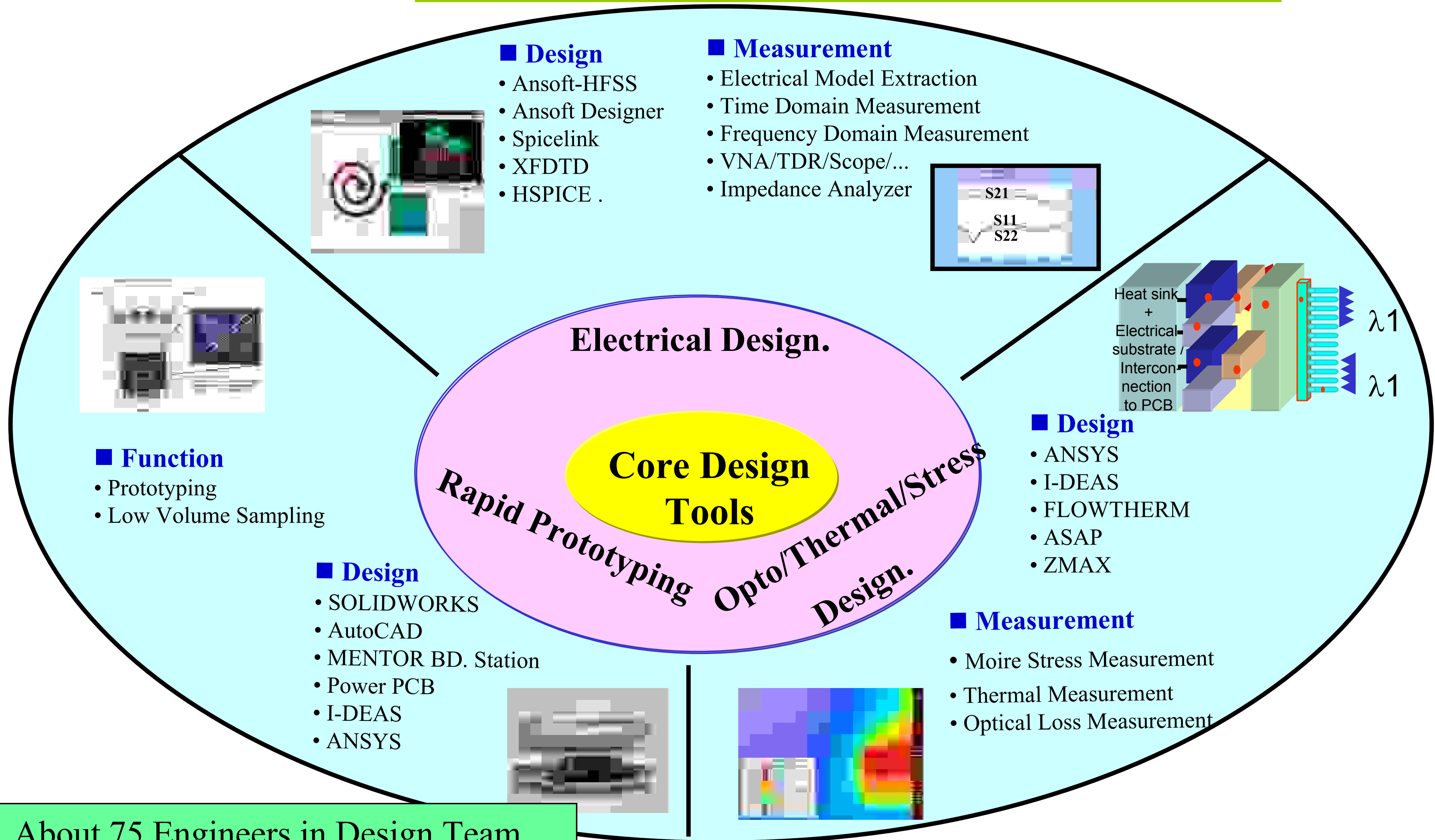
■ Application
•Failure Mode Analysis
•Substrate Materials evaluation
•Manufacturing Consultant

About 50 Engineers in Process Team

Advanced Projects in Process Team

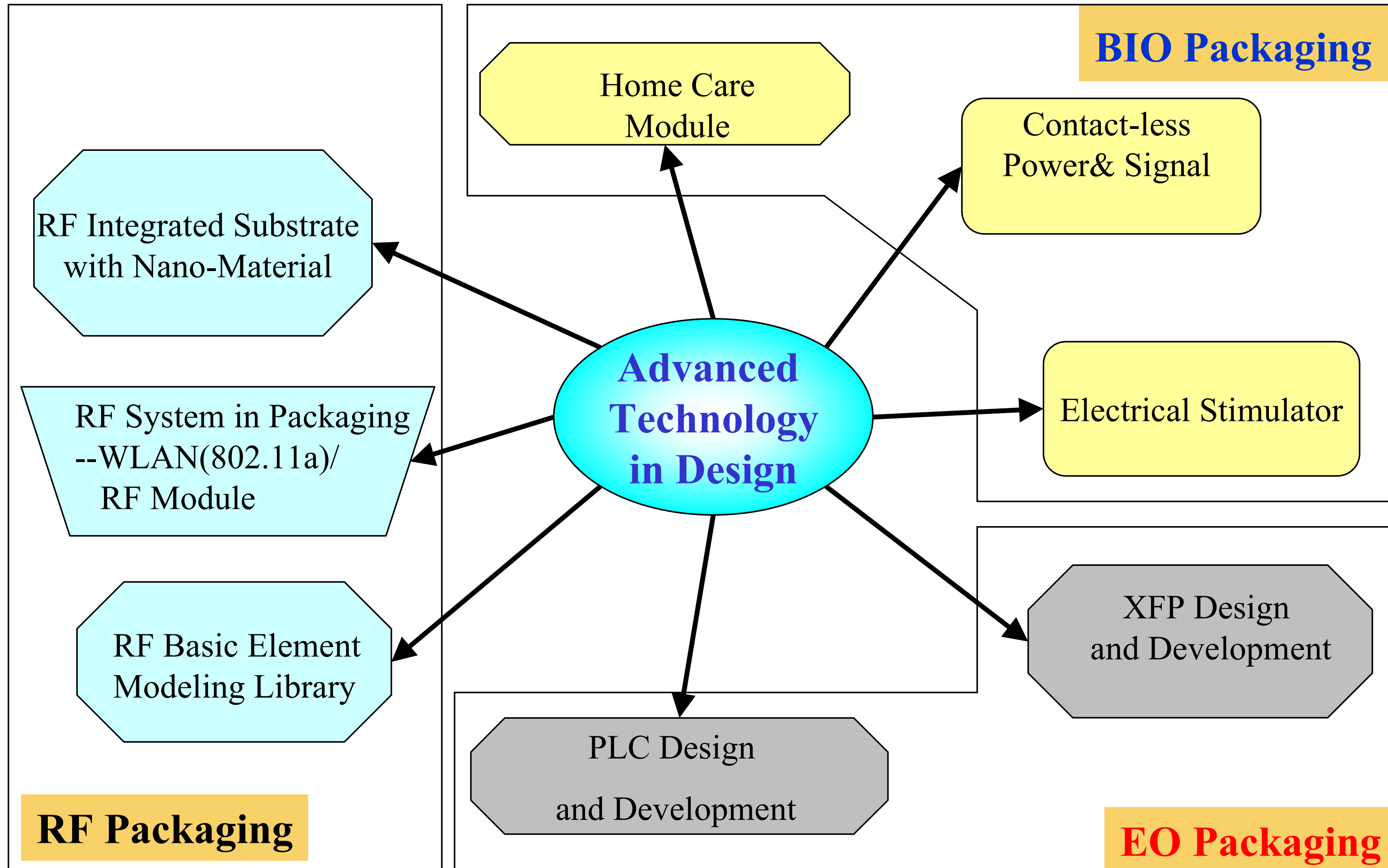


Core Packaging Design Lab.



About 75 Engineers in Design Team

Advanced Projects in Design Team



SiP 快速雛型製作服務 (SiPRPS)

SiPRPS

- Design Service
- ODM Service

- 系統分割
- 裸晶/晶片尺寸構裝來源
- 構裝結構設計
- 熱傳及應力設計
- 邏輯線路設計
- 電性設計及分析
- 基板設計及製程
- 組裝及測試
- 可靠度分析

Products Inquiry

Contract Manufacturing

Bare Chips /CSP

系統模組業

構裝基板業

基板材料業

IC 設計業

IC 封測業

IC 製造業

Technology Transfer

功能基板設計技術
功能基板製程技術
(電子所)

基板內藏元件
材料技術
(材料所)

Current Status

Material/Design/Technology/Integration all in ITRI

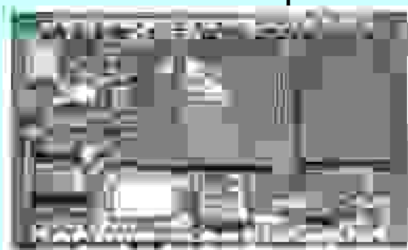
- Hi-DK (**DK=40**@6GHz) Materials Ramping up
- Fine frequency Response up to 6GHz
- Basic Element Model (BEM) <10% @6GHz
- Conventional Low Cost PCB Process
- Embedded Passives for Mixed Circuits

Sanmina/ GIT /Motorola:

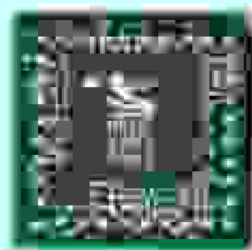
- Hi-DK(DK=22~36@1.9GHz) Premature Materials -- Sanmina, 3M
- Frequency Response up to 6GHz -- GIT
- BEM Modeling -- GIT (Earlier than ITRI),
- Embedded for Analog Circuits Only -- Motorola(Dk4.3@1.9GHz)

2.4 GHz Bluetooth Total Solution

- Worldwide 1st. Announced (ICP-2003)
- Build-in 7 Cap. & 3 Inductors
- 38% Components & 45% Area Reduced

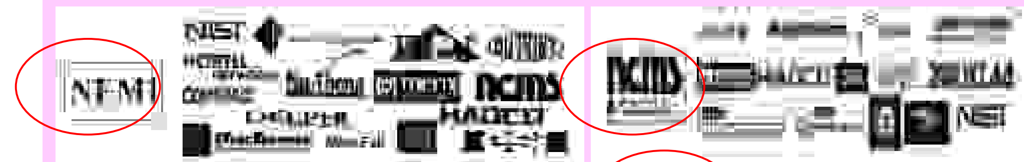


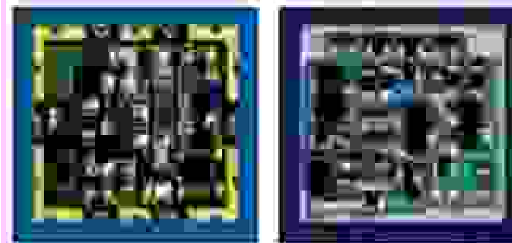
SMD Bluetooth Module (25x15mm^2)



ITRI's Bluetooth in AIS (15x15mm ^{2})

VCO Module for 1.9 GHz GSM





Motorola 1.9GHz Passives Embedded VCO

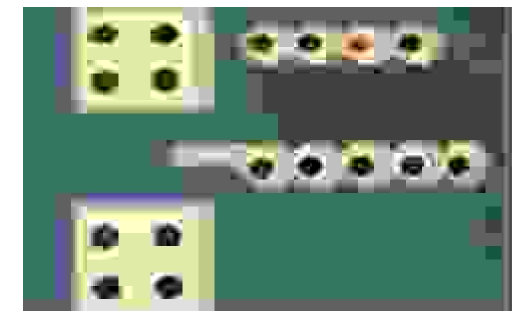
Major Index

- Highest Dk of 40 and keep on improving
- Competitive Df as low as 0.03
- Potentially highest Capacitance Density when thickness being improved in volume production
- Highest manufacturing capability due to nano-composite materials
- Lowest cost due to compatible to current process

Supplier	Sanmina	Sanmina	Vantico	DuPont	3M	MRL/ITRI
Trademark	BC2000	EmCap	CFP	HiK	C-Ply	
Dielectric Material	FR-4	$BaTiO_3$/ epoxy resin	Ceramic/ photodielectric	$BaTiO_3$/ Polyimide	$BaTiO_3$/ epoxy resin	Nano Composite epoxy resin
Thickness, µm	50	100	15~20	25	25	50
Dk @1GHz	4	36	23	11	22	40
Df @1GHz	0.021	0.06	**0.02~0.04**	0.01	0.10	<0.03
Capacitance Density, nF/in^2	0.5	2.1	10	1.5	10	8

- Current Embedded Capacitor Materials

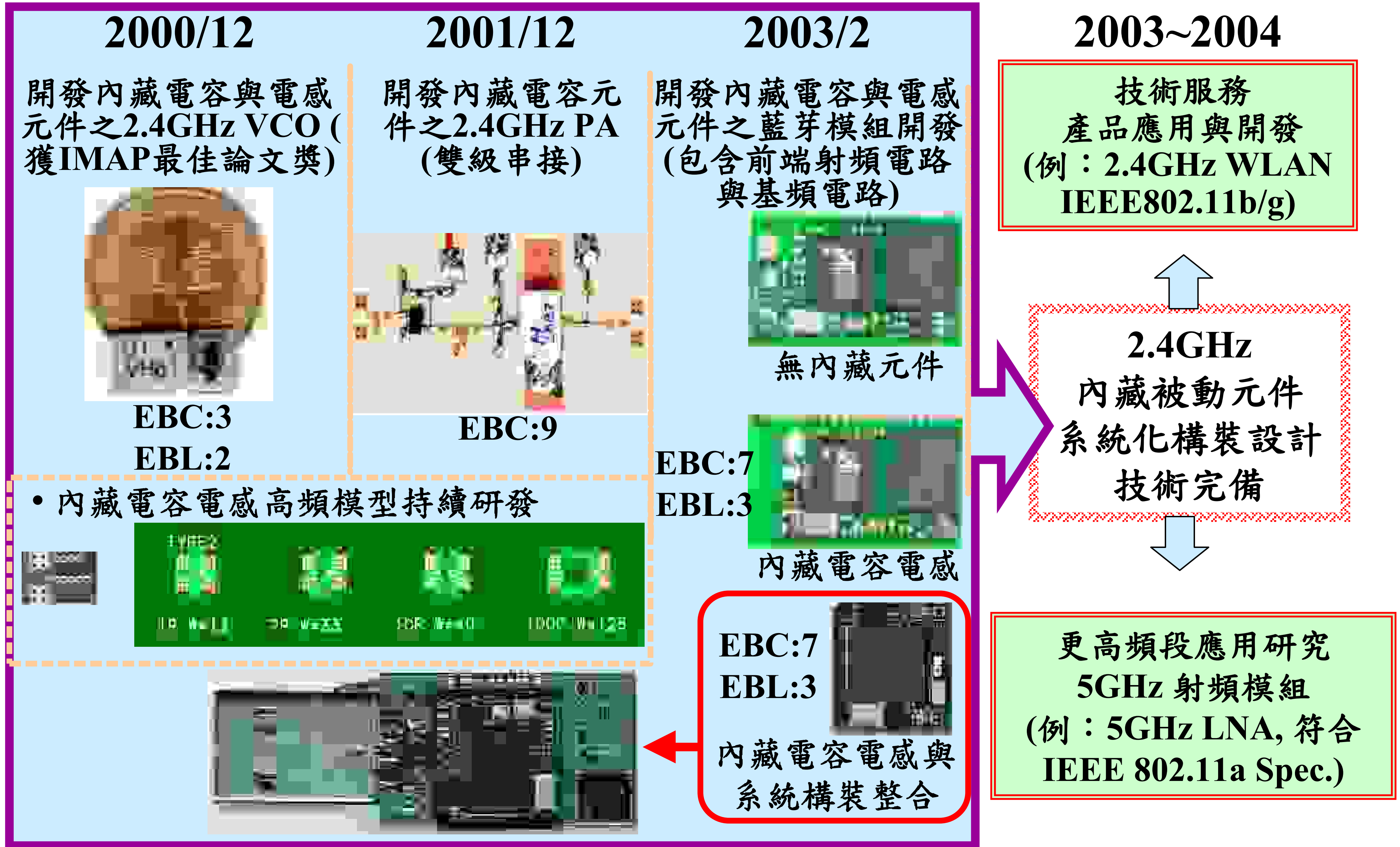
Basic Element Modeling



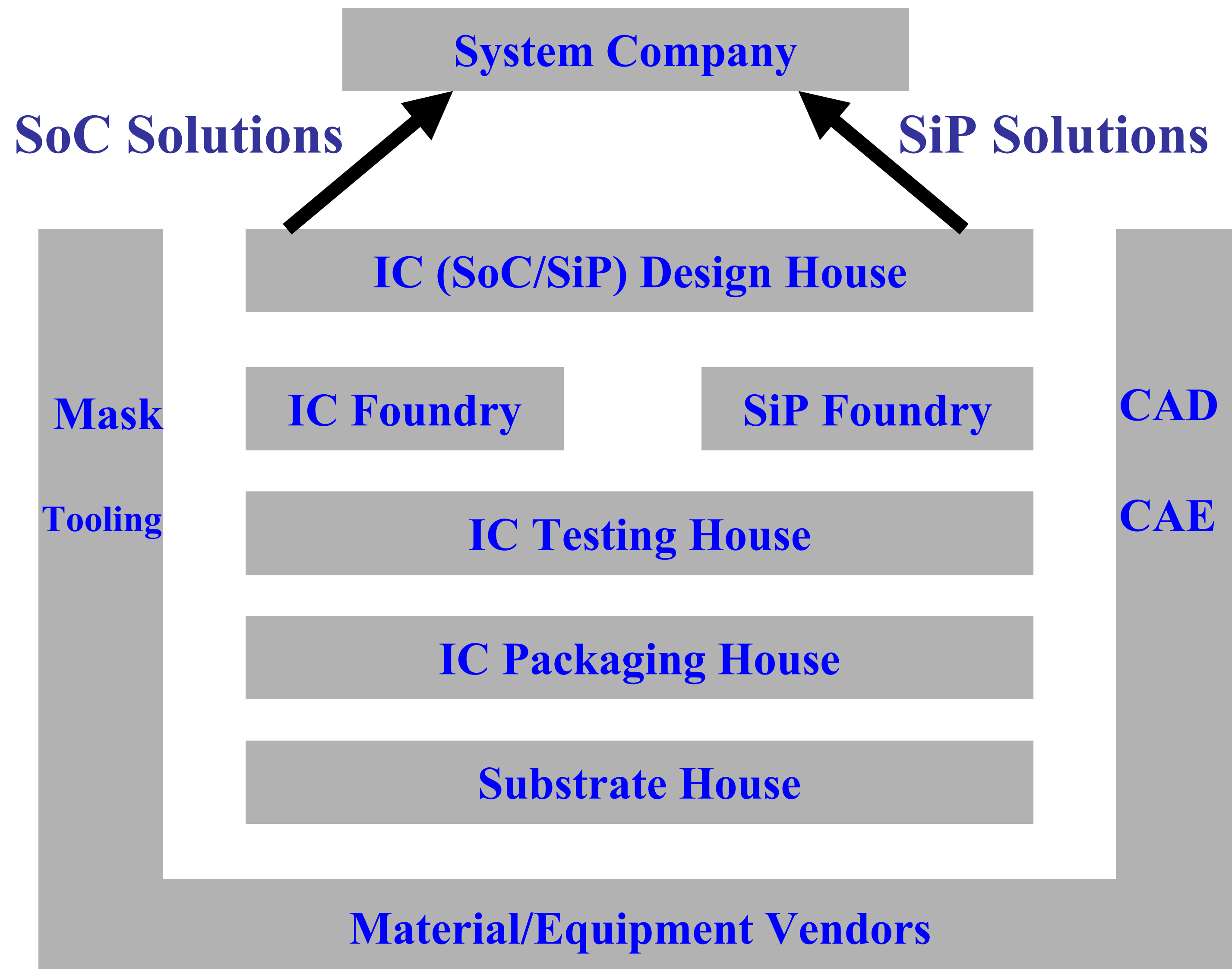
Structure of Inductor

Structure of Capacitor

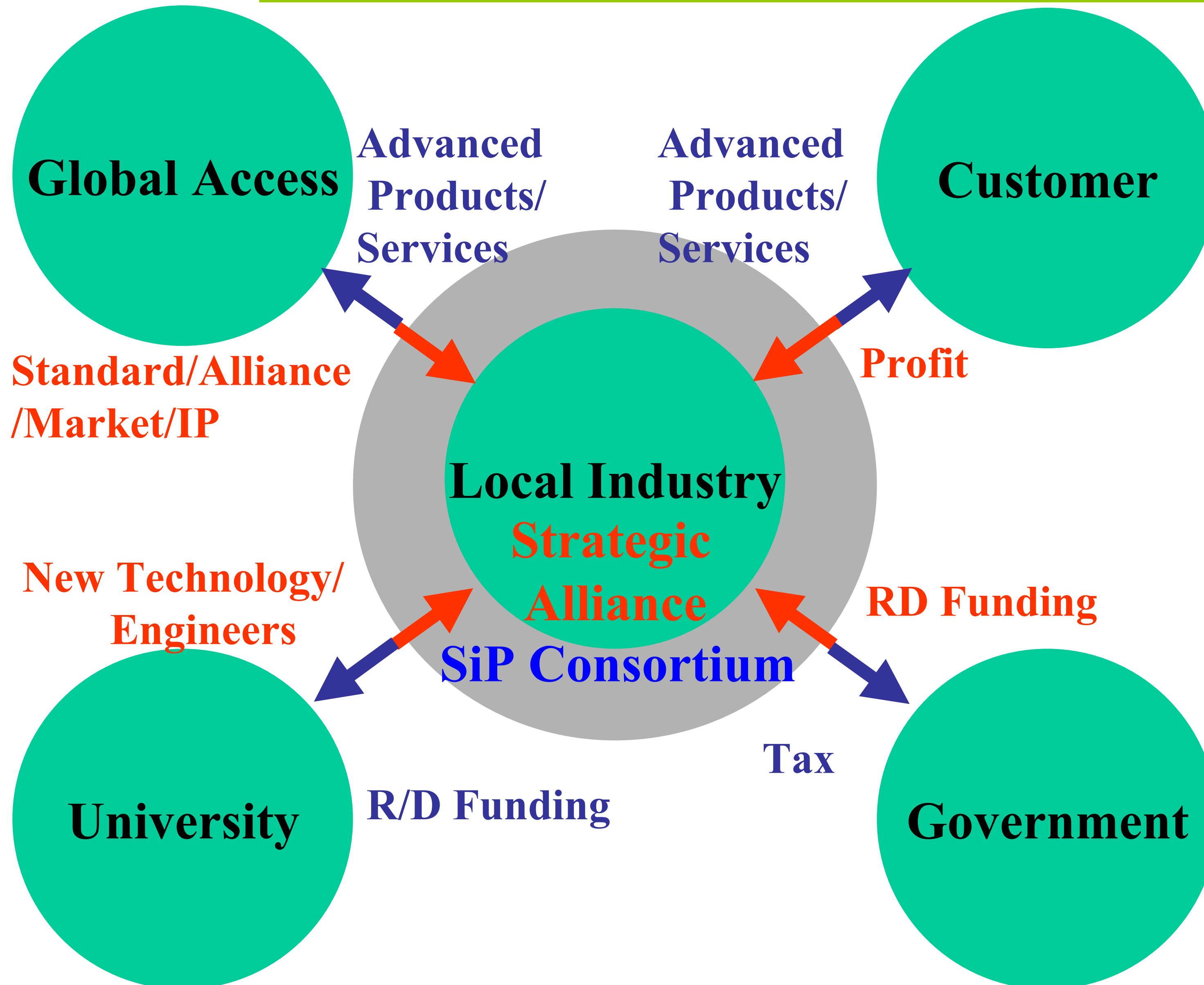
Accomplishment in SiP for RF Applications



Completed Infrastructure of IC Industry



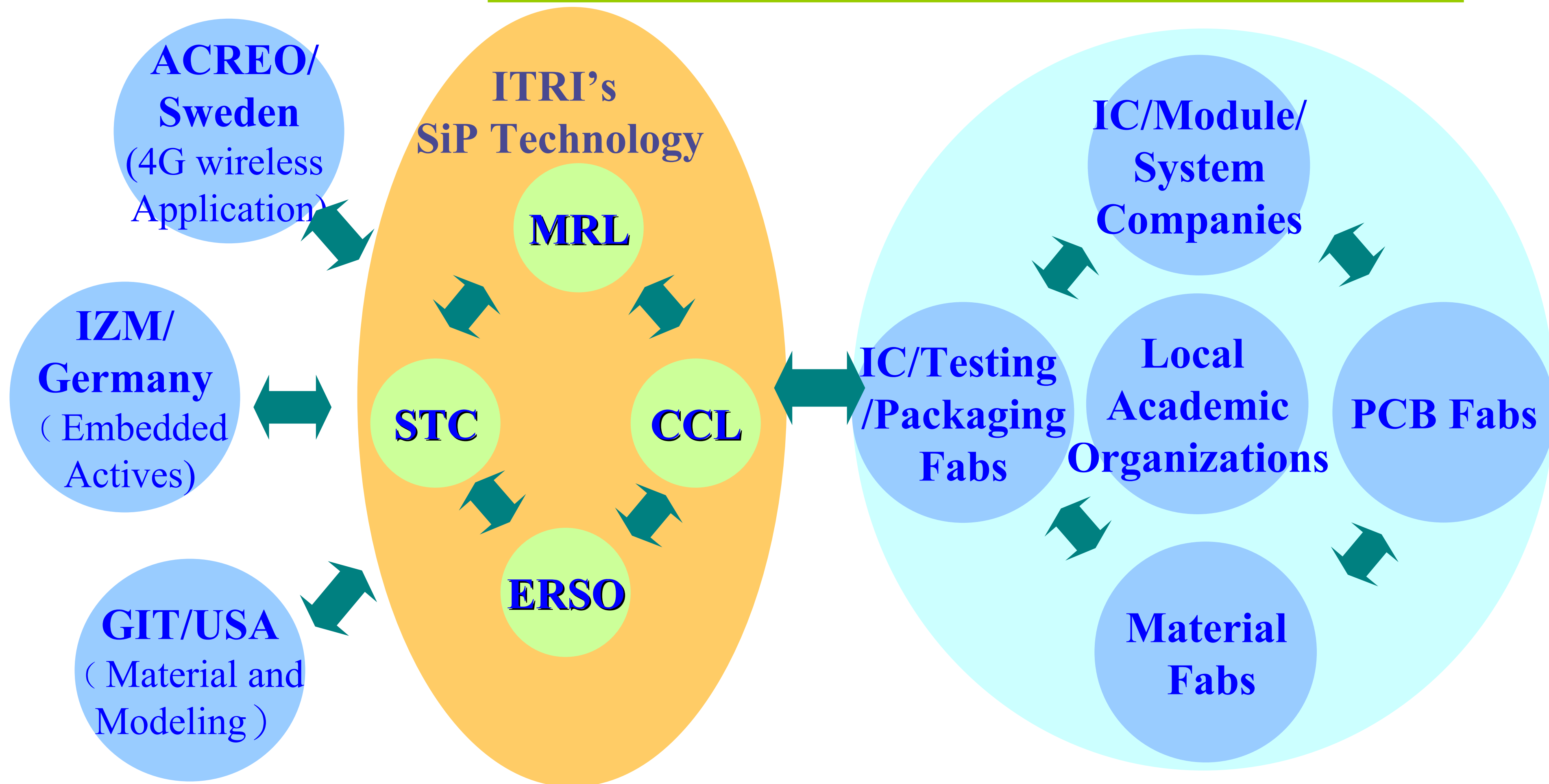
SiP Consortium Working Mechanism



Goals of SiP Consortium

- To provide alternatives to the industry other than SoC solutions
- To back up local industry with core competency
- To mediate industry with better strategic alliance
- To help industry to develop new products & market
- To mediate local industry and MOEA for potential R/D projects
- To bridge local industry to the international opportunities

Strategy



- **Aggressively involve international/local collaboration and maximize technology impact**
- **Upgrade local industry for the next wave competition**
- **Vertically integrate local industry and place Taiwan on top of the SiP Center**

Action Plan

- Push for vertical integration of local industry through strategic SiP alliance.
- Establish SiP working Platform and link with current IC EDA environment.
- Establish proprietary embedded devices BEM and cell library by working with EDA companies and substrate vendors.
- Continue developing higher Dk and lower Df materials as well as key technology for substrate and process to build up entry barrier, especially in nano-technology.
- Extend applications to ESD protection for nano-devices and to de-coupling capacitance for high speed digital system.
- Establish competitive edge through IP mapping, especially on potential area.
- Push for killer applications by working with industrial system and/or module companies through either pure industrial funding or join development funding.

Thank You!