Interconnect Reliability in Conventional and 3D Integrated Circuits

Syed M. Alam, Ph.D.

Freescale Semiconductor

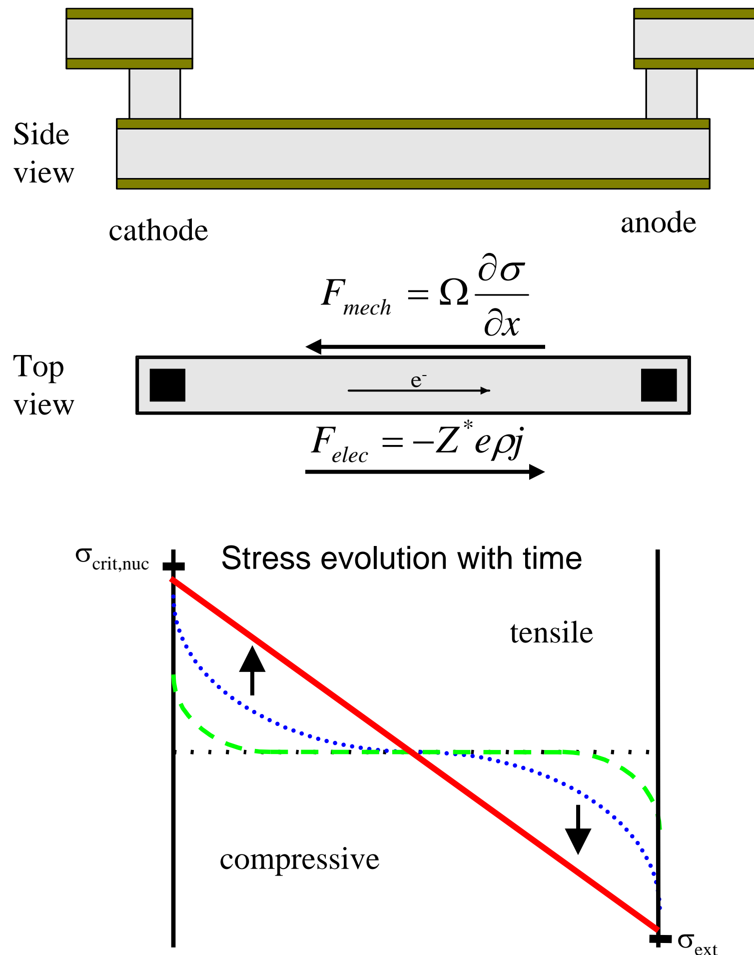
November 17, 2004

Acknowledgements:
MIT Reliability Research: Donald E. Troxel, Carl V. Thompson, Frank L. Wei
Nanyang Technological University: Chee Lip Gan
MARCO Interconnect Focus Center, SRC, Singapore-MIT Alliance

Presentation Outline

- Introduction and Background
  - Electromigration Reliability
- Electromigration Reliability (Cu Metallization)
  - Hierarchical Circuit-level reliability analysis
- Implementation in a CAD Tool
  - Preliminary Circuit Simulation results
  - Thermal-Aware Reliability Analysis
- 3D Integrated Circuits
  - What is 3D IC?
  - Comparative Reliability Analysis
- Conclusion and Future Directions

Electromigration in Interconnects



Electromigration is electron-flow induced diffusion of atoms in a metal line.

According to 1-D Korhonen model,
J_a → atomic flux

$$J_a = -\frac{D\,C_a}{kT}\left(Z^{*} e \rho j - \Omega \frac{\partial \sigma}{\partial x}\right)$$

Diffusivity

Concentration

Electron charge

Stress gradient

Boltzmann's constant

Temperature

Charge number

Resistivity

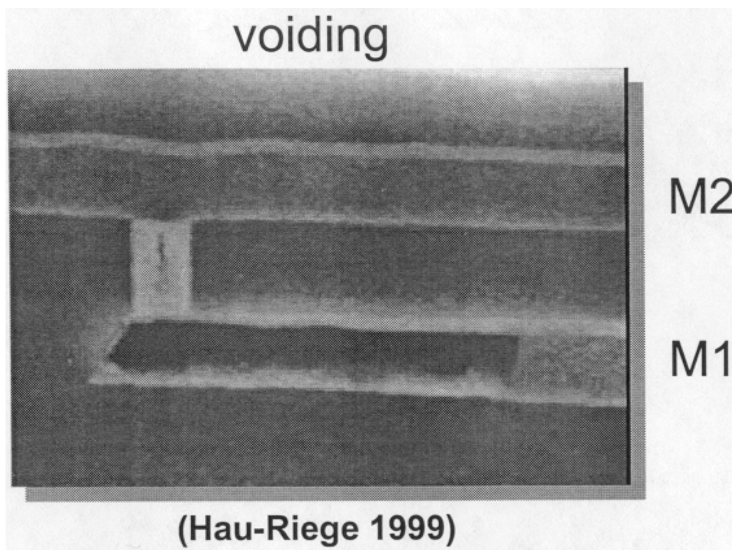
Current density

Atomic volume

M.A. Korhonen *et al.*, JAP, **73**, 3790 (1993)

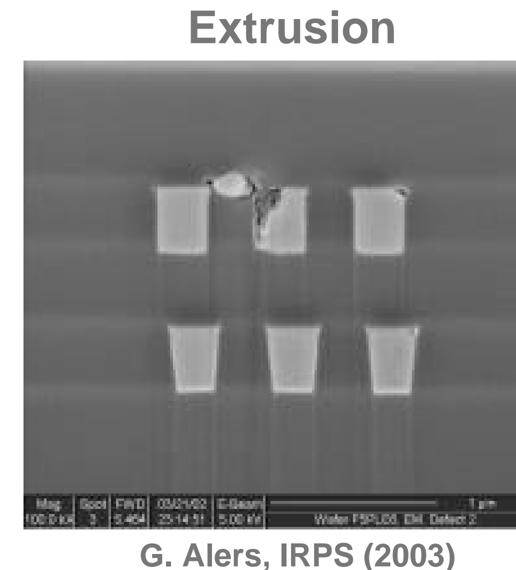
Electromigration-induced Failures

Tensile stress at cathode end can cause voiding



(Hau-Riege 1999)

Compressive stress at anode end can cause extrusion

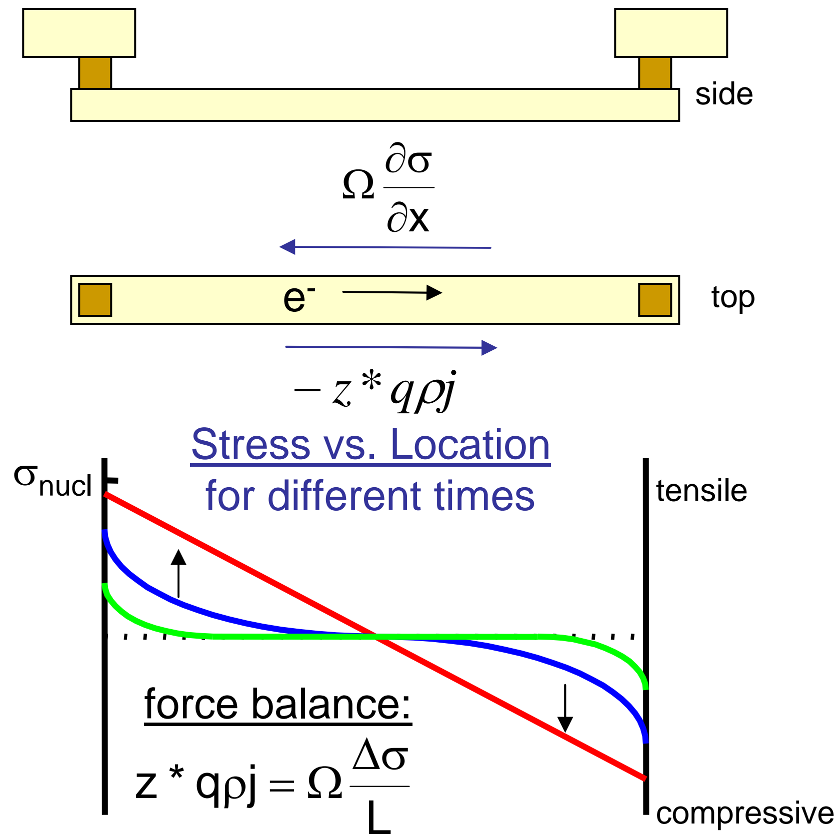


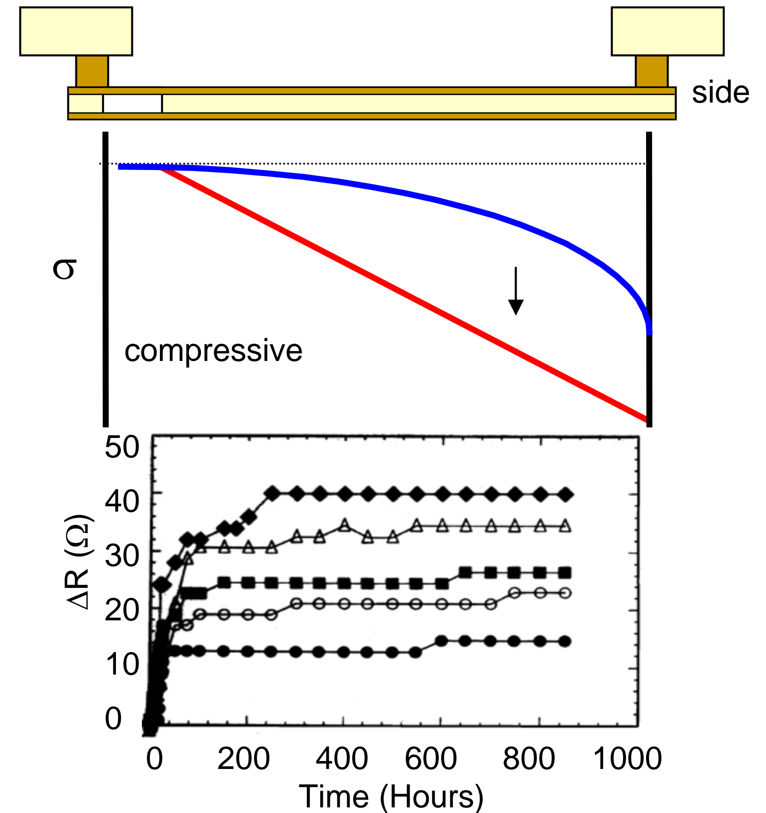
G. Alers, IRPS (2003)

- Extrusion is *not* the primary failure mode during service condition as well as most accelerated testing ($j<5MA/cm^2$) for both Cu and Al

- Voiding can lead to resistance increase or open circuit failure in both Cu and Al interconnects.

Two *Different* Mechanisms for EM Immortality





(R.G. Filippi et.al., *Appl. Phys. Lett.* **69** (1996) 2350.)

Immortal when:

$$(jL)_{nuc} < \left(\frac{\Omega \Delta\sigma_{crit}}{z^* e\rho} \right)$$

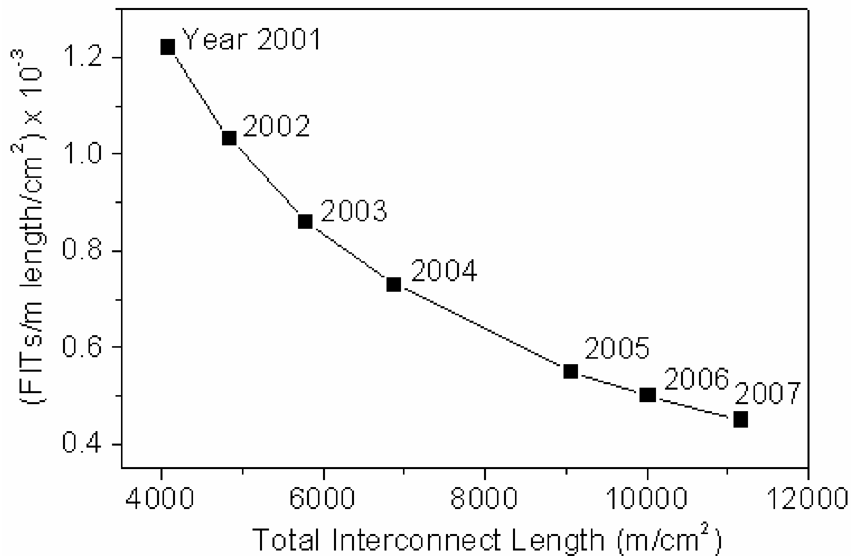
(Blech)

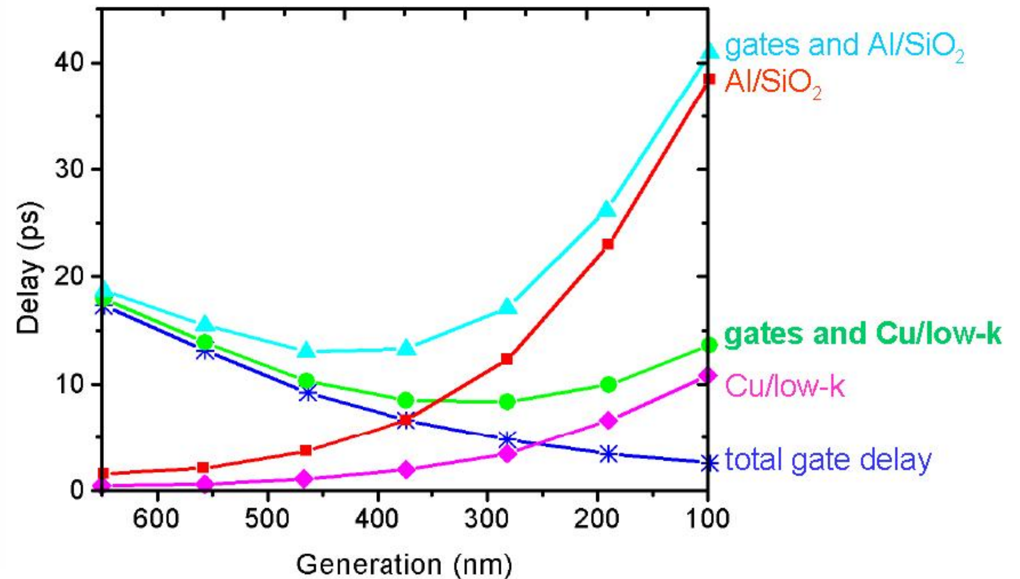
Immortal when:

$$(jL)_{sat} < \frac{\rho / A}{\rho_1 / A_1} \frac{\Delta R_{fail}}{R} \frac{2\Omega B}{e\rho z^*}$$

(Korhonen, Suo, Andleigh)

Motivation for Electromigration Reliability Analysis





Interconnect reliability requirement is increasing exponentially.

Cu must replace Al as the metal of choice to meet performance goals.

[ITRS, 2001]

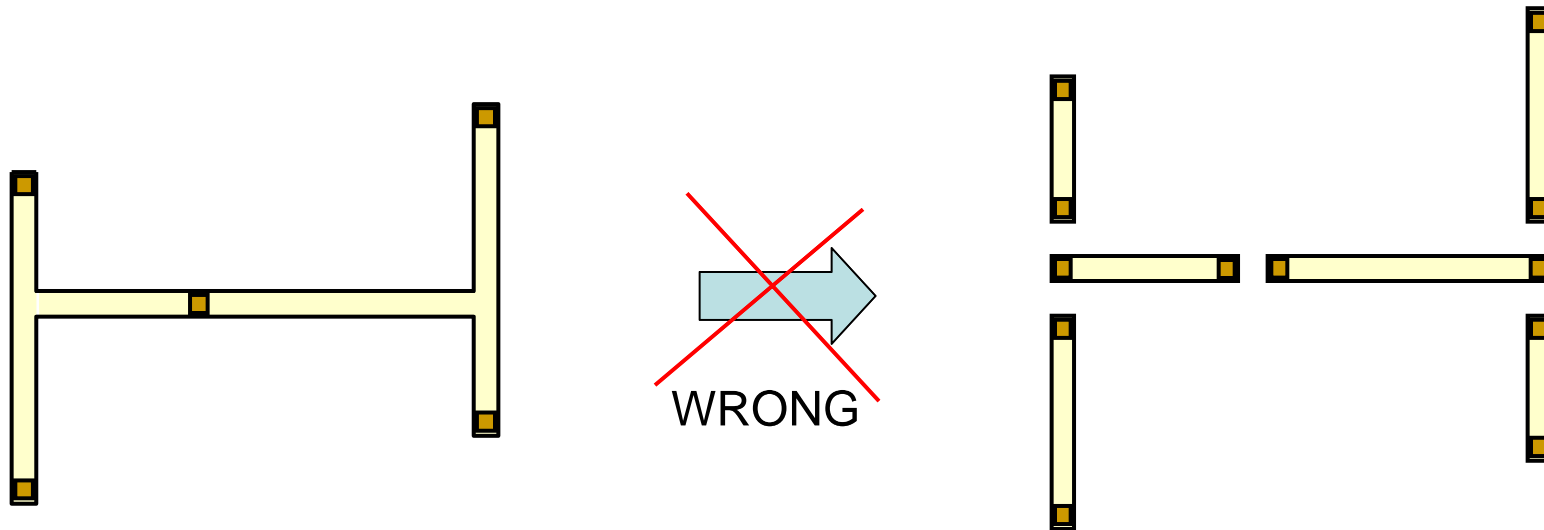
According to SEMATECH Technology Transfer report (2003), "Cu via and line Electromigration" under "Cu/low k interconnects" is among "most critical roadmap challenges from a reliability prospective."

Widely Used Approaches for Interconnect Reliability Analysis

Approaches in academic tools (e.g. BERT, iTEM) and commercial tool (e.g. Nanosim / RailMill):

- Often j-based immortality checks only
- Break up trees into segments
- Assess reliability of each segment using Black's equation

$$MTTF = Aj^{-n}e^{\left(\frac{Ea}{kT}\right)}$$



A common approach in circuit design:

- Limit electromigration critical current density in lines and vias

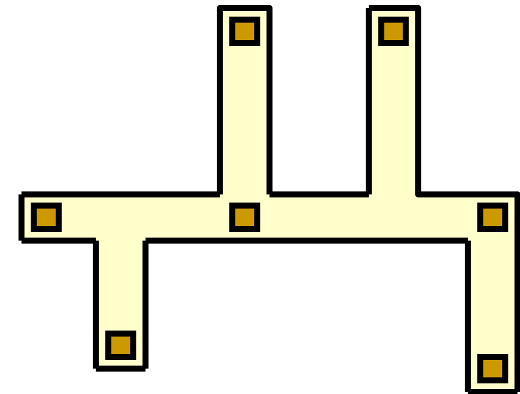
Need for Better Approach in DSM Design

Flaw with segment-based reliability analysis:

- Segments are not independent. Current densities of different segments impact reliability at a via.

It has been shown that Interconnect tree is the Fundamental Reliability Unit for Al electromigration (S. Hau-Riege et al.)

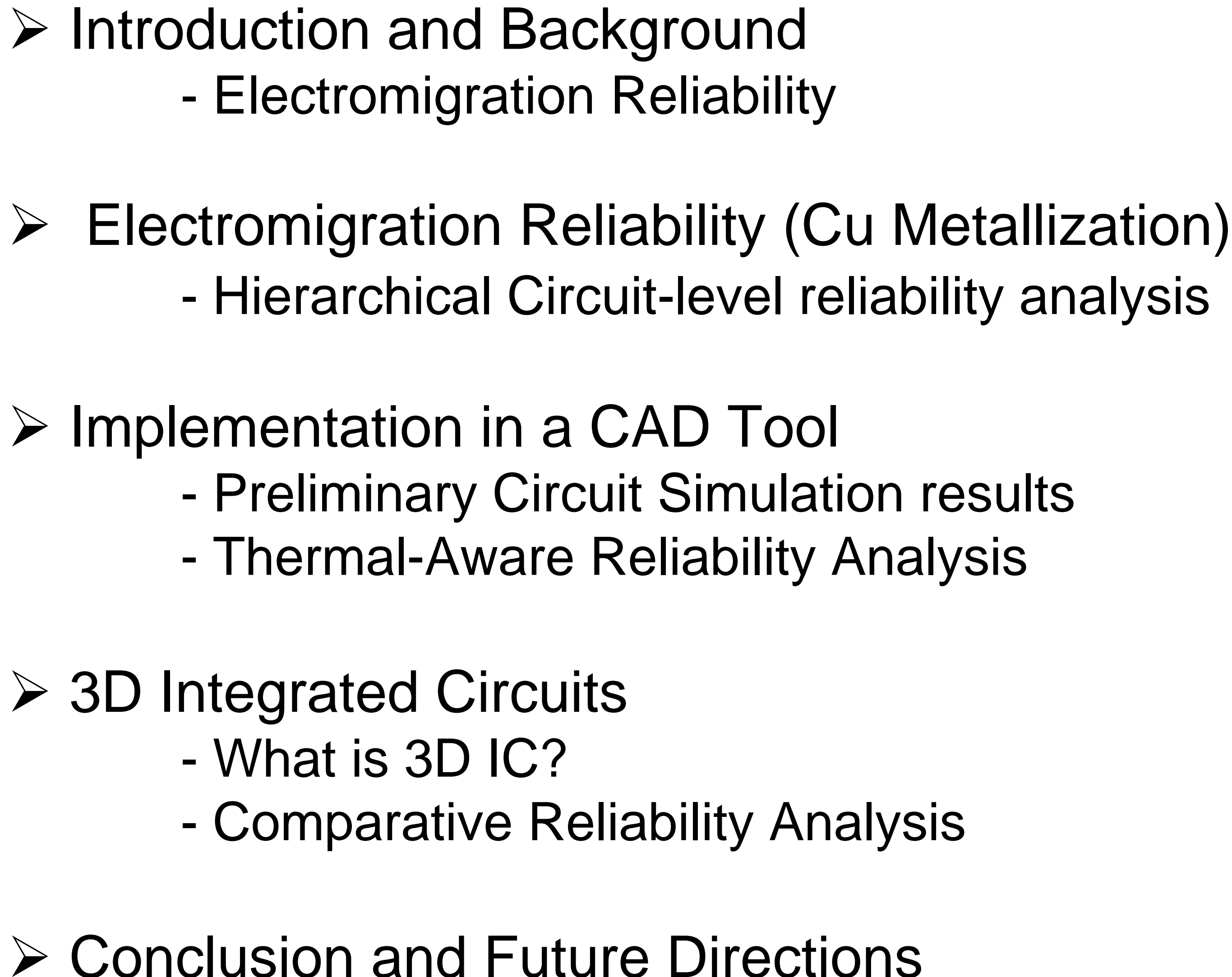
Interconnect Tree:
Continuously connected conductor metal within one layer of metallization terminating at vias (diffusion barriers)



Flaw with current-density, *j*, limited conservative design :

- Leads to wider interconnect layout for lower *j*. Moreover, not all the trees are prone to electromigration failure.

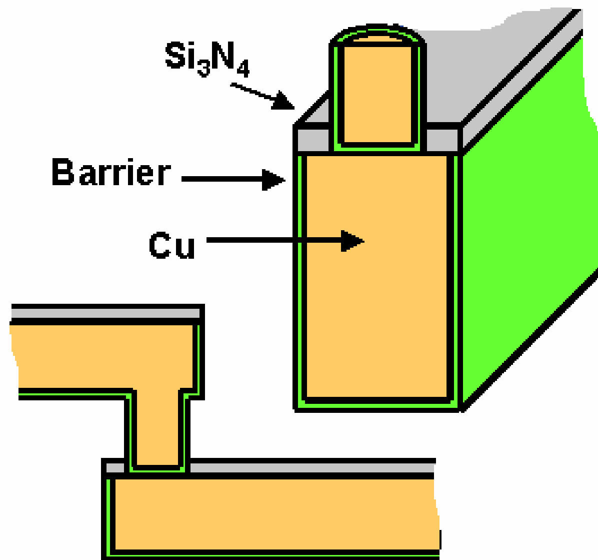
Presentation Outline



Interconnect Technology: Cu

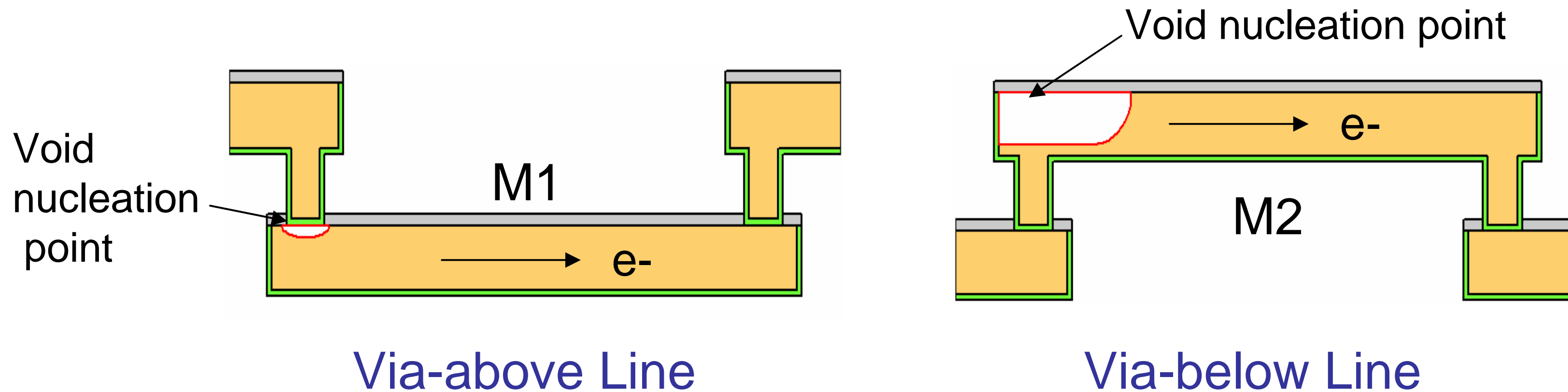
Two main causes for differences in reliability in Al and Cu:

- Interconnect architecture scheme
- Diffusion pathways



- Non-conducting tantalum-based liner as Interlayer dielectric (ILD) barrier on three sides
- Poor bonding to Si_3N_4 on top
- Thin liner acts as diffusion barrier at a via most of the time
- Dominant atomic diffusion pathway is Cu/ Si_3N_4 interface.

Via-above and Via-below Classification in Cu Technology



Via-above Line

Via-below Line

• Cu/Si_3N_4 interface provides lowest threshold for void nucleation and the fastest diffusion path

• Void volume required for failure is larger for M2 than that in M1

• t_{50} of M2 > t_{50} of M1 Gan *et al., APL* **79**, 4592 (2001)

• This phenomenon is not limited to M1 and M2 structures. Therefore, generalization is required through the classification of via-above and via-below lines.

Immortality Condition Filter: Cu

Cu Technology
(Two immortality thresholds)

$(jL)_{sat}$ or via-below filter:

[6, 7] Ho *et al.*, *APL* 79 & 78, 2001

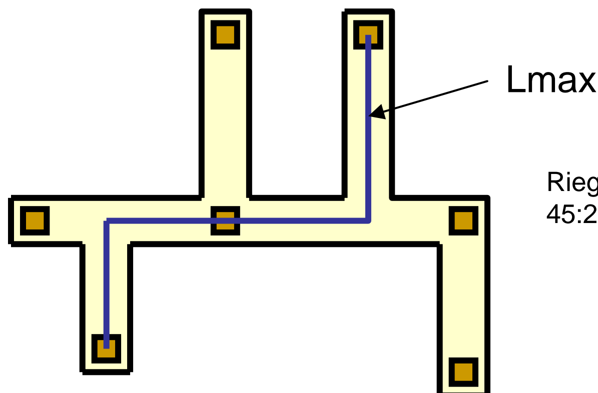
$$(jL)_{sat} = 3700 \text{ A/cm}$$

$(jL)_{nucl}$ or via-above filter:

[8] Hau-Riege *et al.* AMC, 2002

$$(jL)_{nuc} = 1500 \text{ A/cm}$$

Calculating $(jL)_{eff}$ of an interconnect tree:



Riege *et al*. TED, 45:2254, 1998

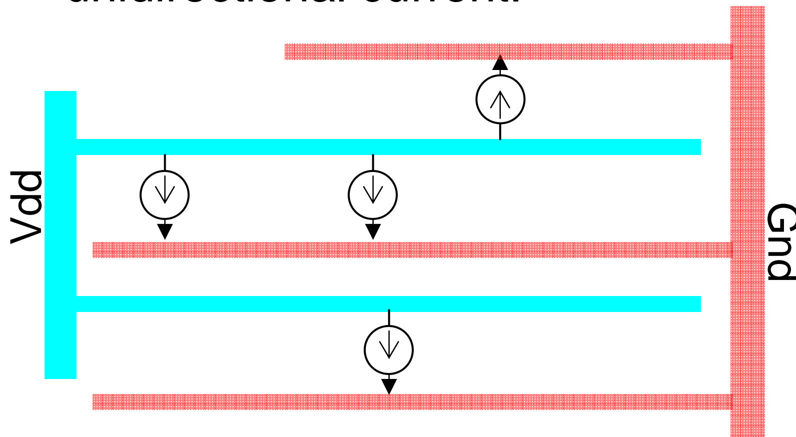
Each segment along an end-to-end via path is denoted as i.

$$(jL)_{eff} \equiv \left(\sum_i j_i L_i \right)_{\max}$$

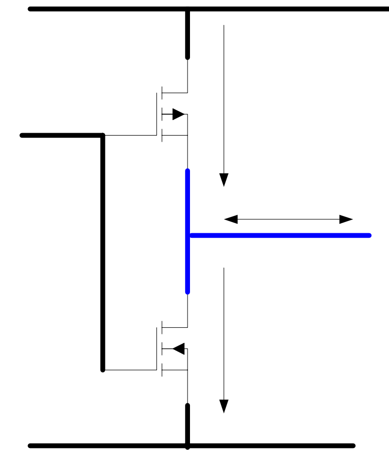
Segment-based current calculation can be computationally expensive, then use j_{max} and L_{max} of the tree.

Current Density in Interconnect Lines

Vdd and Gnd lines carry unidirectional current.



Signal lines usually carry bi-directional current



Current estimation types:

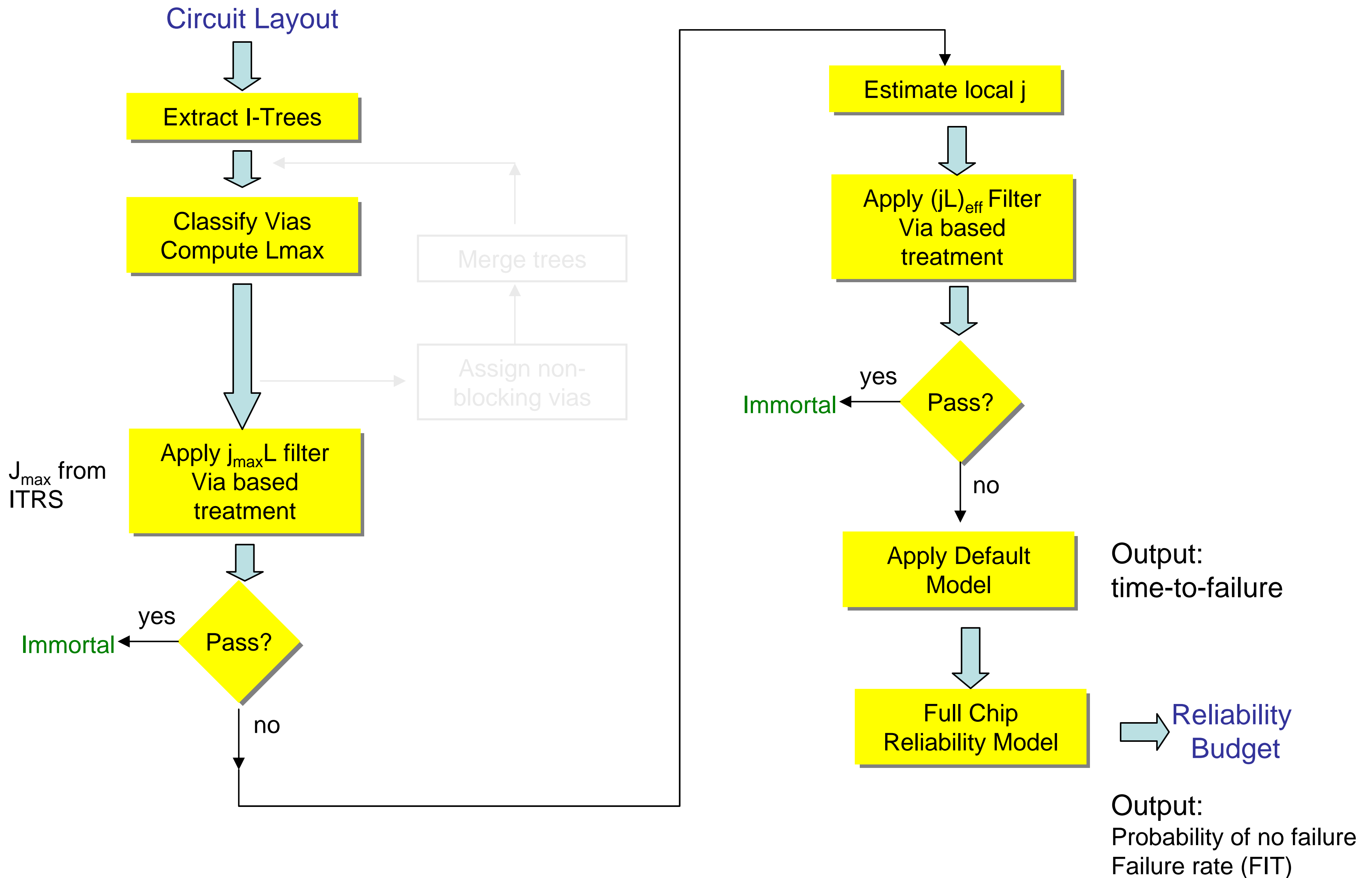
Electromigration J_{avg}

Joule Heating J_{rms} & J_{peak}

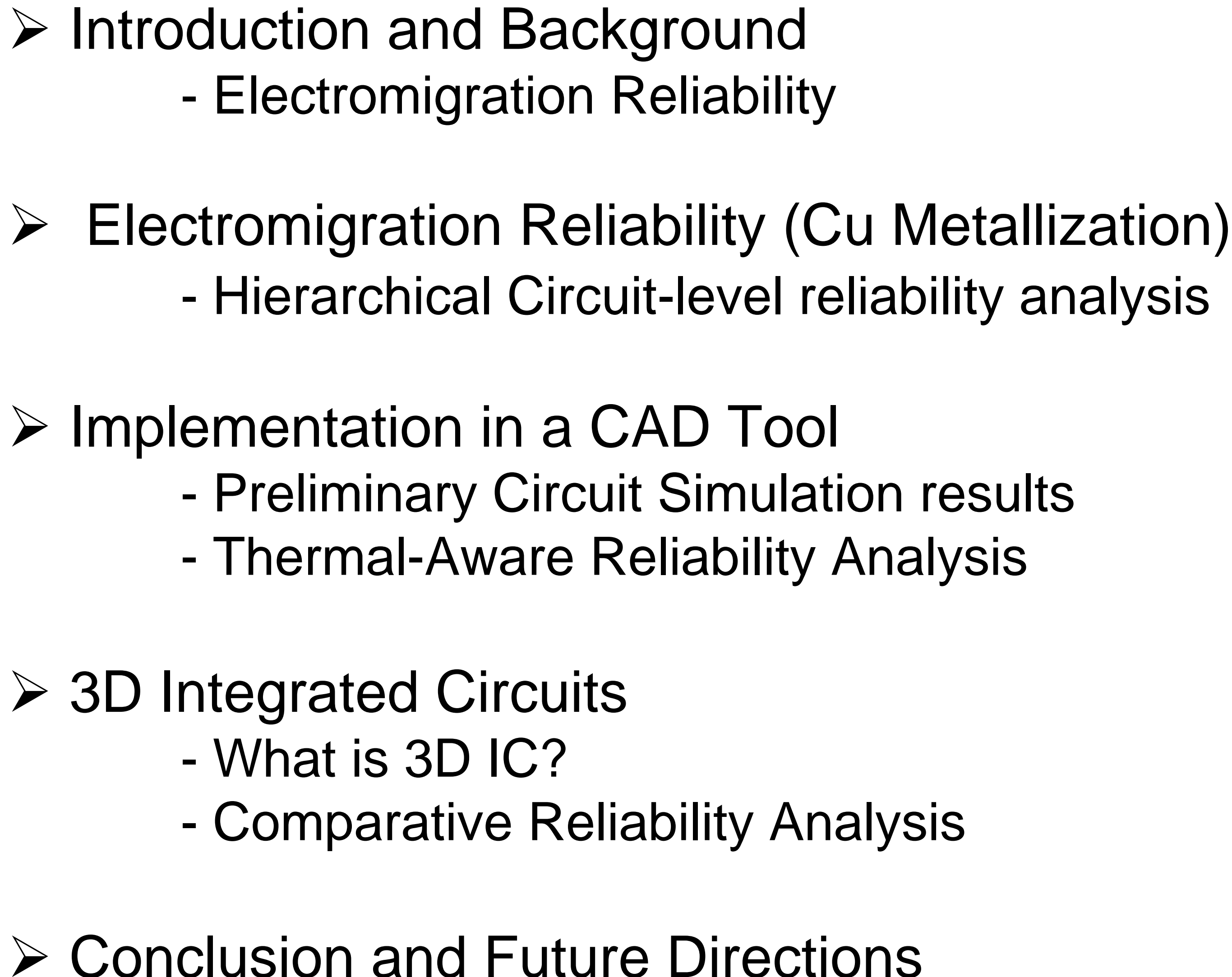
D. Blaauw *et al.,* TCAD ICS, vol. 20 p39, 2003
J. J. Clement *et al.,* TCAD ICS, vol. 18, p576, 1999

Bi-directional current is assumed to have healing effect in electromigration.
Experimental characterization is required (for Cu) to quantify the impact.

Flow Diagram for Cu Reliability Analysis



Presentation Outline



- Introduction and Background
  - Electromigration Reliability
- Electromigration Reliability (Cu Metallization)
  - Hierarchical Circuit-level reliability analysis
- Implementation in a CAD Tool
  - Preliminary Circuit Simulation results
  - Thermal-Aware Reliability Analysis
- 3D Integrated Circuits
  - What is 3D IC?
  - Comparative Reliability Analysis
- Conclusion and Future Directions

SysRel: Interactive Reliability CAD Tool

http://www-mtl.mit.edu/research/reliability

Circuit-Level Reliability

Written in Java 2 (portable program).

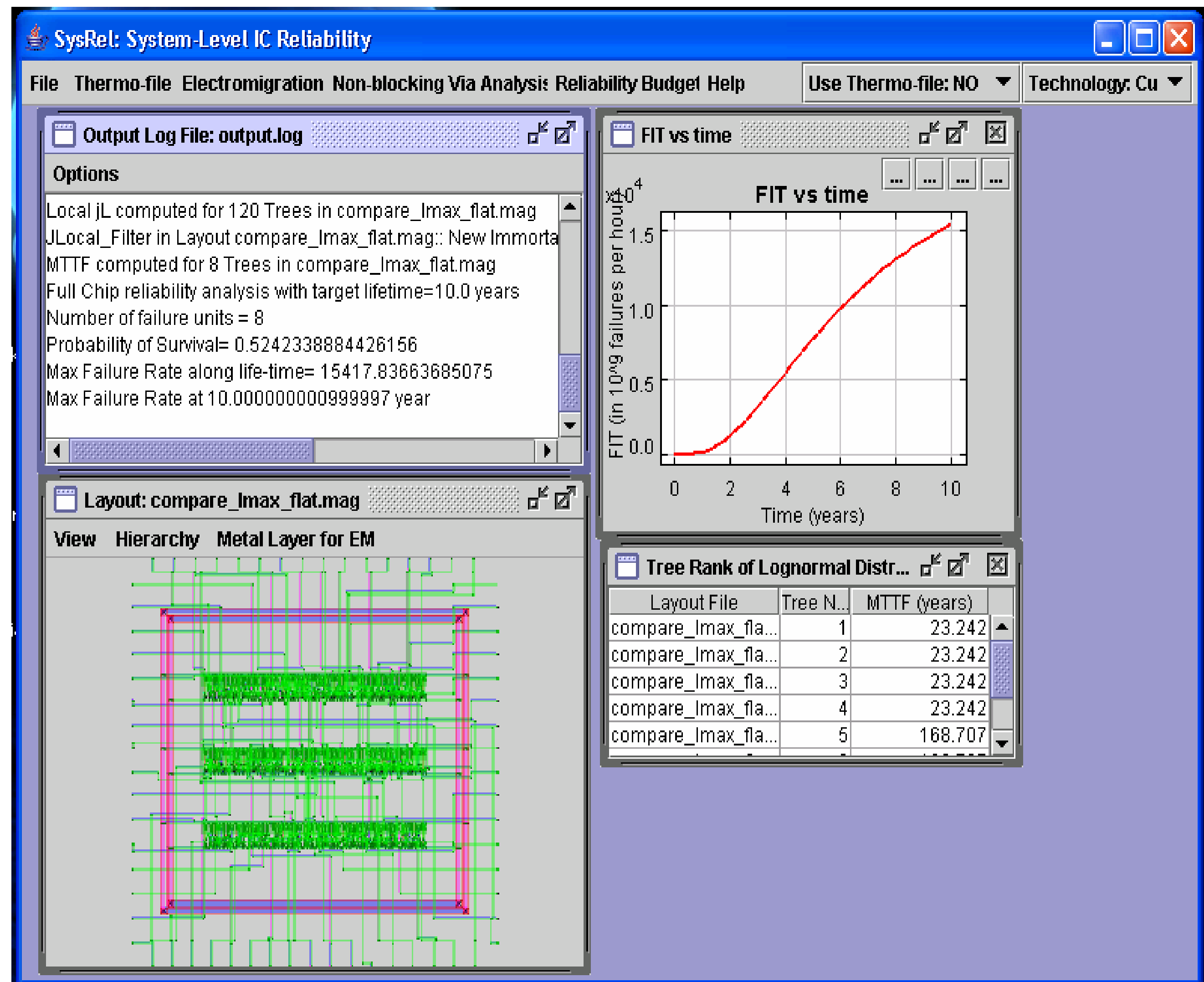
Consists of 31 java files. Approx. 9k lines of code.

Analyzes Layouts from Magic or 3D-Magic*.

Public domain CAD tool. Release 2.0 is available at the listed website.

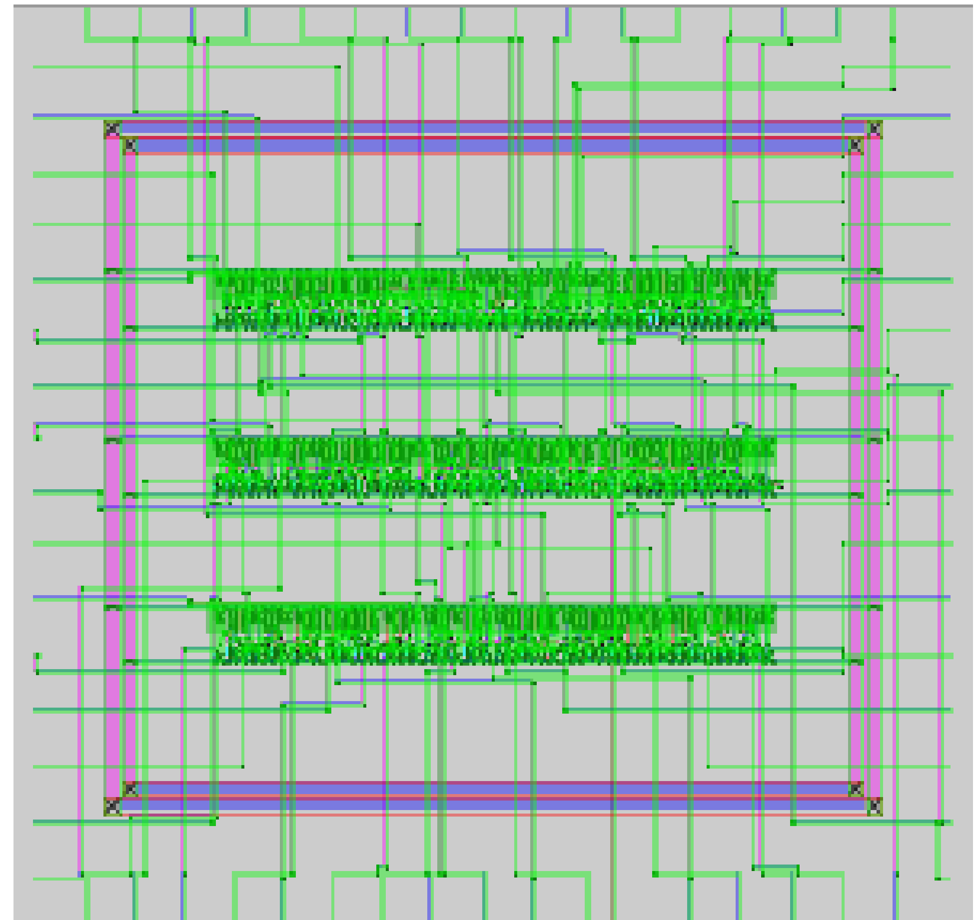
*Also developed by S. M. Alam

S. M. Alam et al., ISQED, 2004



Test Circuit: 32-bit Unsigned Comparator

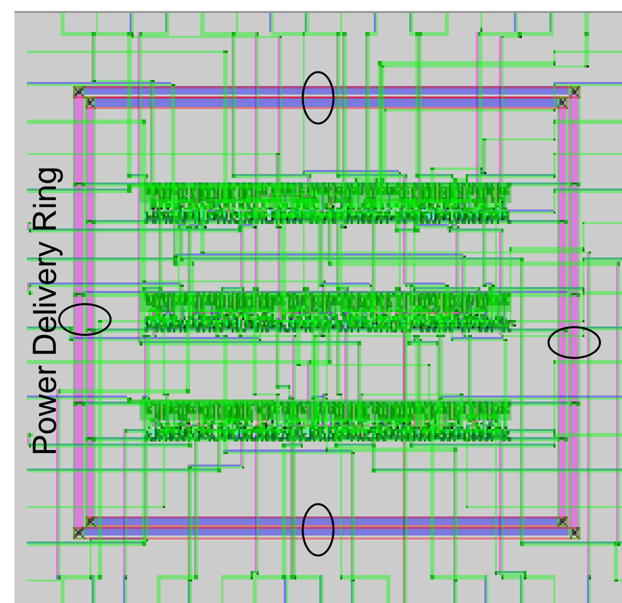
- Design flow using VHDL to synthesis with Design Analyzer and Silicon Ensemble using IIT TSMC 0.18um Cell Library
- Number of Cells: 118
- Up to metal 5 for routing
- Layout Dimension: ~160um x 160um
- Power dissipation from Design Analyzer, P=26.6mW with Vdd=5 V
- Netlist extracted from layout and simulated for functional verification



32-bit Comparator Layout: Cu Technology

Step 1	Layout Extraction (total # of interconnect trees=1143)	
	Metal Plane	# of Interconnect Trees
	1	580
	2	438
	3	102
	4	20
	5	3
Step 2	Via-based ($j_{max}L$) filter	
	Number of immortal trees identified	1023
Step 3	Via-based ($j_{local}L$) filter	
	Number of immortal trees identified	112
Step 4	Default Model (with σ_{nucl} = 40MPa) on 8 mortal trees	
	MTTF of 4 mortal tees in Metal 1 (via-above)	23.2 years
	MTTF of 4 mortal trees in Metal2 (via-below)	168.7 years
Step 5	Full chip stochastic analysis (σ=0.81, lognormal) T=105ºC	
	Target chip lifetime	10 years
	Probability of no failure	0.524
	Max FIT	15.4k @ 10th year
	t_{50} for full chip	10.35 years

- Mortal power lines are marked below



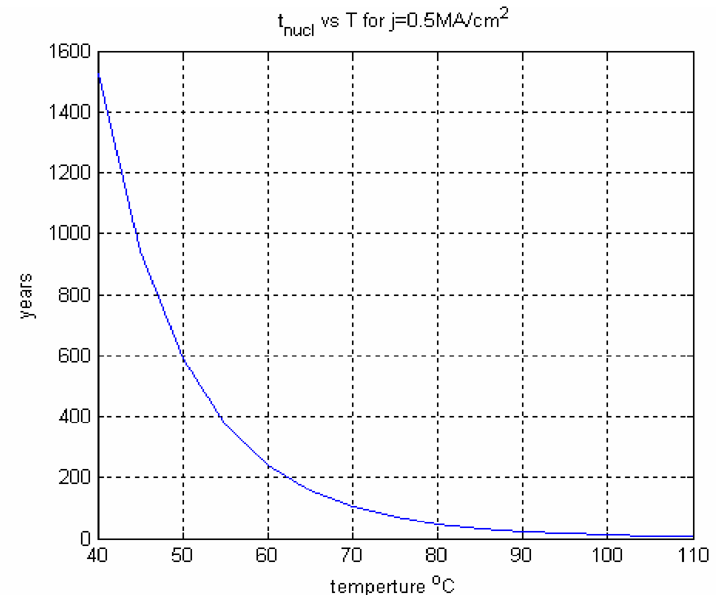
- Increasing the worst mortal line widths by 2, increases t_{50} of each unit from 23.2 years to 92.9 years. Resulting full-chip t_{50}=37.5years, FIT 563, prob. of survival 0.9872

SysRel identifies electromigration critical nets and their impact on full-chip reliability

Thermal-Aware Capabilities in SysRel

⇒ Electromigration Lifetime is *exponentially* dependent on Temperature.

⇒ Need thermal-aware reliability simulation.



⇒ Cell-based thermal analysis approach used in SysRel:

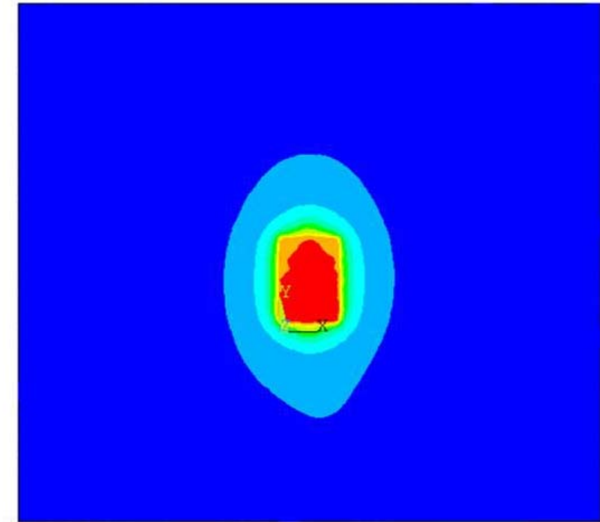
- Derive cell power dissipations from Design Analyzer or Nanosim simulation
- Compute power density matrix in SysRel using cell powers

⇒ IC thermal simulation using ANSYS (FEM tool) to investigate the power density to temperature relation

Thermal Simulation of FETs with ANSYS

- SOI nFET with diffusion contacts and metal lines
- Self-heating: max $\Delta T = 53^{o}C$
- Reported R_{th}= 50-90 $^{o}C/mW/um$

L. Su *et al*. TED, vol. 41, p69, 1994

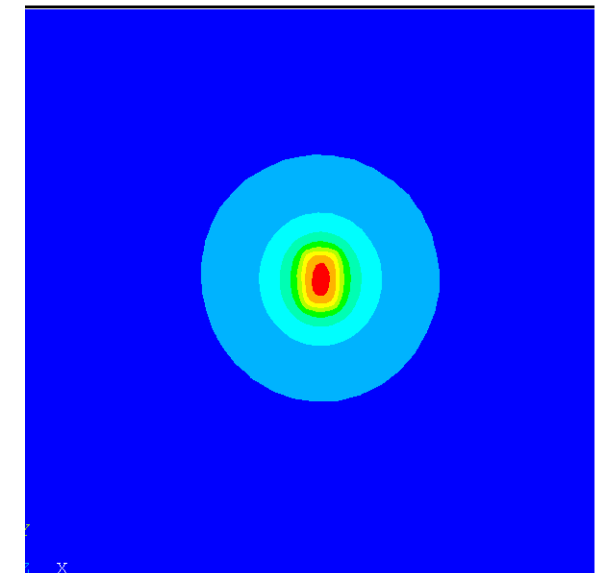


Temperature profile on top surface of substrate (SOI)

- Bulk nFET with diffusion contacts and metal lines
- Self-heating: max $\Delta T = 17.3^{o}C$
- Reported R_{th}=4-6 $^{o}C/mW/um$

M. B. Kleiner *et al*. IEDM p487, 1995

Observation: T distribution in bulk CMOS is axisymmetric with respect to the source.

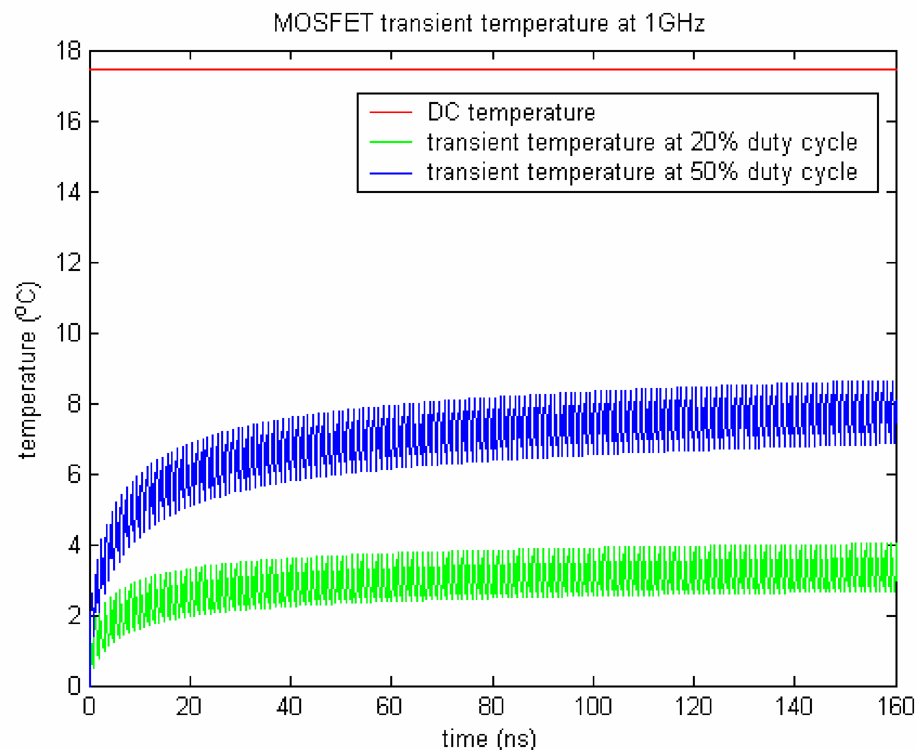


Temperature profile on top surface of substrate (Bulk)

Transient Thermal Modeling in ICs

⇒ Transient thermal simulation represents actual circuit operation. Maximum temperature rise in a device is a strong function of device operation over time.

⇒ Transient thermal behavior can be understood with respect to τ, thermal time constant. From ANSYS simulation τ=17.55ns for a bulk device, and from IBM paper (K. Jenkins *et al*., SOI Conf. p161, 2003) τ=50-90ns for SOI devices.



Modeling Transient behavior of bulk CMOS

At 1 GHz operating frequency (τ=40xPW)

Transient temperature at 50% duty cycle reaches a steady-state value of

$T_{avg} = 8 \pm 0.89$ °C

Using DC to transient approximation using:

$T_{avg} = T_{DC}/2 = 8.73$ °C (50% duty cycle)

(ratio of DC and avg. power)

Transient temperature at 20% duty cycle reaches a steady-state value of

$T_{avg} = 3.35 \pm 0.68$ °C

Using DC to transient approximation using:

$T_{avg} = T_{DC}/5 = 3.49$ °C (20% duty cycle)

(ratio of DC and avg. power)

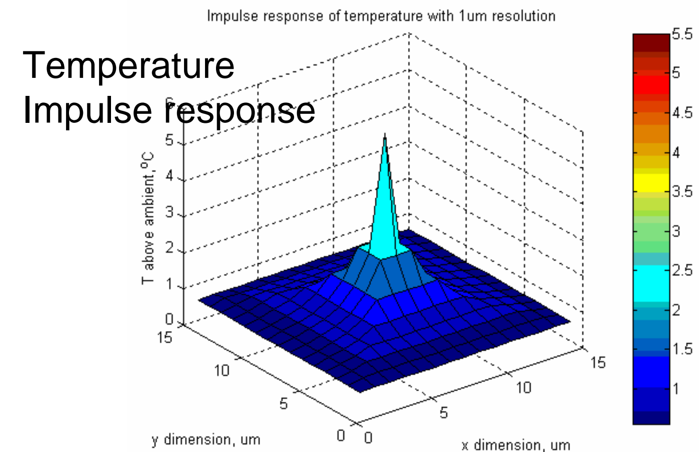
Temperature Profiling Method in a Layout

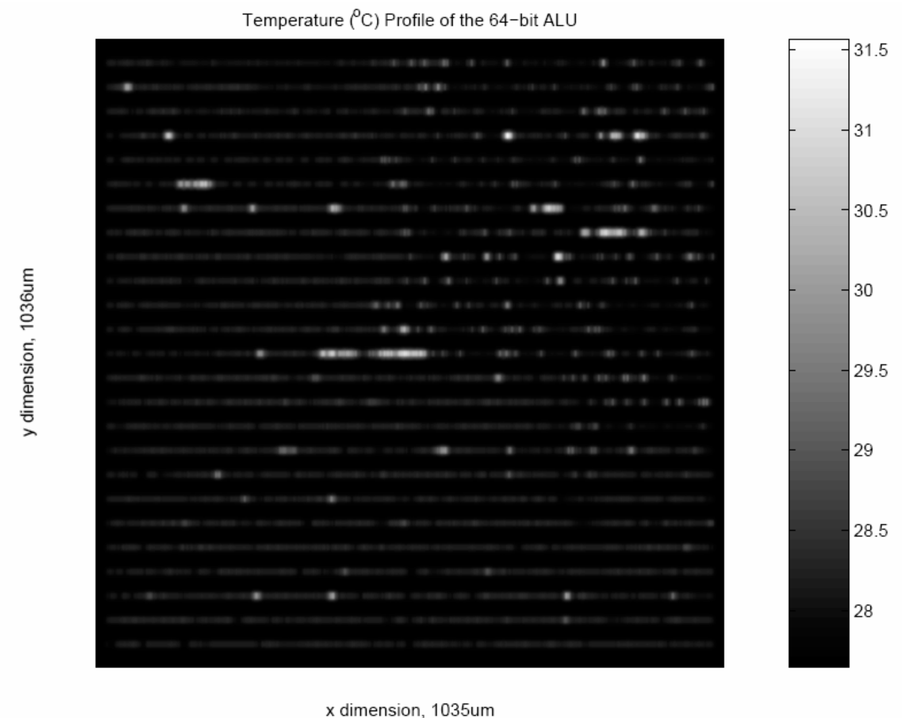
⇒ We obtain a temperature impulse response from FEM analysis (using ANSYS) for 1mW power in 1um x 1um area.

⇒ We assume temperature at the top of the substrate is a *linear spatial independent* variable (very accurate for bulk CMOS technology).

⇒ For the power density profile in a layout computed by SysRel, we compute (using a Matlab script) non-uniform temperature profile using convolution with the impulse response.

⇒ Frequency domain computation with FFT is used for computational efficiency.





SysRel Thermo-file Menu Operation

SysRel: System-Level IC Reliability

File | Thermo-file | Electromigration | Non-blocking Via Analysis | Reliability Budget | Help

- Read Hierarchical Magic file...
- Read Power Distribution (.cpower) File...
- Write Power Density Matrix (currentpden.m) file
- Read Temperature Profile Matrix (tprofile.dat) file..

MOSIS Scalable CMOS Technology for 3D IC desig
Loading Magic file 'file:/Z:/DESIGNS/32bitComp_tsr
11812 tiles added... done
LayoutPanel: hierlevel=1
Layout file compare_lmax_flat.mag opened
Loading Magic Hierarchical file 'file:/Z:/DESIGNS/32
Hierarchical Layout file compare.mag opened for th
EM parameters read from: file:/Z:/sysrel.emparam

Layout: compare_lmax_flat.mag

View | Hierarchy | Metal Layer for EM

Read cell-based power dissipation file from Design Analyzer simulation or Nanosim simulation.

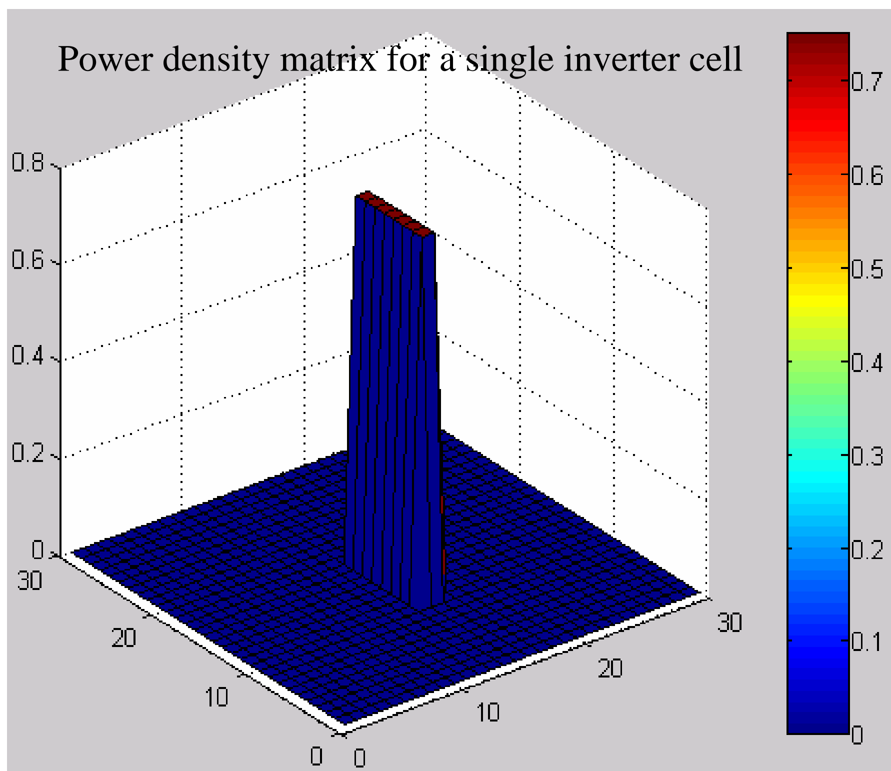
Write power density matrix (1umx1um resolution) in a file for matlab. Distribute Power evenly in a cell.

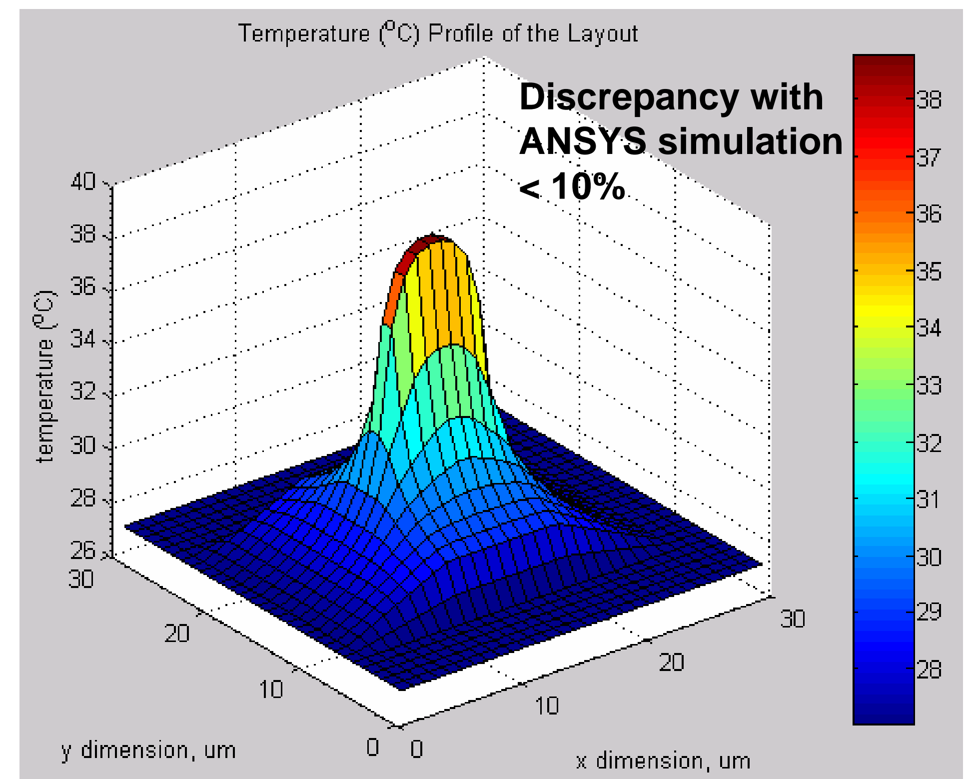
Read temperature profile matrix file produced by Matlab.

TProfile: Matlab Program for Thermal Analysis Using the Impulse Method

- Inputs: temperature impulse response in an array, power density matrix from SysRel
- Outputs: Temperature profile matrix for SysRel input

  Plots the impulse response and temperature profile matrix





Synthesis and Layout of 64-bit ALU

Arithmetic and Logic Unit

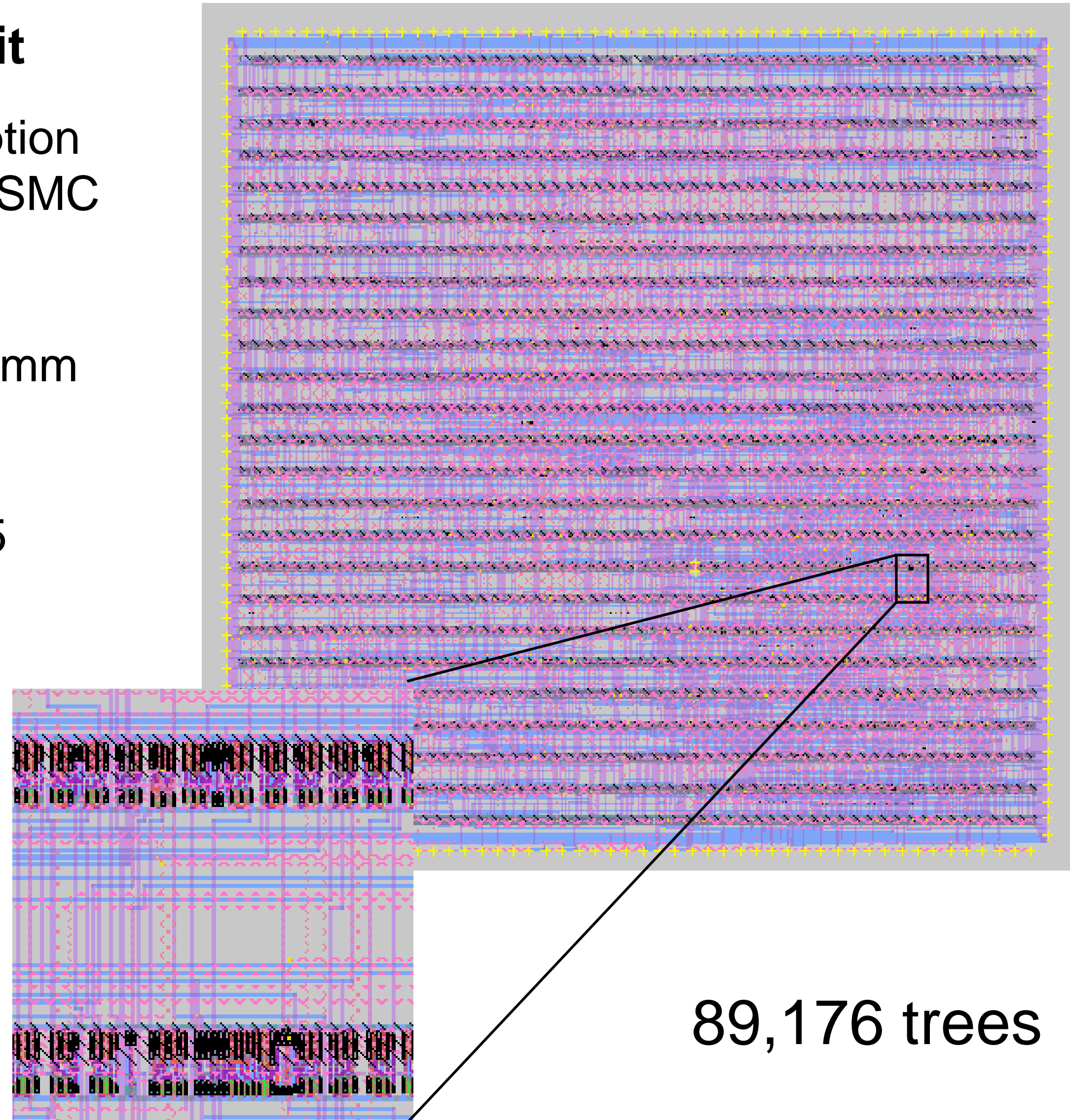
⇒ Synthesized from VHDL description to Verilog gate level netlist using TSMC 0.18um library.

⇒ Layout size: 1.035 mm X 1.036 mm Up to metal 5 for routing.

⇒ Number of cells: 4193. Using 25 rows for cell layout.

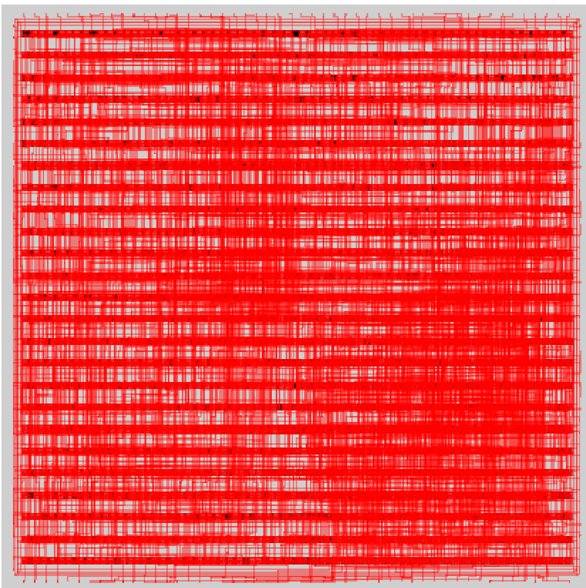
⇒ Power dissipation = 2.129 Watt reported in Design Analyzer with Vdd=5V

⇒ Converted from gds2 output of Silicon Ensemble to Magic format.

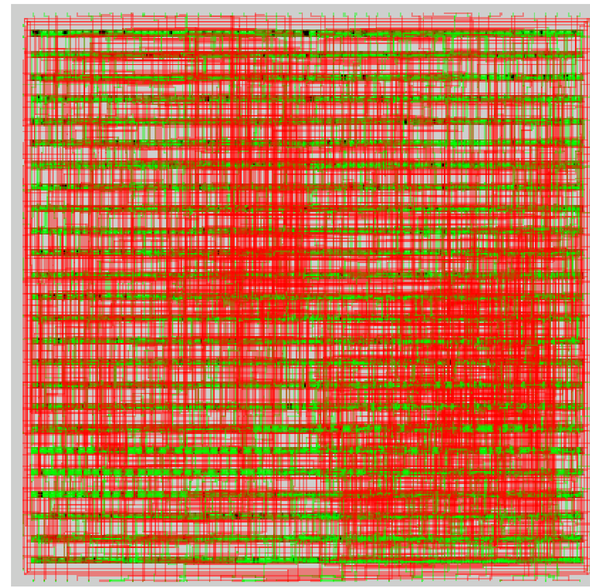


SysRel Simulation with 64-bit ALU Circuit

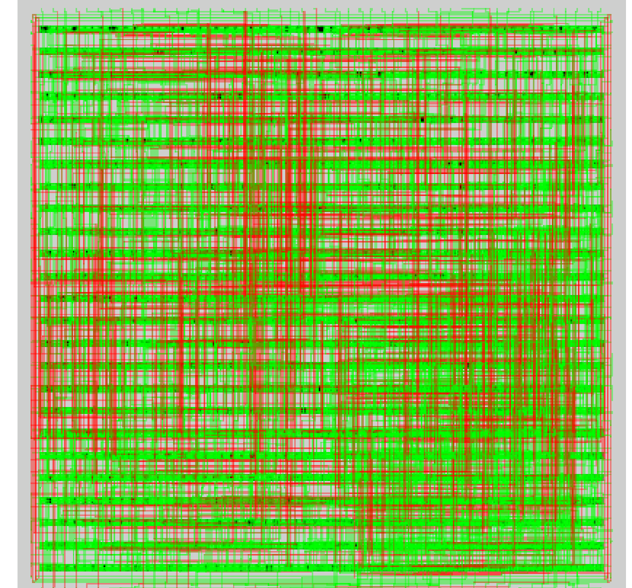
⇒ Cell-based Layout loaded into SysRel for simulation
⇒ Full chip (including cell internal trees) analysis with **Cu technology**



1. 89176 trees after extraction



2. (jmaxL) filter immortal trees =81619



3. (jlocalL) filter, new immortal trees =6415
Final mortal trees=1142

Cu/SiO_2 **:** $(jL)_{M2}$ = 3700 A/cm > $(jL)_{M1}$ = 1500A/cm

98.7% trees are immortal

Thermal-Aware SysRel Simulation

64-bit ALU circuit with Cu/SiO_2 based interconnect technology, **Number of Mortal units=1142**, chip target lifetime=20 years

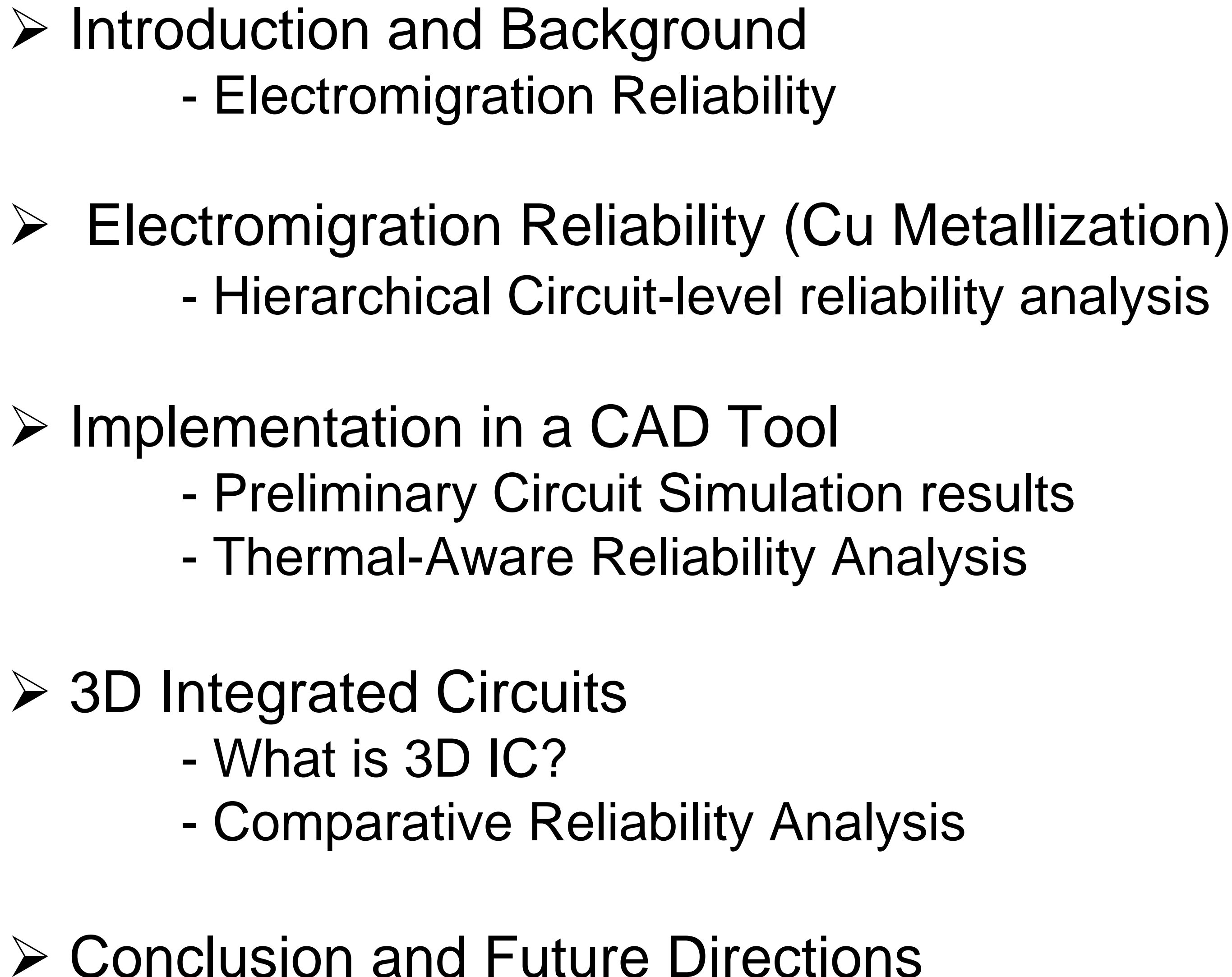
Using worst case thermal analysis with T=105^oC, **prob. of no failure = 0.048**

Operating frequency	Bulk CMOS Technology (Thermal-Aware Result)				Silicon-on-Insulator (SOI) Technology (Thermal-Aware Result)			
	Tmax (^oC)	Tavg (^oC)	Full-chip prob. of no failure	Max FIT	Tmax (^oC)	Tavg (^oC)	Full-chip prob. of no failure	Max FIT
250MHz (P≅2W)	31.56	27.84	≅1	1.01E-10	55.94	28.91	≅1	8.88E-11
1GHz	45.26	30.36	≅1	7.56E-10	142.76	34.63	0.997	68.04
2GHz	63.51	33.72	0.999	9.6E-9	258.51	42.25	2.81E-27	395k
3GHz	81.77	37.07	0.999	1.41E-7				
4GHz	100.0	40.43	0.999	2.95E-4				

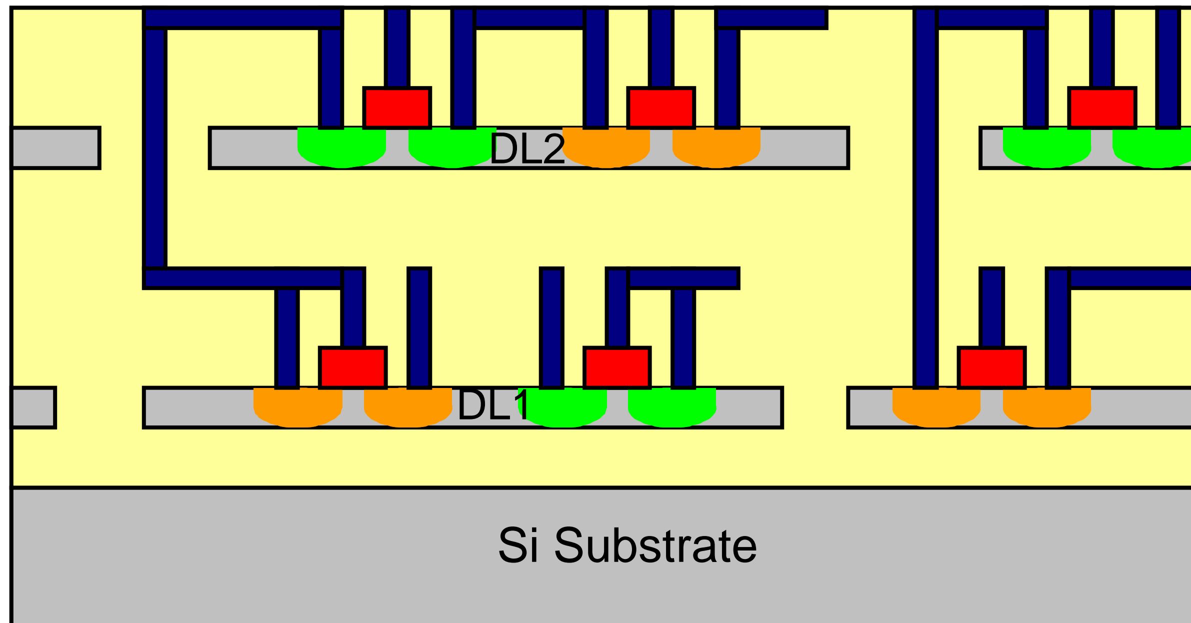
Thermal-aware analysis for

1. performance-reliability trade-off
2. Avoiding over-design

Presentation Outline



Three-dimensional (3D) IC Technology

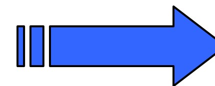


- IBM 3D SOI IC technology by K. Guarini, M. Ieong et al. (IEDM 2002, ECS 2003, and CICC 2003)

- Increased effort on 3D IC technology in industry (Ziptronix, Tru-Si, Intel, Xilinx, Matrix, Freescale)

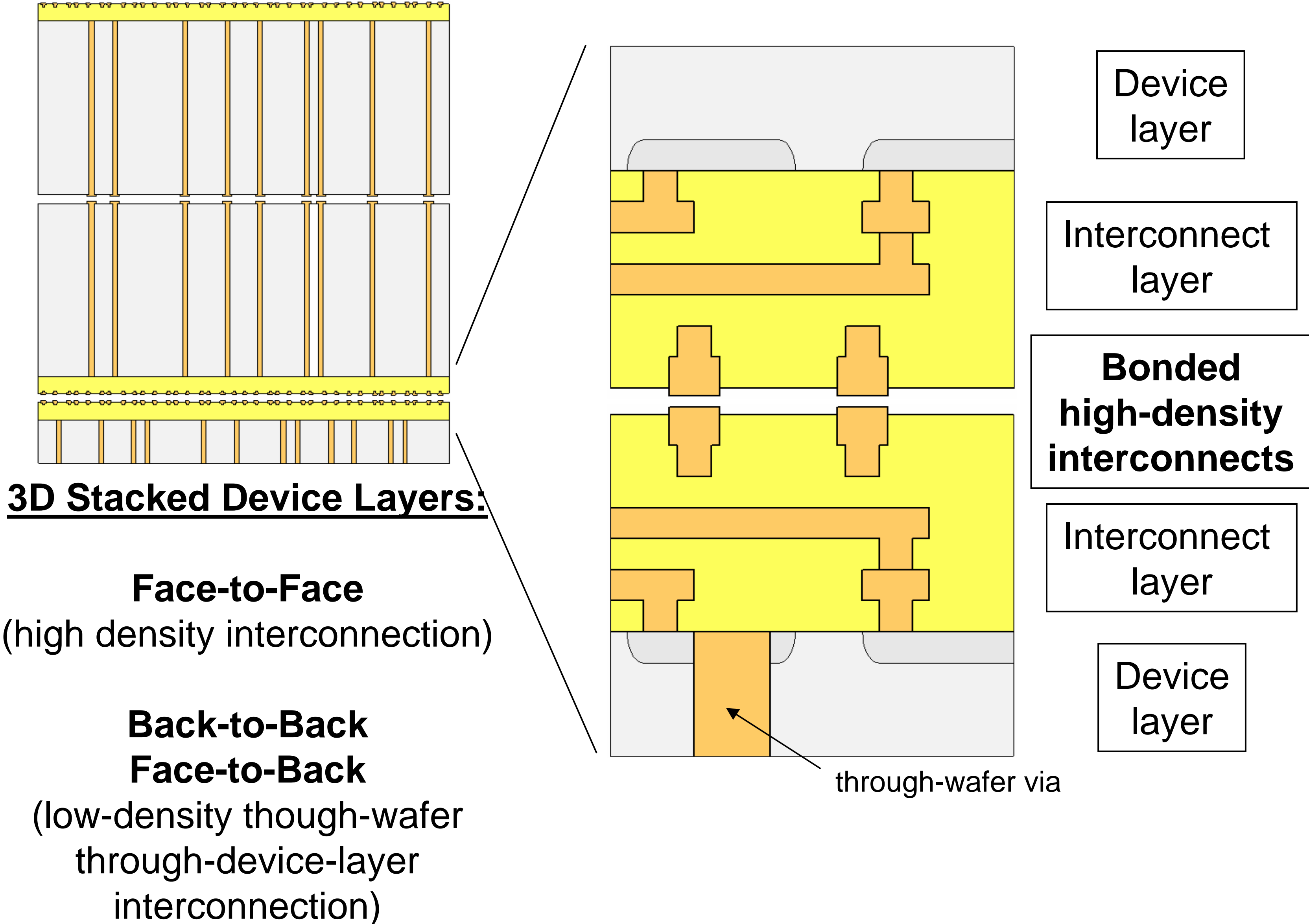
Motivations for 3D IC Technology

- Reduction in wire-length in ICs
- Integration of heterogeneous technologies for SOC



Reduced power
Better signal integrity
High performance
Larger logic span

Bonding Schemes for 3D Technology



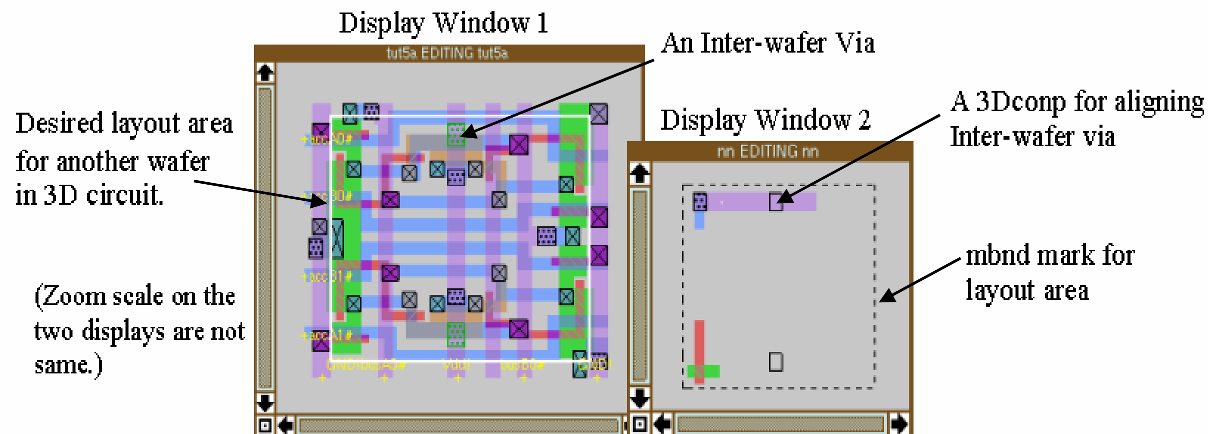
3D-Magic: 3D IC Layout & Extraction Tool

⇒ Developed first public domain layout and RC extraction tool for 3D circuit design extended from Magic

⇒ 3D-Magic is used in coursework (A. Chandrakasan) at MIT. Its newer version is a part of 3D IC design flow and tool research (R. Reif, A. Chandrakasan).

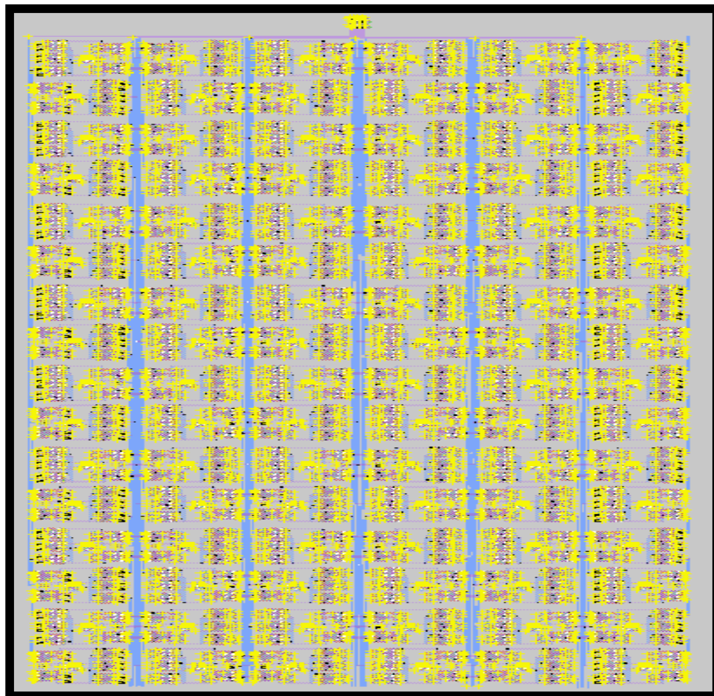
⇒ Publications:

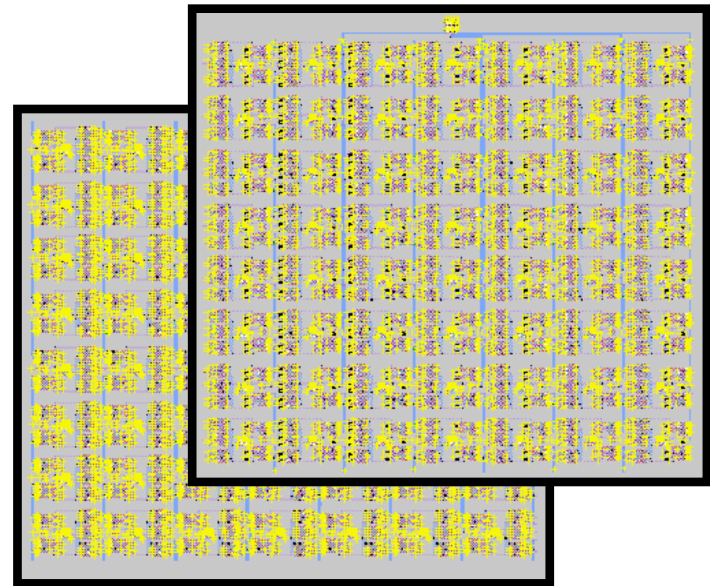
- A Comprehensive Layout Methodology and Layout-specific Circuit Analyses for Three-dimensional Integrated Circuits, ISQED 2002
- Layout-specific Circuit Evaluation in Three-dimensional Integrated Circuits, J. of Analog IC and Signal Processing, (35), 199, 2003



Layout of a 3D FPGA with 3D-Magic

- 8-bit Encryption processor: Layout in two wafers with face-to-back bonding
- Timing Analyses of both 2D (Triptych) and 3D (Rothko) done with PowerMill



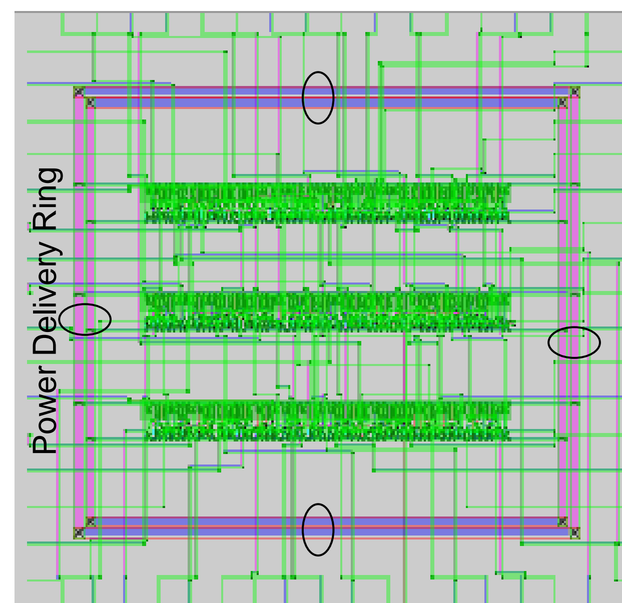


Design and tests by Nisha Checka and Charlotte Lau using 3DMagic.

32-bit Comparator Layout: Cu Technology

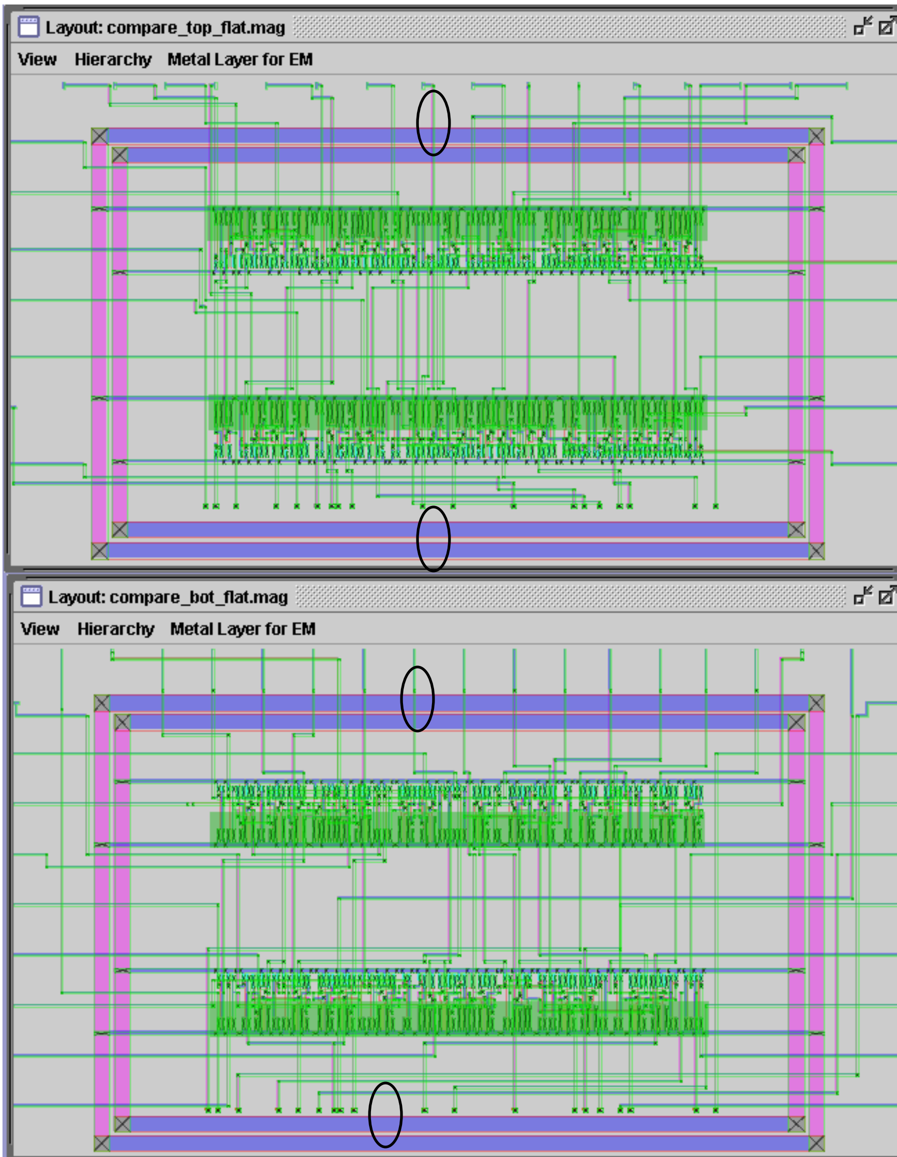
Step 1	Layout Extraction (total # of interconnect trees=1143)	
	Metal Plane	# of Interconnect Trees
	1	580
	2	438
	3	102
	4	20
	5	3
Step 2	Via-based ($j_{max}L$) filter	
	Number of immortal trees identified	1023
Step 3	Via-based ($j_{local}L$) filter	
	Number of immortal trees identified	112
Step 4	Default Model (with σ_{nucl} = 40MPa) on **8 mortal trees**	
	MTTF of 4 mortal tees in Metal 1 (via-above)	23.2 years
	MTTF of 4 mortal trees in Metal2 (via-below)	168.7 years
Step 5	Full chip stochastic analysis (σ=0.81, lognormal) T=105ºC	
	Target chip lifetime	10 years
	Probability of no failure	**0.524**
	Max FIT	15.4k @ 10th year
	t_{50} for full chip	**10.35 years**

- Mortal power lines are marked below



- Increasing the worst mortal line widths by 2, increases t_{50} of each unit from 23.2 years to 92.9 years. Resulting full-chip t_{50}=37.5years, FIT 563, prob. of survival 0.9872

3D 32-bit Comparator Layout Simulation



- 3D circuit layout with 2-wafer face-to-face bonding using 3D-Magic
- Top layout size 141.6 x 75.5 and bottom layout size 141.6 x 79.7
- Inter-wafer vias in metal2 for signal flow.

Reliability Simulation for Cu Technology

- Mortal trees are marked in the layout.

Step 1-3	**Layout Extraction: total # of trees = 1115** **Number of mortal trees = 8**	
Step 4	**Default Model (with σ_{nucl} = 40MPa)**	
	MTTF of each tree	**92.97 years**
Step 5	**Full chip stochastic analysis (σ=0.81, lognormal)**	
	Probability of no failure	**0.97**
	Max FIT	**1020**
	t_{50} for full chip	**30 years**

- Reliability improves due to wire-length reduction and current distribution

Conclusion

$\Rightarrow$ Interconnect related issues (delay, wire-length, signal integrity, reliability) are no longer secondary effects in DSM design.

$\Rightarrow$ Interconnect tree is the right fundamental reliability unit (FRU). Hierarchical reliability analysis with fundamental reliability units (FRUs) allows us to identify 'mortal' or electromigration critical nets.

$\Rightarrow$ A new RCAD tool, SysRel, has been developed and released for electromigration reliability analysis.

- Comparison of Cu and Al based interconnects at the circuit layout level, non-blocking via analysis in Cu, thermal-aware reliability analysis.

$\Rightarrow$ 3D Integrated Circuit technology is an interconnect-driven solution.

- Advantages associated with reduced wire-length
- Heterogeneous integration for SOC
- Many research opportunities: thermal issues, testing, tools, design methodology …..