Thermal Simulation of Laser Annealing for 3D Integration

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Abstract

Fabricating three-dimensional (3D) integrated circuits (IC) frequently involves repeated thermal cycling of the lower layers, and this can be undesirable. The variation of the temperature of various interconnect and device layers of an exemplary 3D IC structure during laser annealing for dopant activation at the upper device levels are determined by solving the light absorption and thermal diffusion equations for an approximate one-dimensional model of the 3D IC. For the structure, the activation of dopants in the upper device layer leads to an unacceptably high temperature in the metal interconnect layers above the first device layer. However, depositing a thin layer of an absorber layer of a metal such as titanium above the device layer to be annealed keeps the temperature rise in the metal interconnects in the lower layers below 800°C. The time variation of the thermal profile within the approximate structure is compared for different number of metal interconnects layers.

Introduction

3D integrated circuits, i.e. electronic chips in which active layers of transistors are stacked one above the other, separated by insulation oxides and connected to each other by metal interconnect wires (Figure 1) may be the best way to continue Moore's Law even in the absence of device scaling [1]. One approach to fabricating 3D circuits is to fabricate independently the 2D circuits corresponding to different levels on separate wafers, align and bond the wafers together, and interconnect them through deep metal vias [2]. An alternative method would be to fabricate devices on crystalline layers above the first layer of active devices and their interconnects sequentially. The crystalline layer can be attached by a low temperature wafer bonding process [3].

One concern in this approach is that high thermal budget requirements in fabricating the devices on the top layer can affect the dopant distribution in the lower layers as well as affect the reliability of the metal wires below the top layer. The most important of the high thermal budget processes involved in transistor fabrication is the high temperature anneal step to activate the dopants in the channel and source drain regions.

Pulsed laser annealing is a very promising technology for dopant activation [4]. Ultra-short, high intensity laser pulses can melt the silicon substrate containing dopants. During the subsequent re-crystallization, the dopants move to substitutional sites in the lattice, thereby becoming electrically activated. However, undesirable heating of lower metal and device layers may occur during this process. Here, we describe 1D simulations to study the temperature excursions of the lower layers.

One-dimensional model

We model the complicated structure of a 3D IC containing multiple device layers connected to each other by different levels of metallization and deep interconnect vias as a simple one-dimensional structure. We assumed that the metal layer is a uniform layer of Copper, and the Inter-Layer Dielectric (ILD) layer is made of a uniform layer of SiO_2. The thermal conduction pathways through the vias are neglected in

this first order approximation. This is a justifiable assumption as we are interested in finding the maximum temperature rise in the metal interconnect layers above the first device layer. Hence, neglecting the thermal conduction pathways through the vias will result in conservative estimates for the temperature excursions in the top metal layers. The top silicon layer containing the dopants to be activated is assumed to be 50 nm thick. Each ILD and metal layer is assumed to be 300 nm thick, and corresponds to a typical 90 nm generation logic technology [5]. The substrate silicon is assumed to be 20 μm thick so that it effectively behaves like a semi-infinite layer, and at the same time minimizing the computational complexity. A 20 ns pulse (full width at half maximum) of 1064 nm laser light is used in this simulation.

The simulations were carried out on a simulation tool called PGILD, developed by Verdant Inc, San Jose. PGILD is a one-dimensional simulator to calculate the thermal profile in structures with arbitrary number of layers and materials during laser annealing. It solves the intensity distribution equations for the light and the thermal diffusion equations for the structure at each time and position in the structure. Temperature dependent values of thermal conductivity, specific heat [6], [7] and the refractive index coefficients of the different materials [8], [9] are used in the calculations. Radiative cooling is not accounted for in the simulation.

A sufficiently fine grid (about 100 points in each layer) was used in the simulations so as to give consistent and meaningful results. The simulations have been done for various energy densities and the best results are reported in this paper.

Procedure and Results

We first simulated the effect of directly annealing the Si layer on top of a pre-existing device layer with just one metal interconnect layer (Figure 2 inset). Due to the low absorption coefficient of Si at 1064 nm wavelength, most of the light passes through the top silicon layer and is absorbed in the copper layer below. As a result, the Cu layer reaches an unacceptably high temperature before the top silicon layer attains the value needed for melting and re-crystallization (~1200 °C) (Figure 2). Hence, it is not possible to activate the dopants on the top silicon device layer without melting and compromising the reliability of the metal layer below.

To circumvent this problem, an absorbing stack layer is added to the top of the previous structure (Figure 3 inset). This stack consists of a 70 nm thick layer of a refractive metal like Tungsten deposited above a 100 nm thick layer of SiO_2 above the second device layer. The thin metal layer on top absorbs the light more efficiently than the layers below, acting as a heat source to melt the device layer beneath it. These deposited stack layer can be etched off after the annealing step. The simulation results shown in Figure 3 confirm that it is possible to melt the top silicon layer and activate the dopants in the top layer, without affecting the device or metal layers underneath. Diffusion of copper at these temperatures can be prevented by using WN_2 cladding layers [10].

An actual 3D IC structure would have many levels of metal interconnect layers and not just the single layer as we have modeled above. To determine how the heat profile is affected by the number of metal interconnect layers between the device layers, we repeated the simulations for the structures shown in the inset of Figure 4 and 5. These structures have two and three layers of interconnects respectively compared to the simpler structure which had only one metal interconnect layer used in the earlier simulation. It is clear from the results shown in Figure 4 and 5 that there are no significant changes in the time variation of the heat profile as the number of metal layers between the two device layers increases. We believe that attaching a heat

sink to the actual 3D IC structure built on a 0.5 mm thick substrate wafer would keep the substrate temperature at much lower levels at the end of the annealing process.

Conclusions

One-dimensional simulations have been used to determine the thermal profile of 3D IC structures during laser annealing. Activation of dopants on the upper device levels is not possible by direct annealing, without melting the metal interconnect layers above the lower device layers and thus causing reliability problems. A practical solution to this problem is to deposit an absorber layer of a metal like titanium above the structure to be annealed. Simulations show that the thermal excursions in the lower layers are not high enough to cause dopant redistribution in the lower device layers or reliability problems in the metal interconnect layers between the two active layers. From these simulations, we conclude that laser annealing is a very promising technology for activation of dopants on the upper device layers of a 3D IC without compromising the quality of devices and metal interconnects underneath it, thus opening up a window for sequential fabrication of three-dimensional integrated circuits.

Acknowledgement

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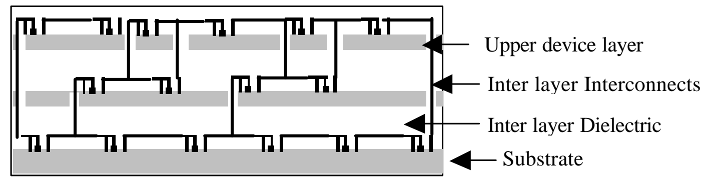

Figure 1. Schematic of a 3D IC showing multiple device and interconnect layers

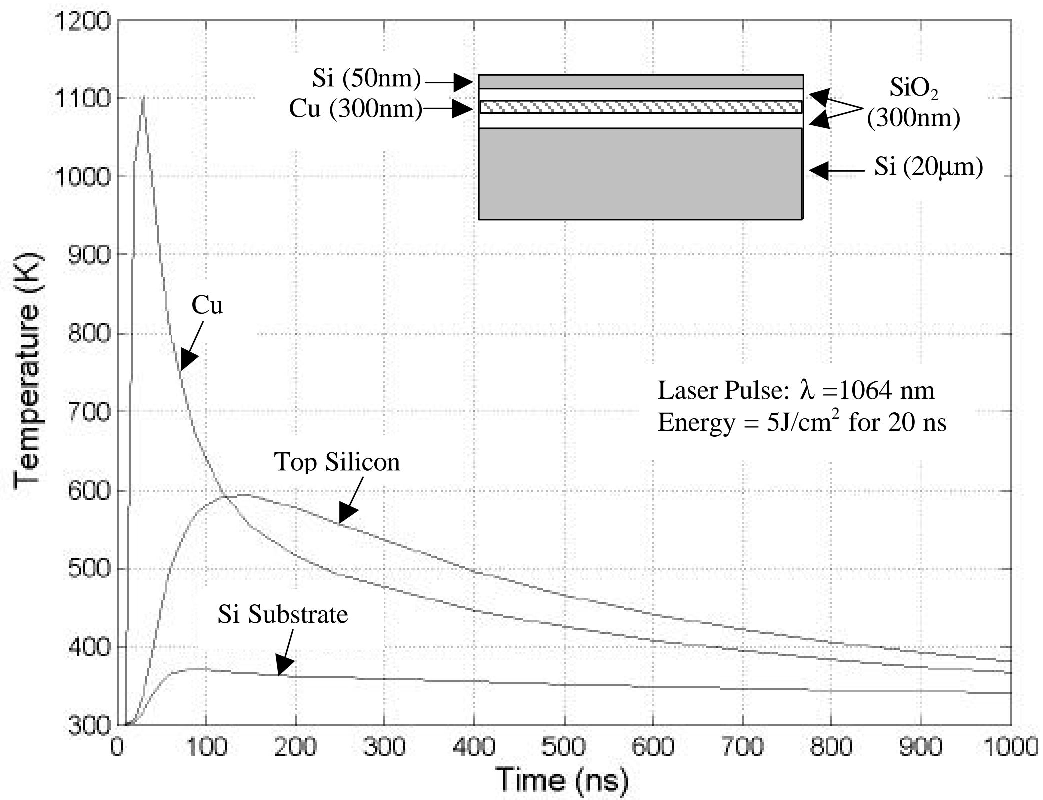

Figure 2. Thermal profiles during laser annealing of the 3D IC structure with one metal layer between the two device layers. A schematic of the 1D model of the structure with the dimensions used in this simulation is shown in the inset.

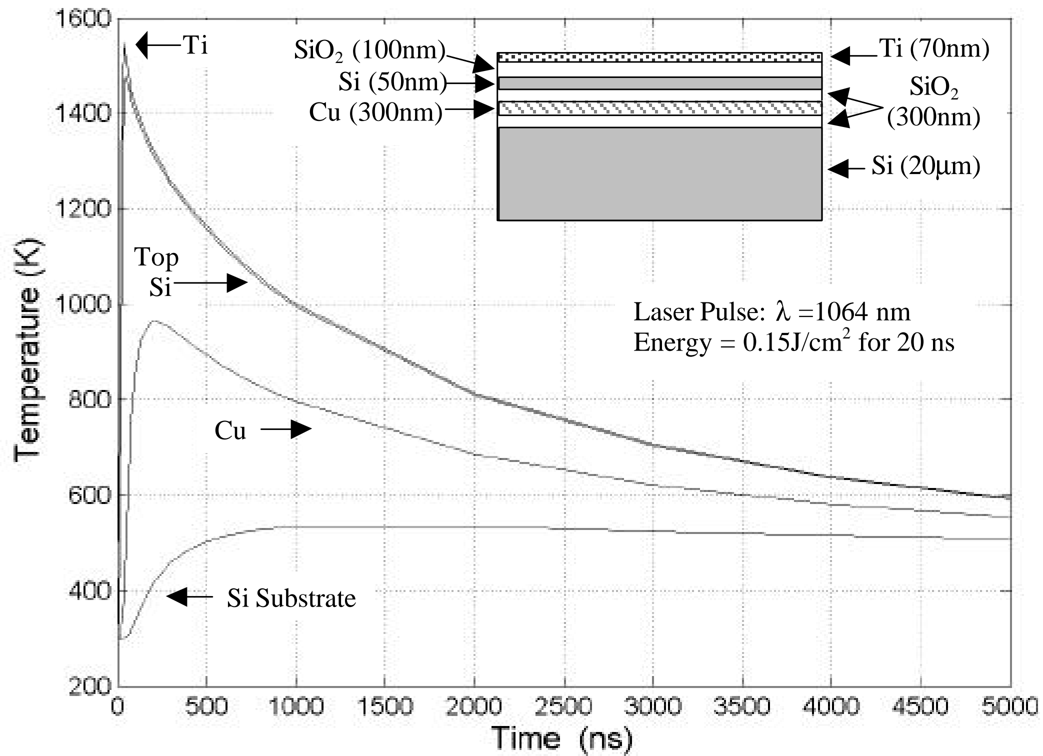

Figure 3. Thermal profile during laser annealing of the 3D IC with Ti absorber coating and one metal layer between the two device layers. A schematic of the 1D model of the structure with the dimensions used in this simulation is shown in the inset.

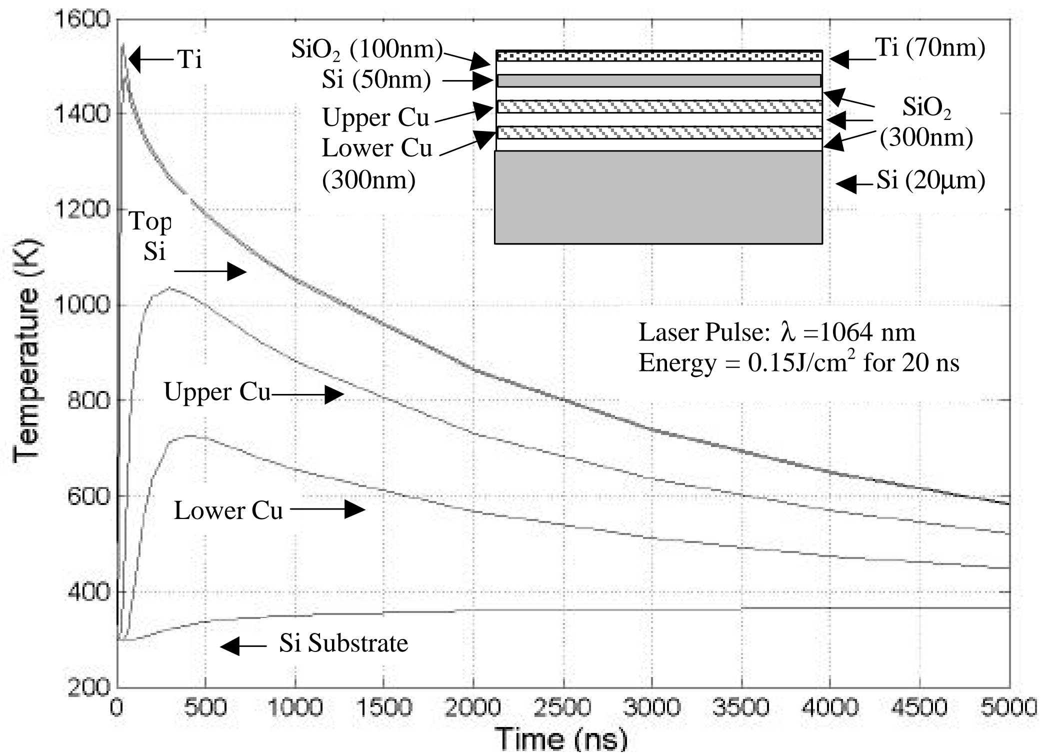

Figure 4. Thermal profile during laser annealing of the 3D IC with Ti absorber coating and two metal layers between the two device layers. A schematic of the 1D model of the structure with the dimensions used in this simulation is shown in the inset.

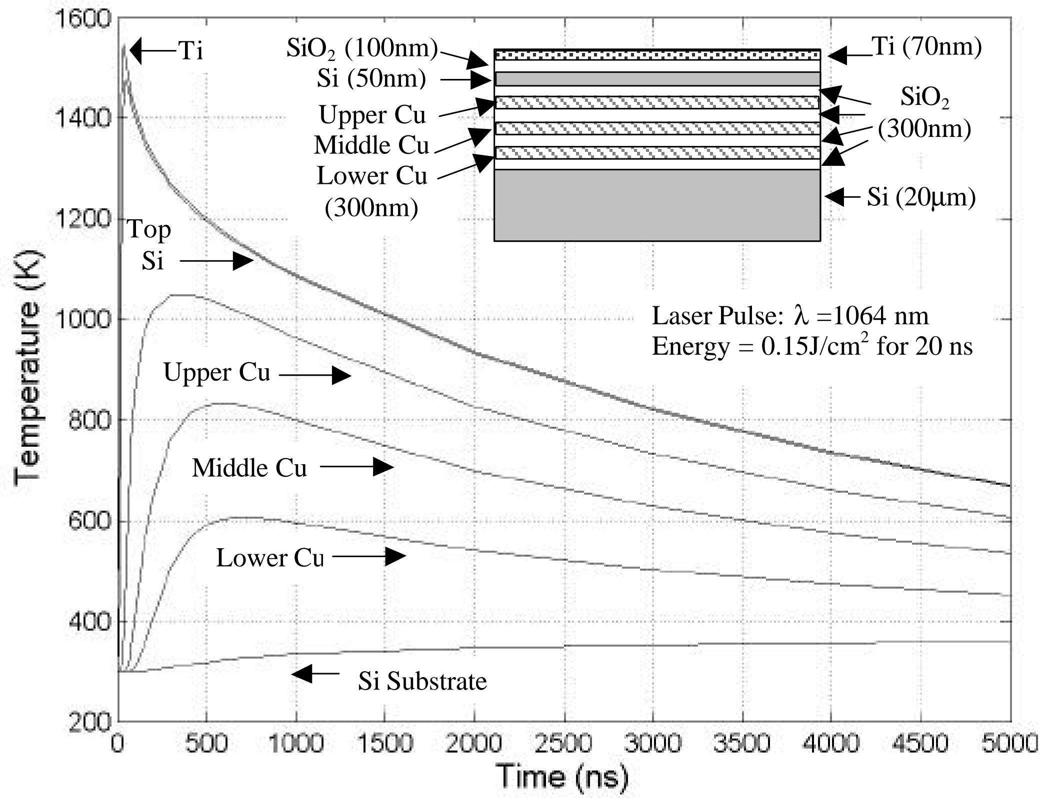

Figure 5. Thermal profile during laser annealing of the 3D IC with Ti absorber coating and three metal layers between the two device layers. A schematic of the 1D model of the structure with the dimensions used in this simulation is shown in the inset.