Simultaneous Switching Noise and Resonance Analysis of On-Chip Power Distribution Network

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Abstract

This paper presents a frequency-domain technique for finding the worst-case time-domain voltage variations in the RLC power bus of digital VLSI circuits. Pattern independent maximum envelope currents are used for the logic gates and macroblocks. The voltage drop/surge at a power bus node is expressed in term of the currents using sensitivity analysis. The sensitivity information together with an optimization procedure are applied to find the upper-bounds on the voltage variations at the targeted bus nodes. The resonance problem due to the on-chip RLC power distribution network is analyzed base on the frequency-domain sensitivity analysis. Comparisons to SPICE simulation of circuits extracted from layouts are used to validate our approach.

1 Introduction

The rapid advances in process technology and the dramatic increase in the number of devices on a chip are making the power delivery network in VLSI circuit design a major design challenge. Switching activity of high speed CMOS circuit may produce large currents or current derivatives. These current transients can generate large potential drops/surges due to the parasitic resistance and inductance of the power distribution network. This is referred to as IR drop and Ldi/dt noise or simultaneous switching noise (SSN). In addition to growing noise generation, the supply voltage are lowered in accordance with the CMOS scaling rules. The combined result of increased noise and reduced supply level can be a large degradation in the signal-to-noise ratio of high speed CMOS circuit.

The power supply variation can cause logic errors and adversely affect the circuit performance. Excessive surge in power bus voltage or drop in ground bus voltage can cause the following problems: transistor gate oxide reliability problems due to the electrical overstress, increased latch-up susceptibility of devices due to increased minority carriers, and discharge of dynamically held nodes resulting in logic errors. Excessive drop in power bus voltage or surge in ground bus voltage can cause following problems: decreases the device drive capability, increases the logic gate delay, reduces the noise margin. Hence, it is important to estimate these voltage variations in the power distribution network. Extensive researches have been done for IR drop analysis [1, 2, 3, 5]. Most of the previous works on SSN estimation have been limited to I/O driver circuits [6, 7, 8] instead of the on-chip core logic circuits. In this work, we focus on the SSN noise upper-bounds estimation due to the on-chip core logic circuit using input-independent technique. Comparing with input-dependent approach [2, 4], input-independent technique can find the voltage variation upper-bounds in the power grid over all possible input excitations quickly.

Simultaneous switching noise is caused by the inductances inherent in the power distribution metal lines. When many circuits switch at the same time, the current supplied by the power lines can change rapidly, and the inductive voltage drop along the line can cause the power supply level to go down. The resulting voltage glitch is proportional to the switching speed, the number of circuit components switching simultaneously and the effective inductance of the power line. At present, Ldi/dt noise caused by simultaneously switching output buffers is more significant than the noise associated with on-chip circuitry. However, both components may become equally important for the next generation high performance VLSI circuits. The total capacitive load associated with on-chip core logic circuits rises as minimum feature size shrinks. With improved circuit speed, both the average current (I_{avg}) required to charge and discharge these capacitances and the speed at which this current is switched (di/dt) increase. As a result, total on-chip current may change by large amounts within very short time periods. The SSN due to the internal switching current become comparable to the SSN due to the output buffers switching current. Hence, the voltage fluctuations in the power bus associated with on-chip circuitry can not be ignored in the noise calculation.

To ascertain if inductance is significant in determining the electrical response of a given on-chip power distri-

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bution metal line, one must compare the line's characteristic impedance Z_0 with line's total resistance R_{line}. We know that for the case of quasi-TEM propagation in a lossy transmission line, inductance is negligible if [9]:

$$R_{line} >> Z_0 = \sqrt{L/C} \tag{1}$$

or

$$R_{line}C >> L/R_{line} \tag{2}$$

where L and C are the inductance and capacitance per unit length. Notice that to increase the switching speed, time constant RC needs to be reduced. This makes it harder to meet the condition of Eq.(2) for a more advanced process.

Even if the instantaneous voltage fluctuation is very small, the periodic nature of the digital circuits can cause resonance [10, 11]. The resonance frequency due to the package inductance(L) and the total decoupling capacitance(C) can be estimated by the expression:

$$f_{chip} = \frac{1}{2\pi\sqrt{LC}} \tag{3}$$

To prevent oscillations at the power lines, the resonance frequency f_{chip} should be much higher or lower than the system clock frequency. In [11], the resonance frequency derived using Eq.(3) is lower than the circuit operating frequency and decreases for the circuits with higher clock frequency. However the resonance problem due to the on-chip RLC power distribution network is not addressed. In section 3, the details of on-chip resonance frequency analysis are explained

The parasitic resistance R_{line} of power distribution network gives rise to IR drops. But the same parasitic resistance helps the resonance problem by introducing a damping effect and reducing the resonance impedance. If simultaneous switching noise is dominant, the decrease of R_{line} may increase the total noise in the power distribution network. This is shown in section 5.

The paper is organized as follows. In section 2, we develop the algorithm to estimate the voltage variation upper-bounds in the RLC power distribution network. The resonance analysis of on-chip power grid is explained in section 3. Techniques that can reduce the simulation time for large VLSI circuits are introduced in section 4. In section 5, experiment results are presented to validate our work. In section 6, we draw some conclusions.

2 Simultaneous Switching Noise Analysis

Simultaneous switching noise (SSN) is caused by the inductance inherent in the power distribution metal lines. When many circuit switch at the same time, the current supplied by the power lines can change rapidly, and the inductive voltage drop along the line can cause the power supply level to go down. SSN can be caused by the simultaneous transitions of the on-chip core logic circuits and the I/O driver circuits. Most of existing techniques emphasize on computing the SSN due to the I/O driver circuits [6, 7, 8]. In this section, we develop the algorithm to compute the positive and negative upper-bounds of SSN due to the on-chip logic circuits.

2.1 Noise Upper-Bounds Estimation

Applying Laplace transform to the power bus equation $\mathbf{YV} = \mathbf{I}$ with zero initial conditions, we get:

$$\mathbf{Y(s)V(s)} = \mathbf{I(s)} \tag{4}$$

$\mathbf{Y}$ is the admittance matrix. $\mathbf{I(s)}$ is the Laplace transform of the current source vector of each circuit component. The frequency spectrum of the maximum voltage drop waveform at node j is:

$$V_j(s) = \mathbf{e_j}^{\mathbf{T}}\mathbf{V(s)} \tag{5}$$

$\mathbf{e_j}^{\mathbf{T}}$ is a unit vector,

$$e_{ij} = \begin{cases} 1 & \text{if } i = j \\ 0 & \text{else} \end{cases} \tag{6}$$

Using Eq.(4), replace $\mathbf{V(s)}$ in Eq.(5):

$$V_j(s) = \mathbf{e_j}^{\mathbf{T}}\mathbf{Y(s)}^{\mathbf{-1}}\mathbf{I(s)} \tag{7}$$

If we define:

$$\mathbf{e_j}^{\mathbf{T}}\mathbf{Y(s)}^{\mathbf{-1}} = \mathbf{\Psi_j}^{\mathbf{T}} \tag{8}$$

where $\mathbf{\Psi_j}$ is the frequency-domain sensitivity vector of node j. The frequency spectrum of $V_j(s)$ equals to the inner product of vectors $\mathbf{\Psi_j}$ and $\mathbf{I(s)}$.

$$V_j(s) = \mathbf{\Psi_j}^{\mathbf{T}}\mathbf{I(s)} \tag{9}$$

In the time-domain, all the elements in vectors $\mathbf{\Psi_j}$ and $\mathbf{I(s)}$ are time dependent. $V_j(t)$ can be expressed as the summation of the convolution between the corresponding elements from these two vectors. The sensitivity vector $\mathbf{\Psi_j(s)}$ can be calculated by solving Eq.(10).

$$\mathbf{Y(s)\Psi_j(s)} = \mathbf{e_j} \tag{10}$$

The sensitivity vector $\mathbf{\Psi_j}$ is frequency dependent. Eq.(10) needs to be solved at different frequencies. The frequency-domain samples are selected as following. Let T_{clk} be the user specified clock period. T_s is the sampling time. The sampling rate is chosen fast enough that there is no aliasing. From sampling theorem, the signal frequency spectrum is in the range of $-F_s/2$ and $F_s/2$, where $F_s = 1/T_s$. The number of samples has to be same for the time-domain and frequency-domain. From this explanation, it is clear that Eq.(10) needs to be solved at the frequencies from $-F_s/2$ to $F_s/2$ with step F_s/N_s, where N_s is number of samples.

$$N_s = T_{clk}/T_s \tag{11}$$

After all the samples of the sensitivity vector in the frequency-domain are found, they are transformed back

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to the time-domain using Inverse Fast Fourier Transform(IFFT). Based on Eq.(9), the voltage drop waveform V_j can be expressed as the convolution of vector $\mathbf{\Psi_j}^\mathbf{T}$ and $\mathbf{I}$ in time-domain.

$$\begin{aligned} V_j(t) &= \mathbf{\Psi_j} \otimes \mathbf{I(t)} \\ &= \int_0^{T_{clk}} \mathbf{\Psi_j}^\mathbf{T}(\tau)\mathbf{I}(t-\tau)d\tau \\ &= \int_0^{T_{clk}} \sum_{i=1}^{g_N} \Psi_{ij}(\tau) I_i(t-\tau)d\tau \end{aligned} \quad (12)$$

g_N is the total number of circuit components in the circuit. Each element of the time-domain sensitivity vector is a time dependent variable. We have N_s samples for each of this variable distributed evenly from 0 to T_{clk}. The current envelope drawn by each circuit components is also sampled at the same time instants. Because $\Psi_{ij}(t)$ and $I_i(t)$ are sampled at discrete time instants, the integration in Eq.(12) becomes a summation as shown in Eq.(13).

$$\begin{aligned} V_j(nT_s) &= \frac{T_{clk}}{N_s} \sum_{k=0}^{N_s-1} \sum_{i=1}^{g_N} \Psi_{ij}(kT_s) I_i[(n-k)T_s] \\ &= \frac{T_{clk}}{N_s} \sum_{i=1}^{g_N} \sum_{k=0}^{N_s-1} \Psi_{ij}(kT_s) I_i[(n-k)T_s] \\ &= \sum_{i=1}^{g_N} V_{ij}^d \end{aligned} \quad (13)$$

In Eq.(13), the maximum voltage variation at node j at time nT_s is expressed as the summation of contributions from all the circuit components. The contribution of circuit component i to $V_j(nT_s)$ is expressed as the convolution of $\Psi_{ij}(t)$ and $I_i(t)$ at time nT_s. For R/RC power bus network, $\Psi_{ij}(t)$ is always non-negative.

proof: Let $\mathbf{I(t)}$ be the vector of currents at various nodes of the R/RC network, the following relationship exists between $\mathbf{V(t)}$ and $\mathbf{I(t)}$ for power bus:

$$\mathbf{YV} = \mathbf{I} \quad (14)$$

and

$$V_j(t) = \mathbf{e_j^T Y^{-1} I(t)} \quad (15)$$

For R/RC network, its admittance matrix $\mathbf{Y}$ has following properties:

- It is a symmetry matrix.
- All the elements on the diagonal are positive.
- All the elements off the diagonal are negative.

The matrix with these properties is known as M-matrix. All the elements of a M-matrix inverse matrix are positive [14]. If $\mathbf{I(t)}$ in Eq.(15) is instant-wise upper-bounds on the current waveform for all the circuit components, the $V_j(t)$ is also the maximum voltage drop waveform.

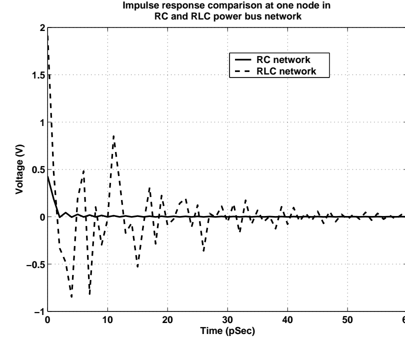

Figure 1: Impulse response at one node in RC and RLC power bus network

Using frequency-domain sensitivity analysis, $V_j(t)$ can also be expressed as:

$$V_j(t) = \sum_{i=1}^{g_N} \Psi_{ij}(t) \otimes I_i(t) \quad (16)$$

Assuming there is no aliasing during sampling process, Eq.(15) and Eq.(16) should give the same result, i.e., $V_j(t)$ in Eq.(16) is also the maximum voltage drop if $I_i(t)$ is the maximum current envelop. This is true only if $\Psi_{ij}(t)$ is non-negative at any given time. ■

Since the admittance matrix of a RLC network is not a M-matrix, $\Psi_{ij}(t)$ can be negative at some time instants. Fig. 1 shows the comparison of the voltage impulse responses of one node in RC and RLC power bus network. The unit impulse current excitation is connected at the same node. Due to this difference between RLC and RC power bus network, $V_j(t)$ calculated using Eq.(12) is not guaranteed to be the upper-bounds if $I_i(t)$ is the maximum current envelop. In order to solve this problem, $\Psi_{ij}(t)$ is split into two variables $\Psi_{ij}^d(t)$ and $\Psi_{ij}^s(t)$.

$$\Psi_{ij}^d(t) = \begin{cases} \Psi_{ij}(t) & \text{if } \Psi_{ij}(t) > 0 \\ 0 & \text{else} \end{cases} \quad (17)$$

and

$$\Psi_{ij}^s(t) = \begin{cases} 0 & \text{if } \Psi_{ij}(t) > 0 \\ \Psi_{ij}(t) & \text{else} \end{cases} \quad (18)$$

The maximum voltage drop $V_j^d(t)$ and the maximum voltage surge $V_j^s(t)$ at the specified node in the power bus are formulated as:

$$V_j^d(t) = \sum_{i=1}^{g_N} \Psi_{ij}^d(t) \otimes I_i(t) \quad (19)$$

and

$$V_j^s(t) = \sum_{i=1}^{g_N} \Psi_{ij}^s(t) \otimes I_i(t) \quad (20)$$

Eq.(19) and Eq.(20) give us the positive and negative noise upper-bounds at the target node in the RLC power distribution network.

2.2 Top-level Power Grid Model

The number of nodes in the power distribution network can be extremely large because the power distribution

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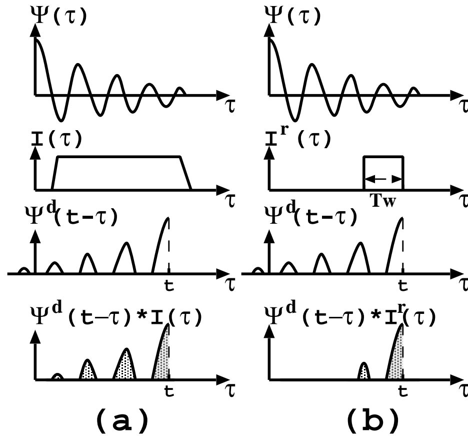

Figure 2: Comparison of convolution results using different current signatures for logic gate

network connects to every transistor in an integrated circuit. But a power bus is typically designed as a hierarchical structure in which the top-level power-grid connects to the macroblocks and the power distribution network inside the macroblock connects to the logic gates. Power bus analysis techniques exploit this hierarchical structure by splitting the problem into evaluation of the current signature of each macroblock (non-linear devices) and the use of these currents to analyze the linear top-cell power distribution network to estimate the voltage variation waveforms. These waveforms are then propagated back to compute the voltage drop at nodes inside the macroblocks by using a current signature for each logic-gate (non-linear device). This hierarchical abstraction was proposed in [15]. The maximum current envelope derived from pattern independent technique [13] is used as current signature for each macroblock. The frequency-domain sensitivity vector $\mathbf{\Psi_j}$ is calculated by solving Eq.(10) of top-level RLC power bus network. The voltage drop/surge upper-bounds at the contact points to each macroblock are derived from Eq.(19) and Eq.(20).

2.3 Power Grid inside the Macroblock

The power grid inside the macroblock consists of nonlinear logic gates plus linear RLC interconnects. In [5, 12], each standard cell is assumed to draw its maximum current during its switching timing window. Depending on the circuit design, the width of some logic gates switching timing window may be much wider than their real current waveforms. Applying the maximum current envelopes derived in this way gives a pessimistic upper-bound on the supply voltage variation as illustrated in Fig. 2(a). The shadow area is the convolution of $\Psi^d(\tau)$ and $I_i(\tau)$ at time instant t.

In order to get a tighter upper-bound, a new current signature for each logic gate is defined. A new parameter, current waveform maximum duration time T_w, is characterized for each standard cell using SPICE simulation. When a standard cell output has low-to-high transition, it draws current from the power bus. Let I_{peak} be the peak current value of the current waveform. I_{th} equals to 10% of I_{peak}. The current waveform duration time is defined as the time between the two I_{th} points on the current waveform. T_w is the maximum value of all the possible duration times of the stand cell. The new current signature $I^r(t)$ for a logic gate is constructed assuming that the gate draw its maximum current during a time interval T_w. $I^r(t)$ can slide inside the gate's switching timing window since we assume the gate can switch at any time during this time interval. As shown in Fig. 2(b), when $I^r(\tau)$ is aligned with $\Psi^d(t-\tau)$, their convolution reach the maximum value. Then the voltage drop/surge upper-bounds at the target node can be derived from Eq.(19) and Eq.(20). But these results can be pessimistic upper-bounds due to the logic constraints in the circuit [13]. Given an input vector pair, not all the gates in the circuit draw currents from the power bus. Constraint graph optimization tries to find an independent set of gates. When they switch, Eq.(19) and Eq.(20) are maximized. This procedure is performed at each time interval in order to find the upper-bounds for V_j^d and V_j^s.

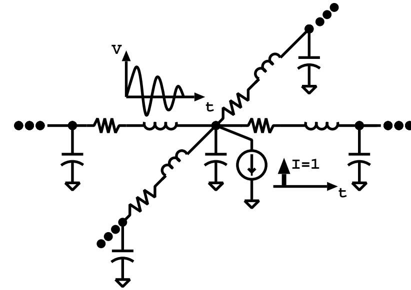

Figure 3: Impulse response at a node in RLC power bus

3 Resonance of On-Chip Power Grid

The package inductance combined with on-chip decoupling capacitance forms an RLC circuit that can resonate. The resonance frequency due to package inductance(L) and total decoupling capacitance(C) can be estimated by Eq.(3). To prevent oscillations at the power lines, this resonance frequency should be much higher or lower than the system operation frequency. This is discussed in [11].

However the resonance problem due to the on-chip RLC power distribution network is not addressed in their work. Based on the previous frequency-domain sensitivity analysis, the impedance frequency spectrum at each node in the power bus is available. It is also the impulse response frequency spectrum at the node that is connected to a unit impulse current excitation as shown in Fig. 3. A typical impedance frequency spectrum is shown in Fig. 4. The first peak of the frequency spec-

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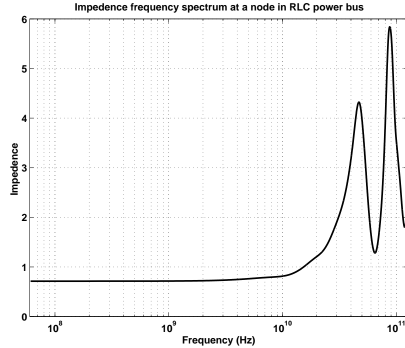

Figure 4: A typical impedance frequency spectrum at a node in RLC power distribution network

trum was observed at $48GHz$. As the circuit operation frequency approaches this peak, the resonance problem due to on-chip RLC power distribution network will become the major concern.

4 Simulation Time Reduction Techniques

Using the approach described in the previous sections, the simulation time grows linearly with the number of nodes analyzed. Thus, it is highly desirable to shorten the simulation time at each node. The following techniques are proposed to reduce the computation time.

First, a straightforward technique is parallel programming. Parallel programming is applicable in this case because the procedures for finding the worst-case voltage drop waveforms at different nodes in the power bus are independent of each other, although they may share common data, such as formulation and factorization of bus matrix equation, sampling of gate currents, and gate switching intervals.

Secondly, the constraint graph optimization is performed during a time interval only if Eq.(19) and Eq.(20) is higher than a user specified value.

Thirdly, the number of nodes of interest at any given time can be reduced by focusing only on the nodes connected to switching gates at any given time point since they are the gates whose performance are affected by the voltage variation across them.

Fourth, constraint graph optimization is usually a time consuming step. The size of the graph can to be reduced in order to speed up the simulation. This is achieved by finding the vertices that have weights, $\Psi_{ij}(t) \otimes I_i(t)$ in Eq.(19) or Eq.(20), below a certain threshold and eliminating them from the constraint graph. In our experiments, we found that at any given time point, only few gates contribute to the total value in Eq.(19) or Eq.(20). They are the gates that are close to the specified node. Based on this observation, at every time point we only keep those vertices in the optimization graph that contribute most to the summation in Eq.(19) or Eq.(20). We implement it this way.

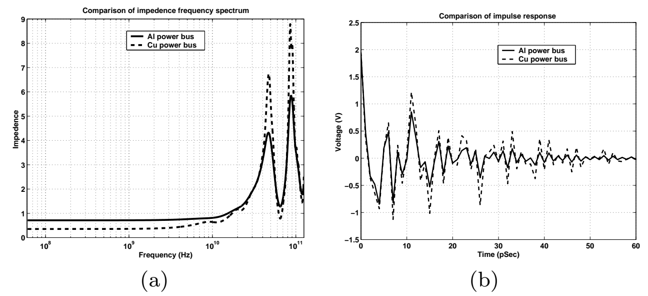

Figure 5: Comparisons of (a)impedance frequency spectrum and (b)impulse response at a node in Al and Cu power bus

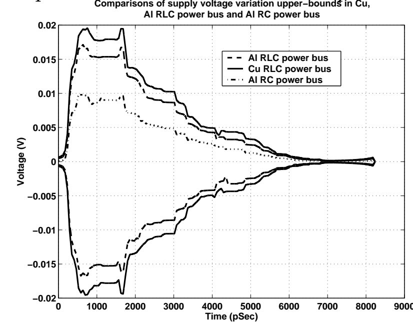

Figure 6: Comparisons of supply voltage variation upper-bounds in Cu, Al RLC power bus and Al RC power bus

At every time point, the vertices are sorted according to their weights, with the vertex having the highest weight selected first. Vertices are then selected based on their weights in descending order until the summation in Eq.(19) or Eq.(20) reaches a certain percentage of the total sum. Note that the weights of the vertices of the vertices change from one time point to the next. Typically the simulation speed gains are more than 10 with the error smaller than 5%.

5 Experimental Results

The parasitic resistance of power distribution network is the source of IR drops. Ironically, the same parasitic resistance helps the resonance problem by introducing a damping effect and reducing the resonance impedance. If the simultaneous switching noise is dominant, the decrease of resistivity of power bus metal line may result in larger voltage variation in the RLC power distribution network. Fig. 5 shows the comparisons of the impedance frequency spectrum and impulse response at a node in Al and Cu power bus network.

If copper is used as power bus metal line, the resistivity reduces by 1.7 times. The DC component in Fig. 5(a) that corresponds to IR drop decreases. However, the SSN increases because of less damping resistance as shown in Fig. 5(b). The final voltage variation upper-bounds are shown in Fig. 6.

The simulation results for some ISCAS85 benchmark circuits are shown in table 1. All the benchmark circuits are implemented using 0.35μ, 3V technology. The RC

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Table 1: Simulation results of some benchmark circuits

Circuit Name	Gate Num.	Total Vdd Nodes	Noise Upper-bounds			SPICE (V)		CPU Time (Sec)
			IR Drop	IR and SSN				
C432	204	566	0.018	0.040	-0.038	0.029	-0.026	2.18
alu2	347	446	0.039	0.061	-0.063	0.034	-0.028	14.1
C880	432	564	0.057	0.085	-0.086	0.089	-0.072	26.7
C1908	519	821	0.056	0.110	-0.117	0.052	-0.051	71.7
C499	526	660	0.032	0.045	-0.042	0.035	-0.032	37.7
C1355	526	995	0.025	0.033	-0.032	0.017	-0.019	34.1
alu4	686	847	0.028	0.044	-0.043	0.022	-0.026	208.2
dalu	746	914	0.081	0.119	-0.114	0.081	-0.074	308.6
C3540	1274	1904	0.148	0.218	-0.209	0.145	-0.147	2022
C5315	1754	2185	0.132	0.214	-0.228	0.103	-0.109	2950
C6288	2400	3064	0.160	0.227	-0.213	0.161	-0.146	7958
C7255	2391	3457	0.218	0.298	-0.271	0.278	-0.263	8432

interconnect parasitics of the power bus are extracted from the layout. Each resistance is replace by two resistances with half the value and an inductance of a nominal value(0.05nH) between the two resistances. Column 4 shows the maximum IR drop in the resistive power bus. Column 5 and 6 are the maximum voltage drop/surge in the RLC power bus using the technique in this work. A small group of input patterns that cause large noise in the power grid are chosen using Genetic Algorithm [16]. The maximum voltage variations in the power bus after applying these input patterns are derived from SPICE simulation results and shown in column 7 and 8. Last column is the simulation time of column 5 and 6 on SunUltra5 workstation.

6 Conclusions

In this paper, we presented an input-independent method for finding the upper-bounds on the voltage variations due to IR drop and Ldi/dt noise in RLC power bus of digital VLSI circuit. The approach relies on the frequency-domain sensitivity analysis and constraint optimization. The program can find the supply voltage noise upper-bounds in a fast and accurate way. The resonance problem due to the on-chip RLC power distribution network was also analyzed. Several techniques were introduced to reduce the simulation time. Comparisons with SPICE simulation are used to validate our approach.

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