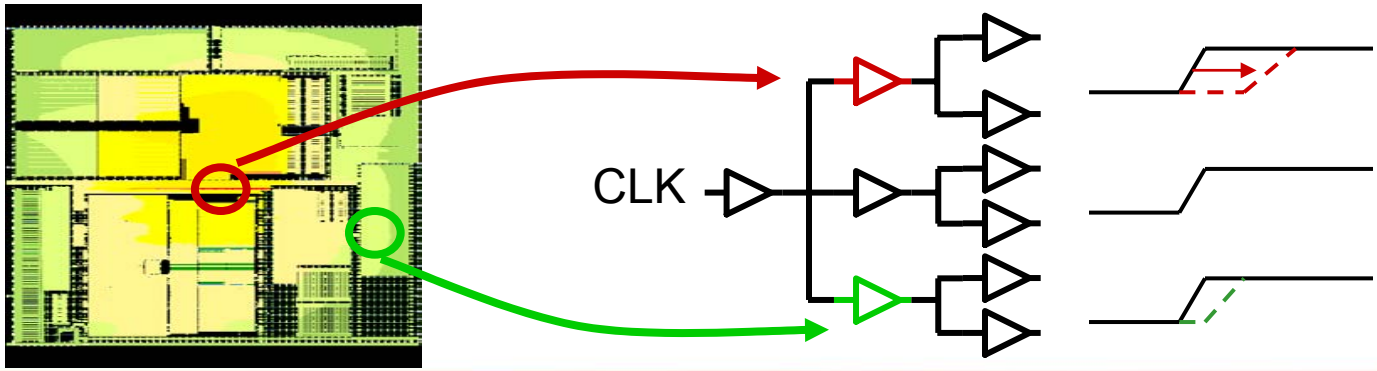
Signal Integrity and Power Supply Network Analysis of Deep SubMicron Chips

Overview of presentation

- What are the problems?
  - Power supply analysis
  - Signal Integrity analysis
  - How do these two analyses interact?
  - Design Flow and Convergence Issues
- How can design and analysis be improved?
- What new data, tools, and methodologies are required?
- Conclusions

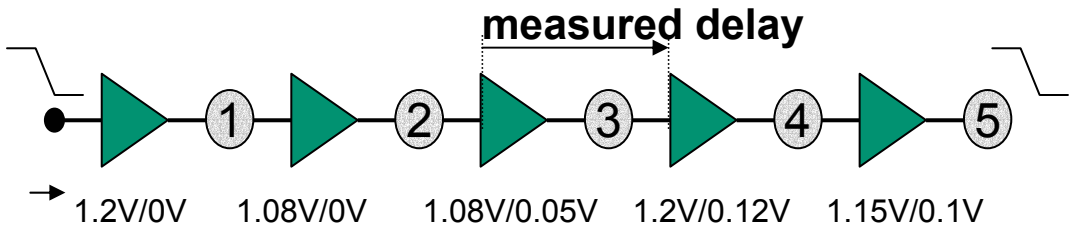
The Power Grid Problem

- IR drop
  - Describes voltage drops caused by current flowing from the power source through the resistive power network to the on-chip devices
- Ground bounce
  - Describes voltage spikes caused by current flowing from on-chip devices though the resistive ground network to the ground pins (or bumps)
- IR drop and ground bounce combine to impact silicon performance
  - Increased clock skew → hold time violations
  - Increased signal skew → setup time violations



IR Drop Impact on Path Delay
Validation to HSPICE

- Design Statistics
  - 5 element delay chain of the same buffer
  - 0.13µ process
  - 1.2V ideal VDD



CeltIC NDC Results	Delay1	Delay2	Delay3	Delay4	Delay5	Total
Ideal VDD/VSS (1.2/0V)	405ps	515ps	513ps	513ps	471ps	2.417ns
% Error	**-8.4**	**1.9**	**2.1**	**-12.3**	**-13.5**	**-7.0**
Actual VDD/VSS	440ps	523ps	497ps	594ps	541ps	2.595ns

IR Drop Impacts Timing
Causes Silicon Failure

Customer silicon failed due to hold time violation

.18µ TSMC

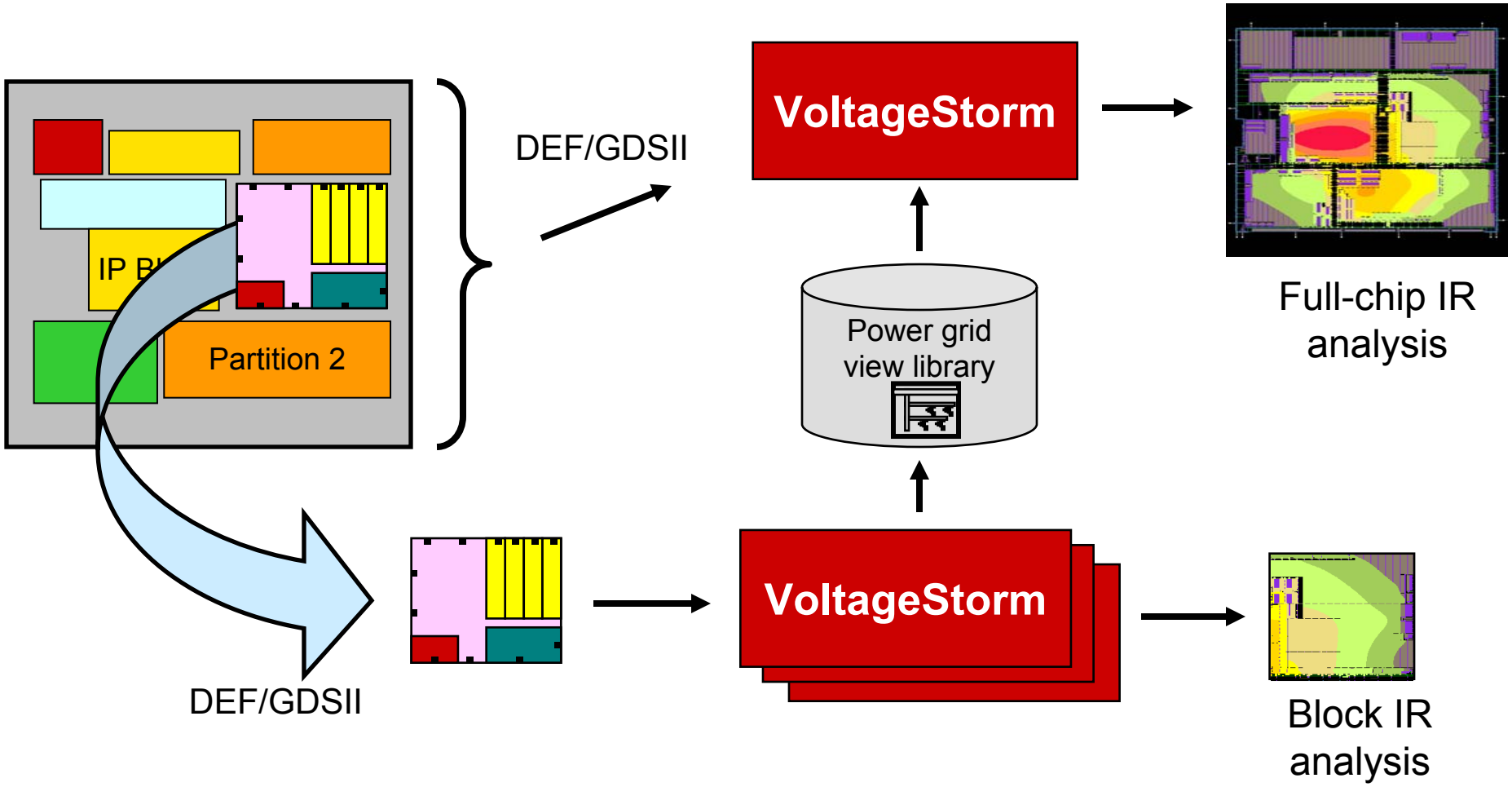
- IR drop effects on timing not analyzed
- Detailed timing + Detailed IR validated that hold time violation caused the failure

Validation	Standard Timing Ignoring IR Drop			SignalStorm + VoltageStorm Including IR Drop		
(all times in ns)	Data Available	Data Required	Slack	Data Available	Data Required	Slack
SignalStorm	3.759	3.648	0.111	3.751	3.803	**-0.052**
Pearl DC + PT STA	3.95	3.83	0.120	Feature Not Available		
HSPICE	3.808	3.66	0.148	3.811	3.83	**-0.019**

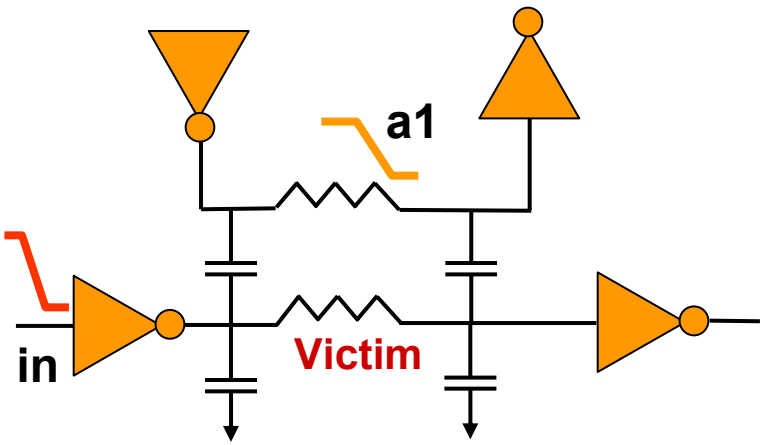
IR Drop Analysis Challenges

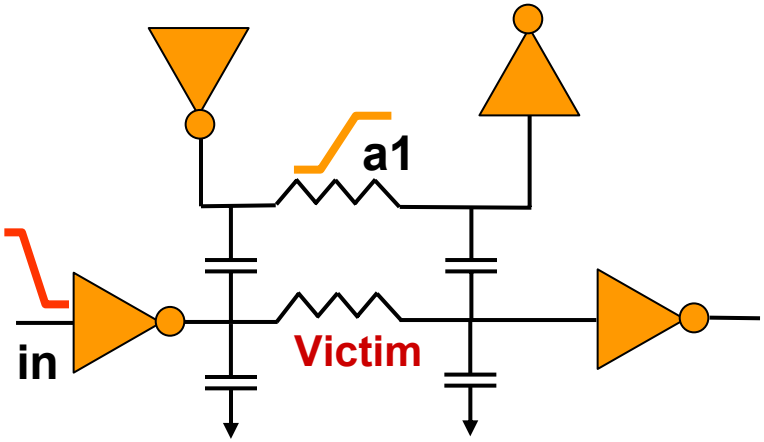
- Accurate handling of custom IP and blocks
  - Power consumption and power distribution
- Extraction for 90nm copper
- Handling large flat blocks
- Handling hierarchical designs
- Static & dynamic transistor-level power integrity analysis
  - Required for custom IP, memory
  - Required for managing power-down/up transients

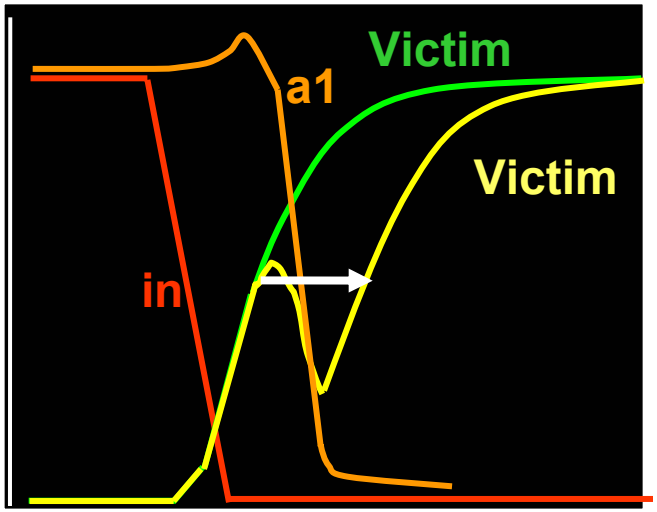
Hierarchical Power Grid Verification



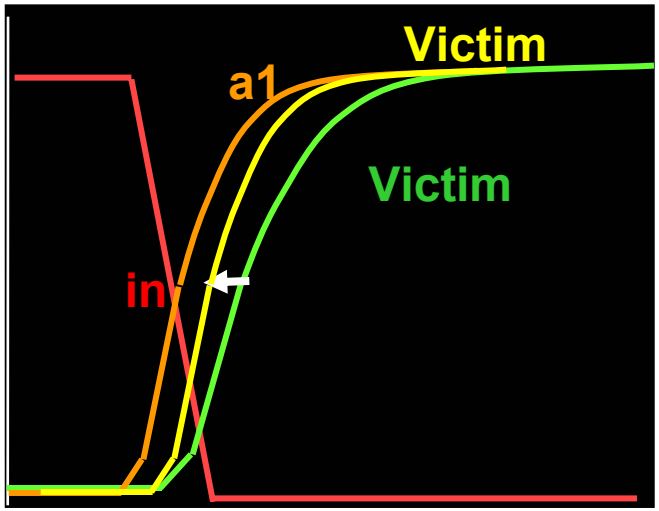
Impact of Crosstalk on Delay





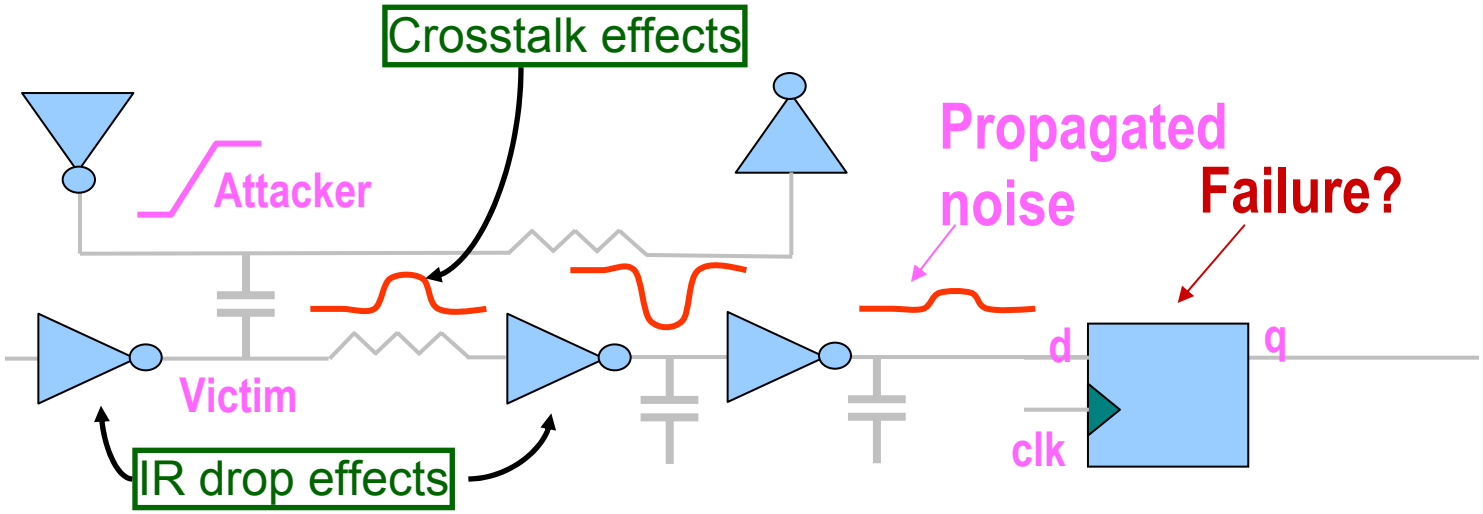


Crosstalk increases delay



Crosstalk decreases delay

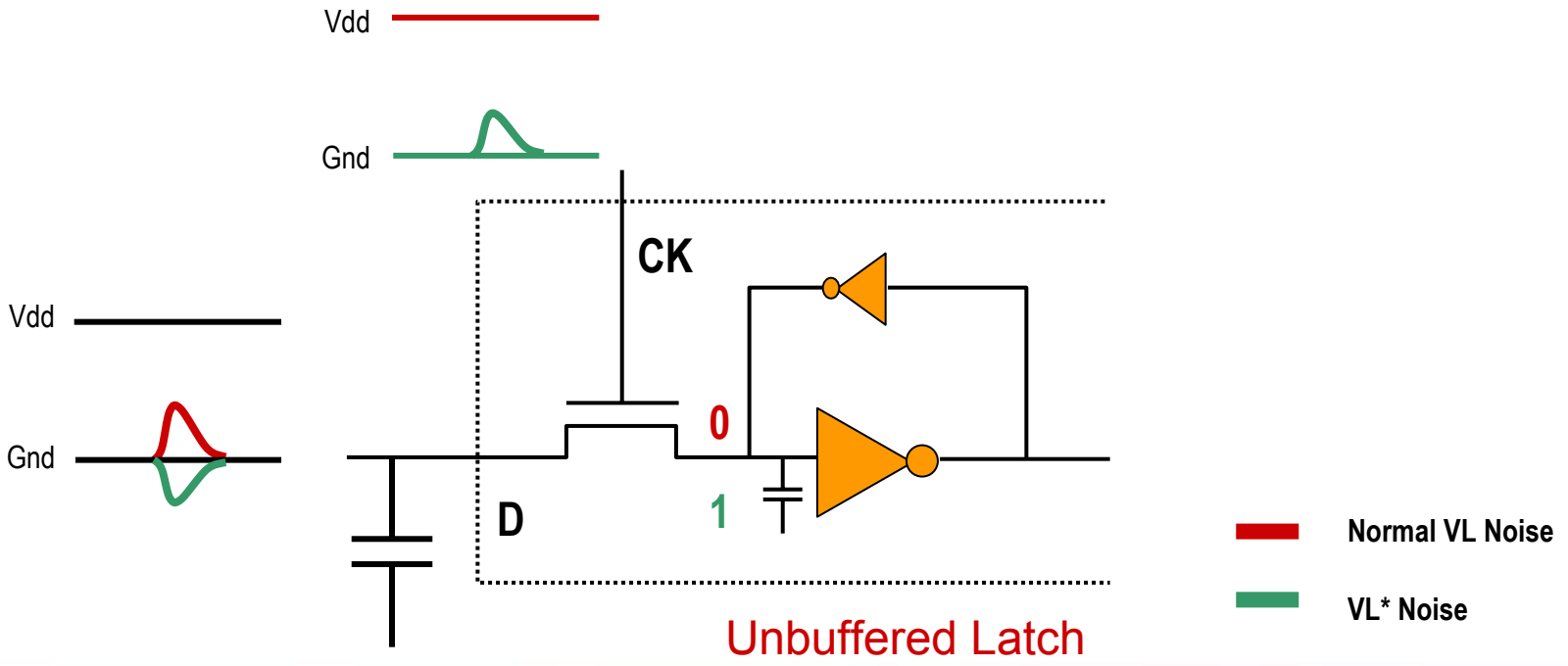
Impact of Crosstalk & IR drop on Functionality



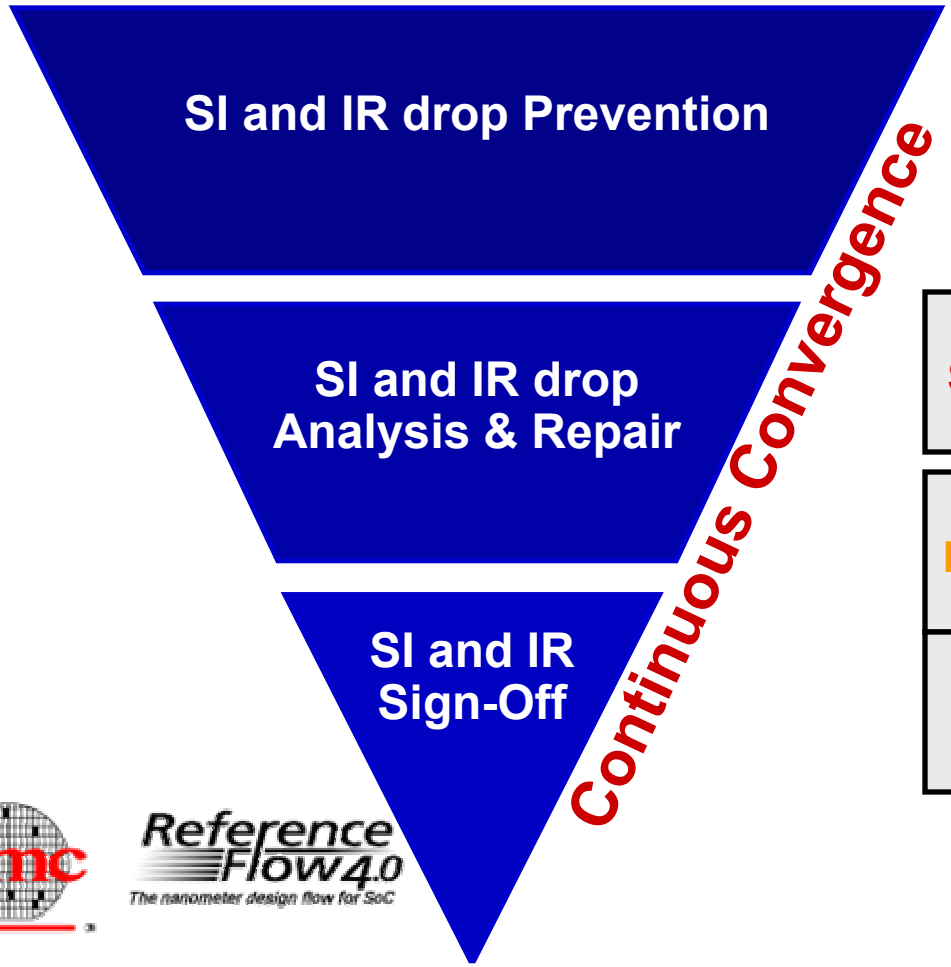
- Crosstalk glitches propagate to latches to create functional failures
- IR drop weakens victim driver, increases receiver sensitivity
- IR drop noise combines with crosstalk noise

Overshoot / Undershoot Noise Analysis - Functional Failure

- Over/Under shoot noise attacks unbuffered latches
- Causes charge sharing between long victim wire and short internal wire with weak keeper
- Causes functional failure when latch is off!



SI Closure requires attention at all times



- SI and IR problems identified and fixed throughout design implementation
- Design output is SI and timing clean

Without SI Closure	Clock speed 320Mhz 890 “glitch” violations
After Prevention Pass	Clock speed 366Mhz 25 “glitch” violations
After Repair Pass	Clock speed 400Mhz 0 “glitch” violations

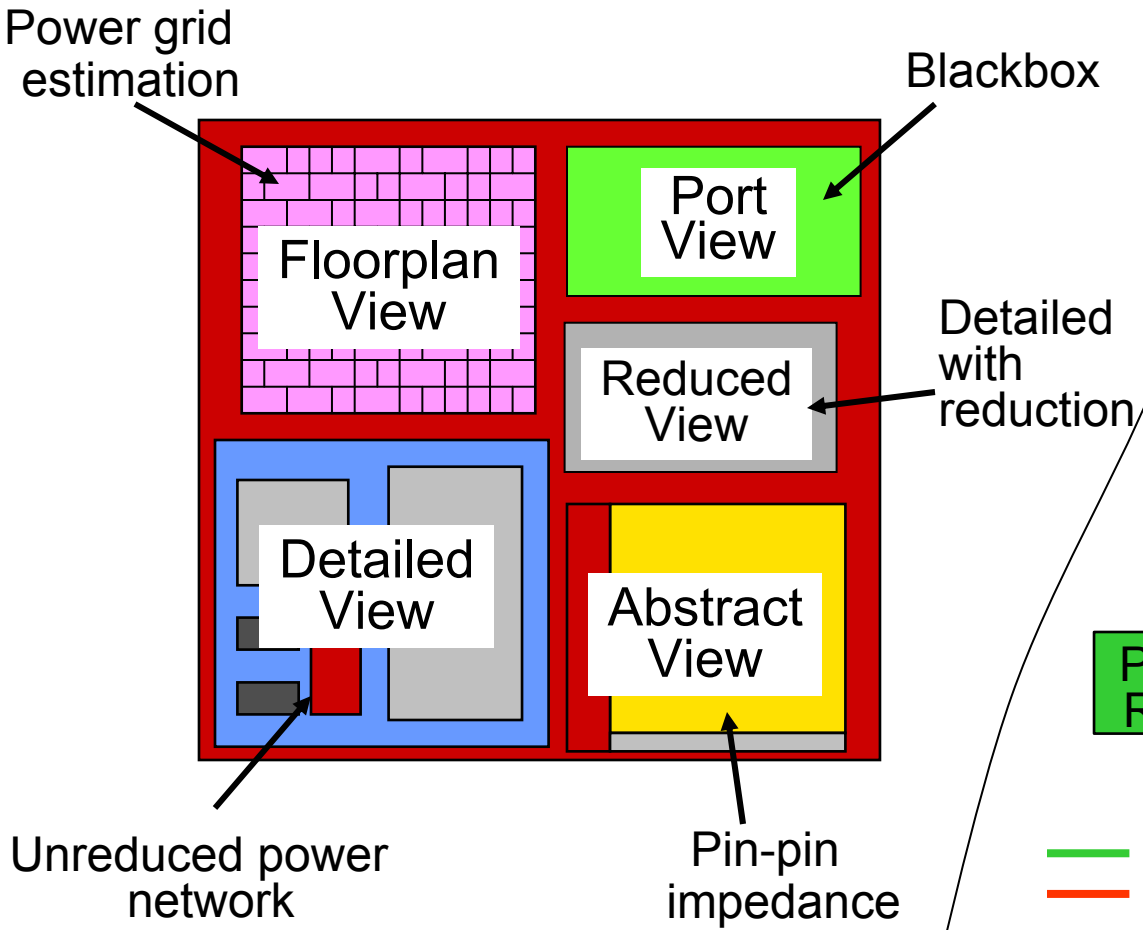
tsmc Reference Flow 4.0
The nanometer design flow for SoC

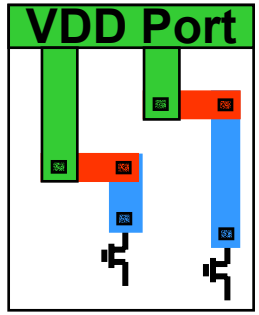
cadence

So these are the problems – what are the solutions?

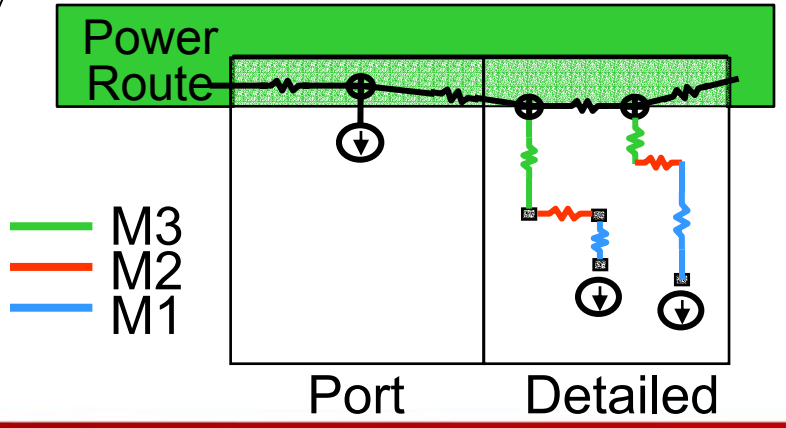
- Hierarchical analysis for IR drop and SI
- More detailed analysis for signal integrity
  - Requires new library models
- Better flows and methodology with SI and IR drop included earlier

VoltageStorm Power Grid Views (.cl)



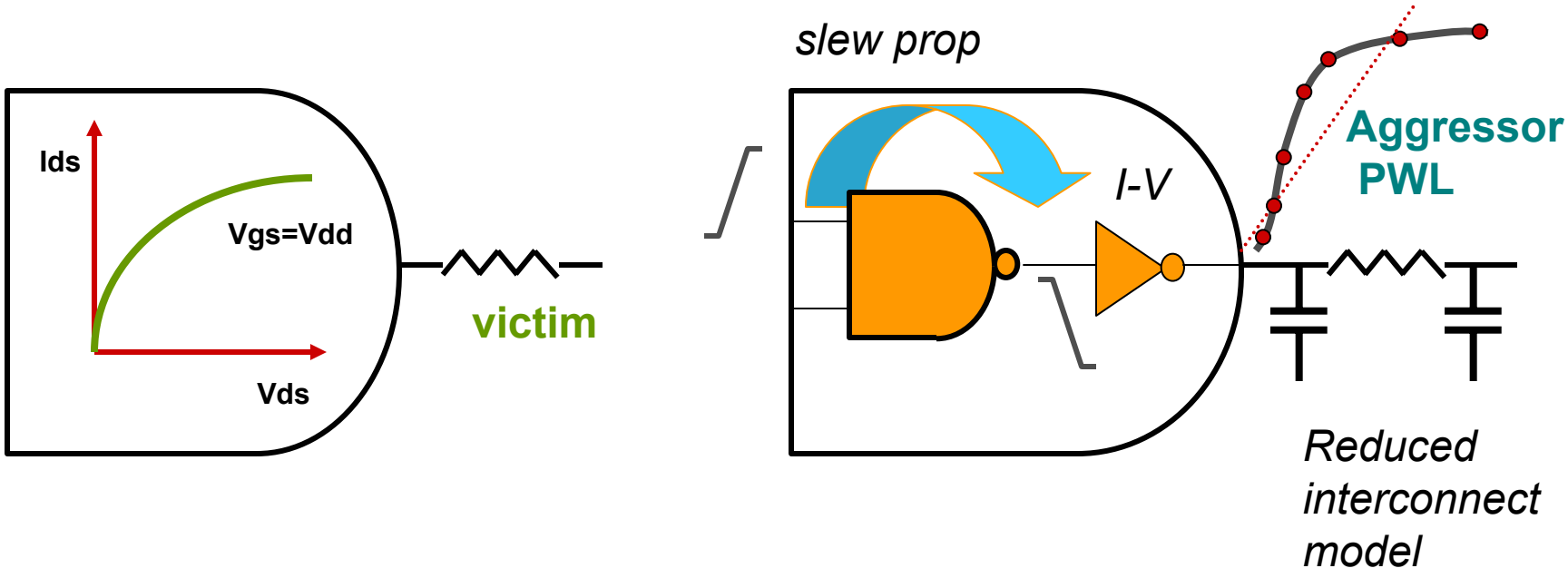


Original Cell



CeltIC Cell Based Noise Models

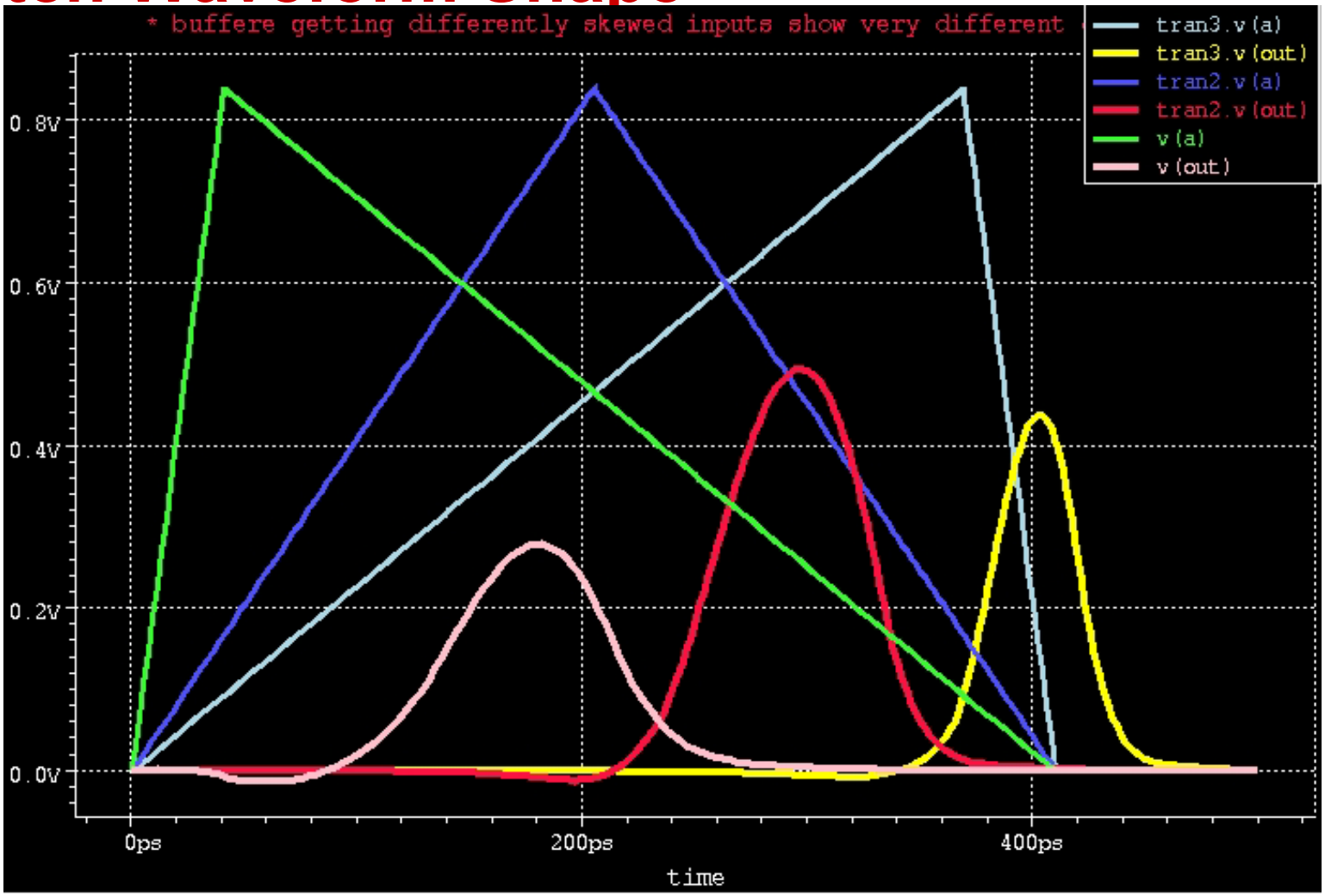
- Holding state I-V for victim driver
  - Default to transistor models in the presence of propagated noise
- Slew propagation characterization to input of aggressor's last stage
- Aggressor driving point PWL slew calculation using PI model



SI analysis is a near-analog problem

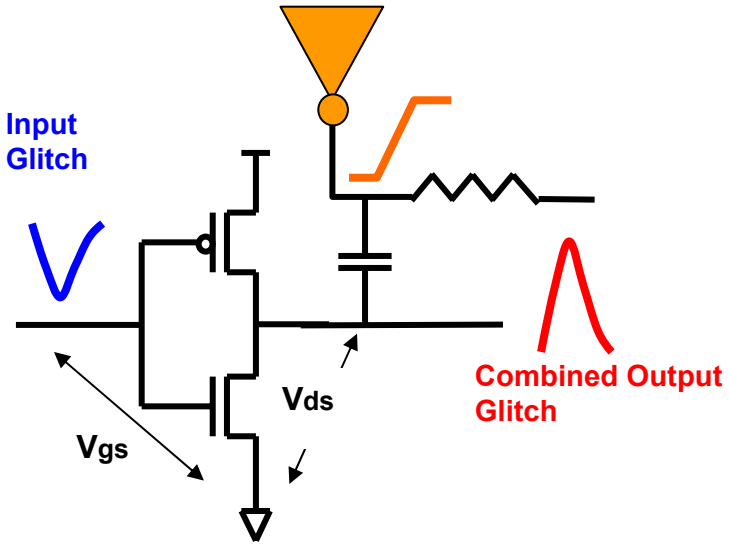
- Accurate analysis requires specialized libraries
  - Crosstalk analysis requires transistor level analysis
  - IR drop analysis requires and writes libraries
    - Input: Information on power consumption, both detailed and average
    - Output – complex block models with R and I networks
  - Timing analysis with IR drop requires more sophisticated models
- Table based libraries will not be enough!

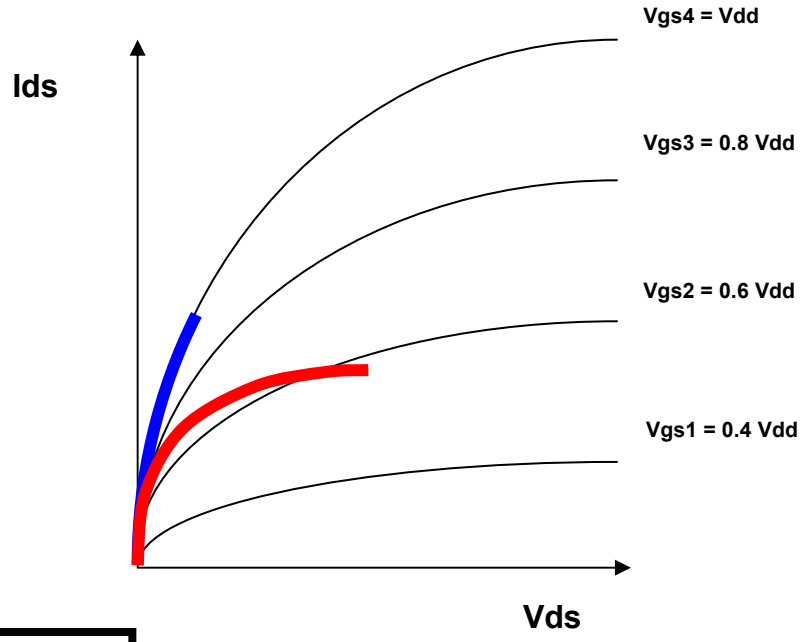
Modeling Considerations: Glitch Waveform Shape



Modeling Considerations: Driver Weakening

- Driver resistance variation due to noise induced changes in Gate and Drain voltages

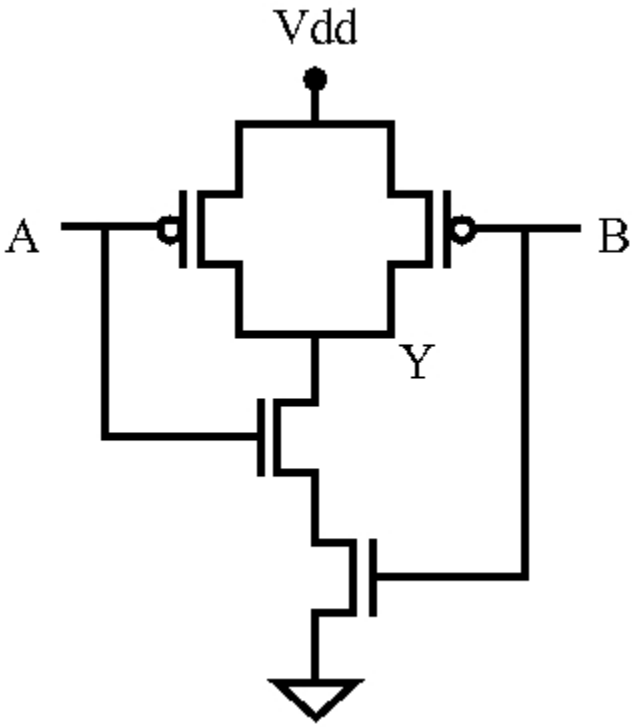




		Linear Model Glitch under estimation	
Total nets	Impacted nets	Average	Worst-Case
616K	2665	31%	342%

Modeling Considerations: Simultaneous Input Noise

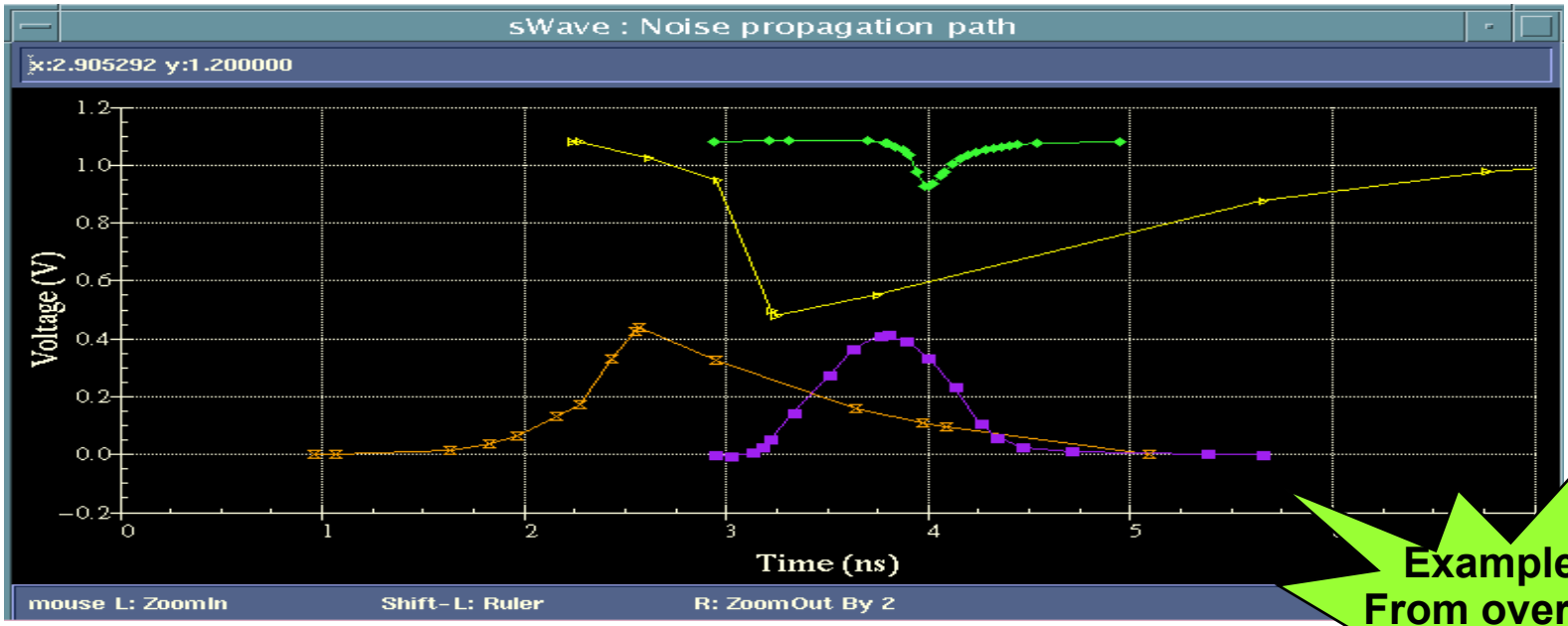
- Noise combination can be highly non-linear
- Simple summation leads to both optimistic and pessimistic results

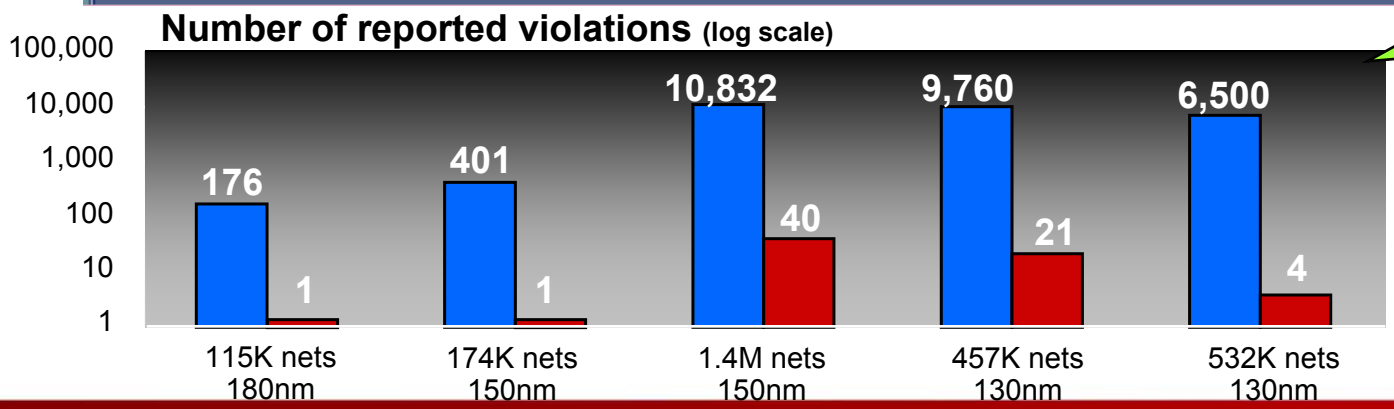


Input Glitch	A->Y	B->Y	Linear Sum	Actual
VH (mV)	95	184	279 (-70%)	943
VL (mV)	175	105	280 (+60%)	175

Crosstalk Glitch Analysis

- Glitches propagated to registers to filter false failures
  - Uses simulation of piecewise linear waveform (not triangle table-lookup based)



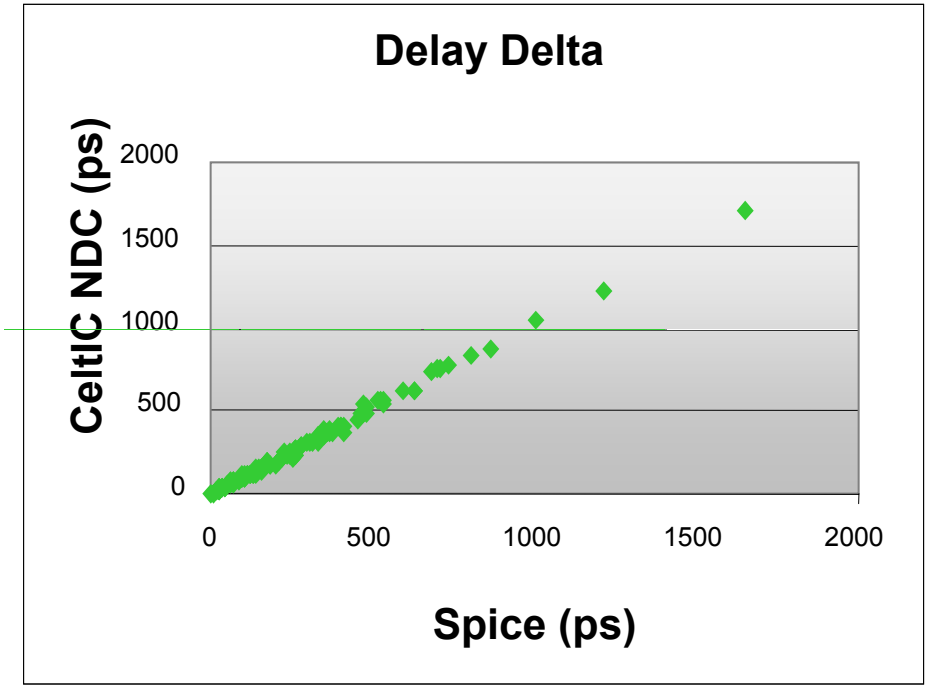


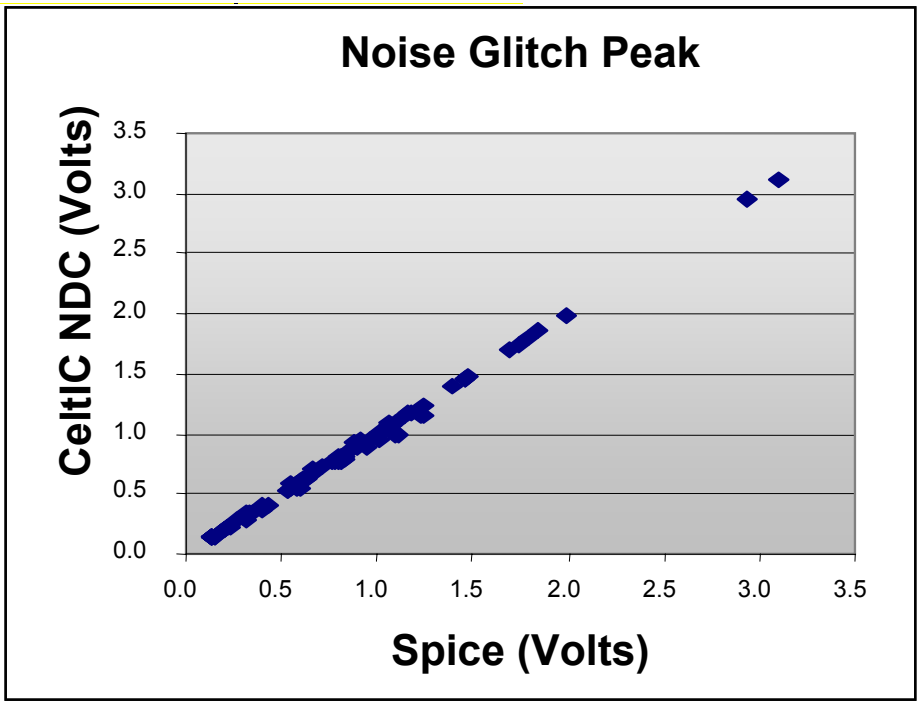
Examples From over 350 chips analyzed

Peak > 30% Vdd

More detailed (analog) analysis

Accurate Noise analysis is possible, and very helpful





Data from numerous customer 130nm benchmarks

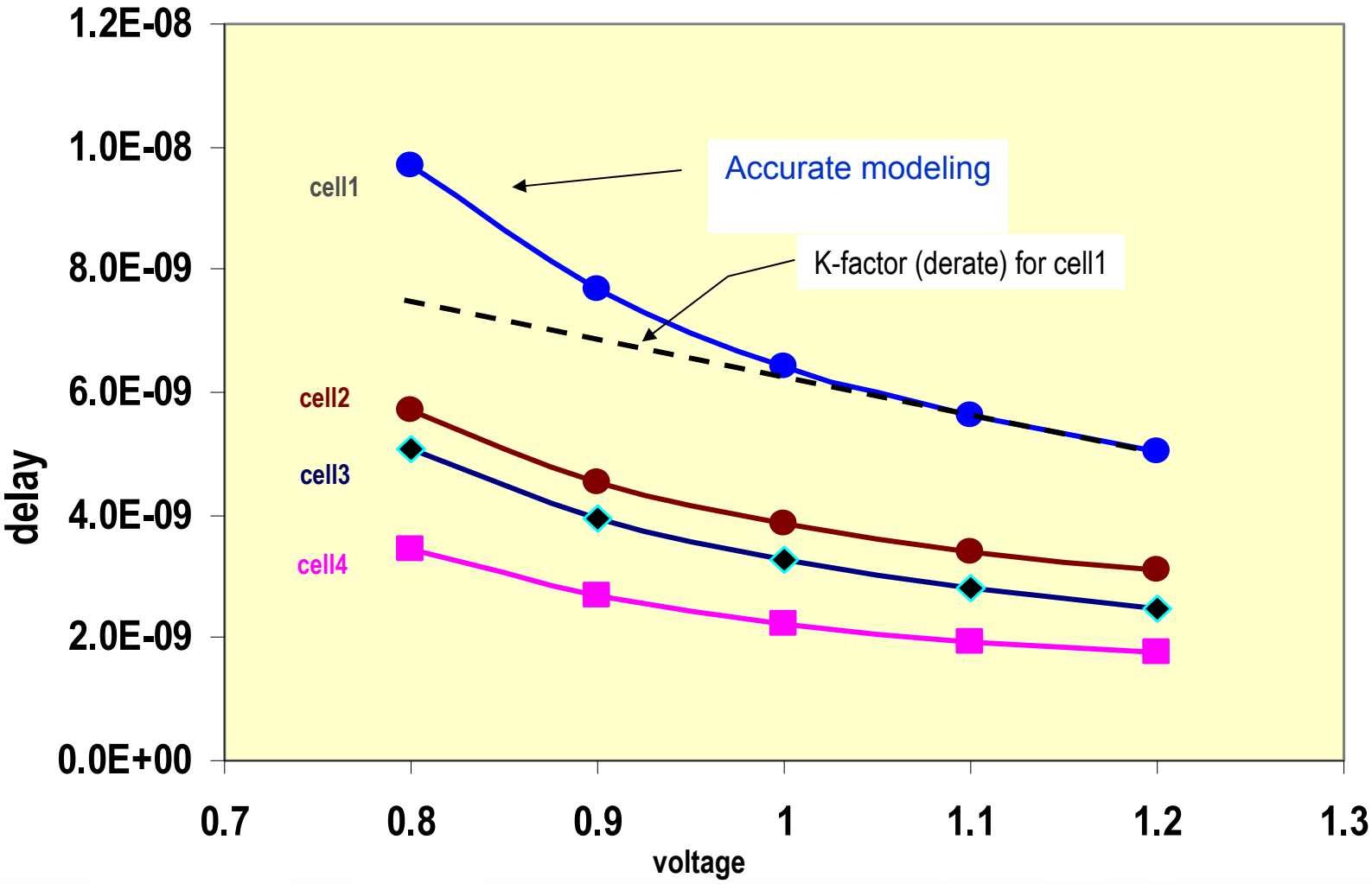
Average Vs SPICE

Delay Delta:	4.6%
Noise Glitch:	2.6%

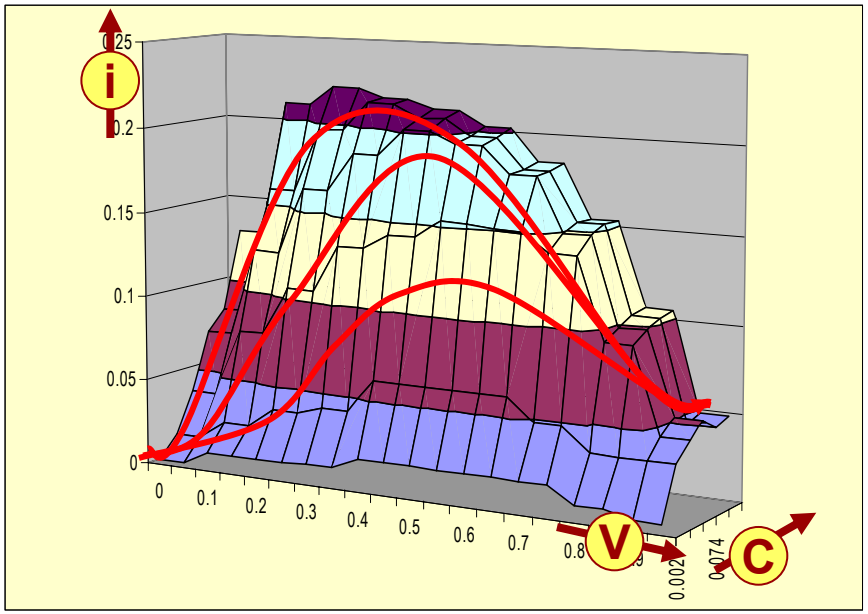
Accuracy due to advanced victim/aggressor alignment algorithms and on-the-fly fast transistor level simulation

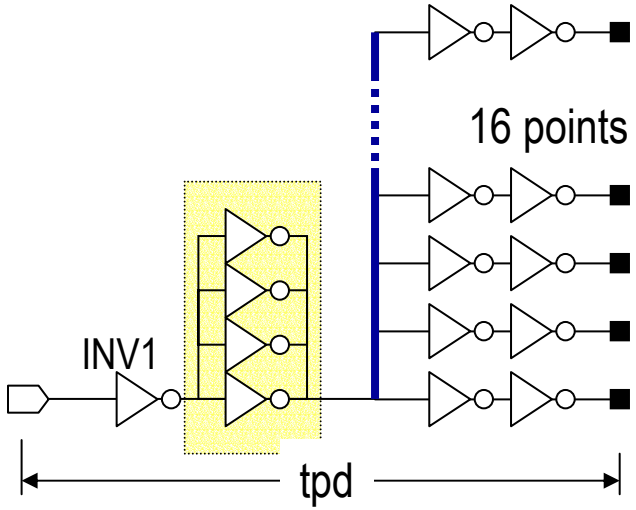
Problem – change in delay with IR is not linear

IR Delay Calculation

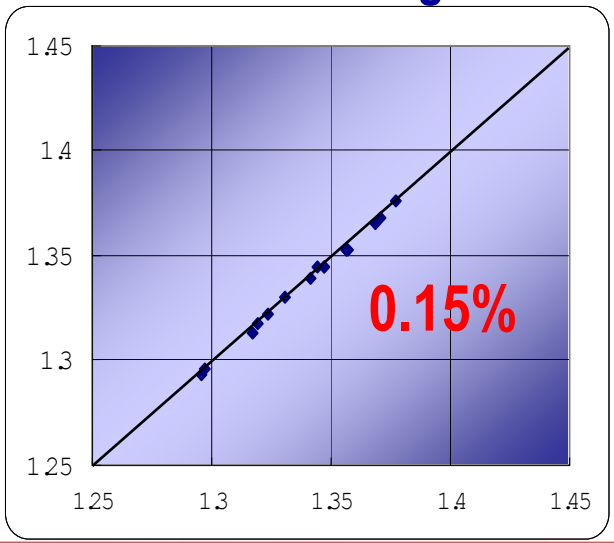


SignalStorm: ECSM Delay Modeling





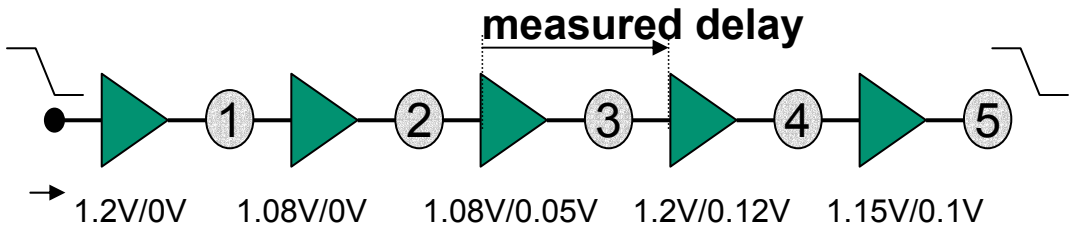
HSPICE SignalStorm



- ECSM™: effective current source model
  - Nonlinear current source fitting
  - Input slew & output load dependence
  - Excels at multiple driver cells, clock meshes, long interconnects, modeling IR drop effects

IR Drop Impact on Path Delay
Validation to HSPICE

- Design Statistics
  - 5 element delay chain of the same buffer
  - 0.13µ process
  - 1.2V ideal VDD



CeltIC NDC Results	Delay1	Delay2	Delay3	Delay4	Delay5	Total
Ideal VDD/VSS (1.2/0V)	405ps	515ps	513ps	513ps	471ps	2.417ns
% Error to Spice	**-8.4**	**1.9**	**2.1**	**-12.3**	**-13.5**	**-7.0**
Actual VDD/VSS	440ps	523ps	497ps	594ps	541ps	2.595ns
%Error, ECSM model	**-0.5**	**-0.4**	**-1.1**	**1.6**	**-0.6**	**-0.15**

Note: ALL Spice results were measured with actual VDD/VSS

Validated Signal Integrity Library Views

Noise Library

- Accurate crosstalk analysis (delay and glitch)

Power Library

- Accurate IR drop and electromigration analysis

Timing Library

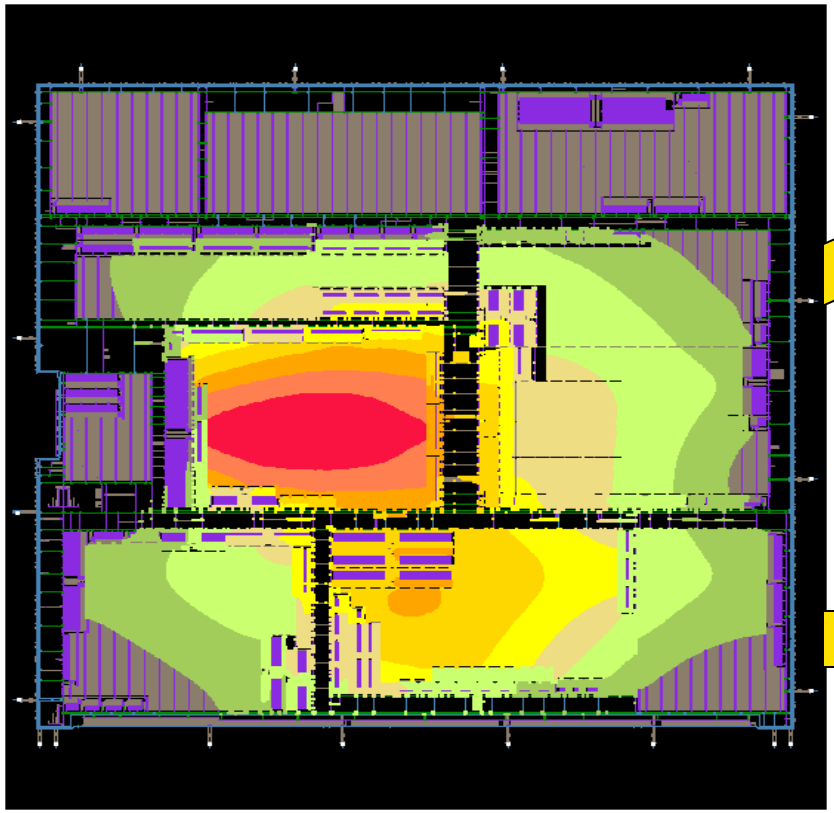
- Accurate delay modeling including IR drop effects

Improved Flow Support for Convergence

- Need to see problems as early as possible
  - In particular, IR problems are almost impossible to fix without more resources
  - Must be seen and fixed during silicon prototyping
- Need prevention, analysis, prevention throughout the flow
- New unifications of tools required

IR Drop analysis during early prototyping

SoC Encounter



Block-level analysis

Encounter power analysis

Block power consumption

VoltageStorm

Block Power grid view

CELL PGV

Power grid view library

Top-level analysis

Encounter power analysis

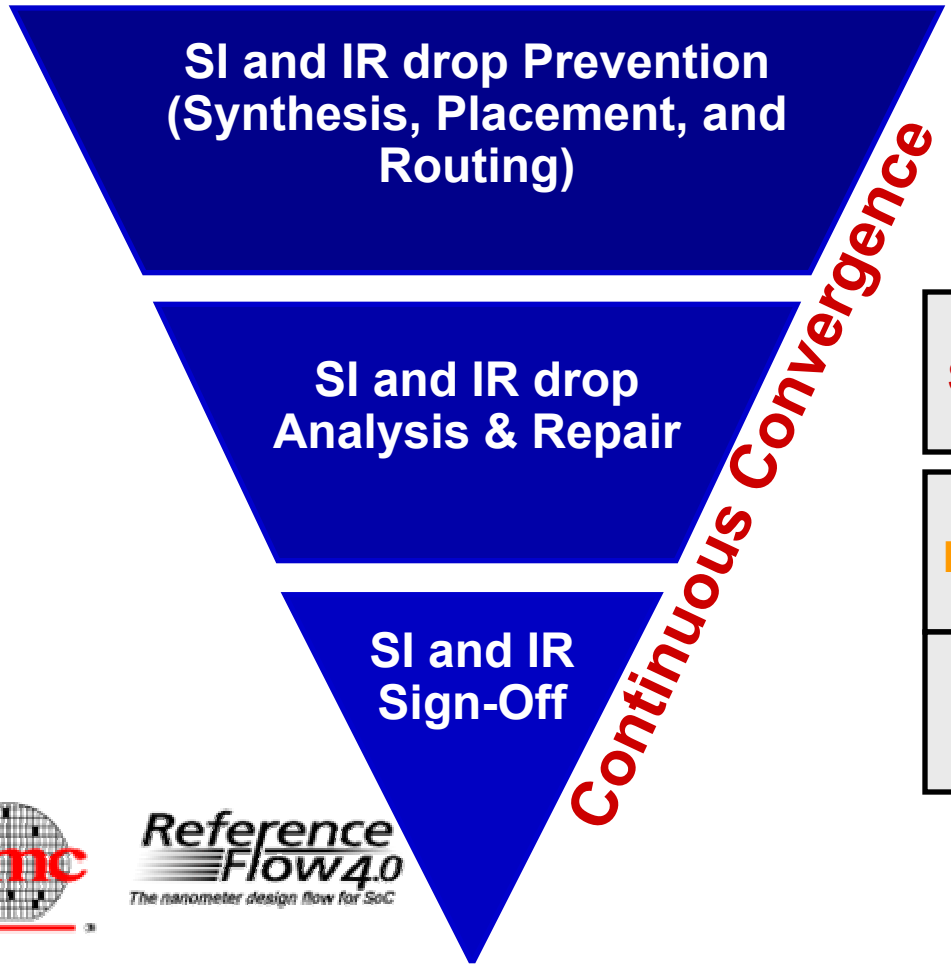
Instance power consumption

VoltageStorm

BLOCK PGV

Results displayed in SoC Encounter interface

SI Closure



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- Design output is SI and timing clean

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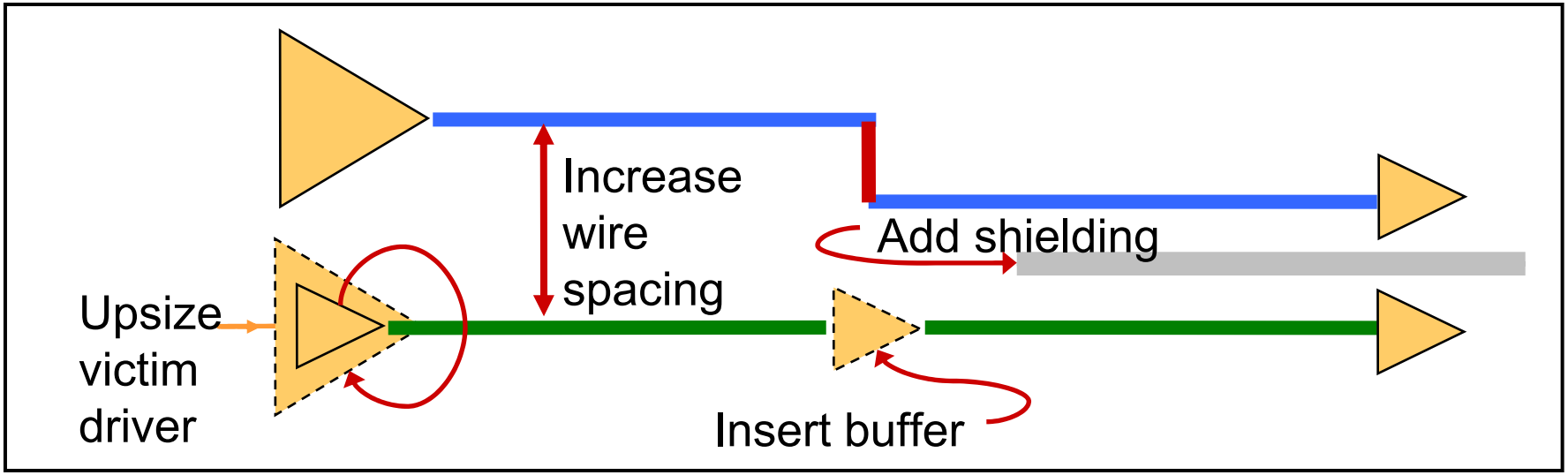
Reference Flow 4.0
The nanometer design flow for SoC

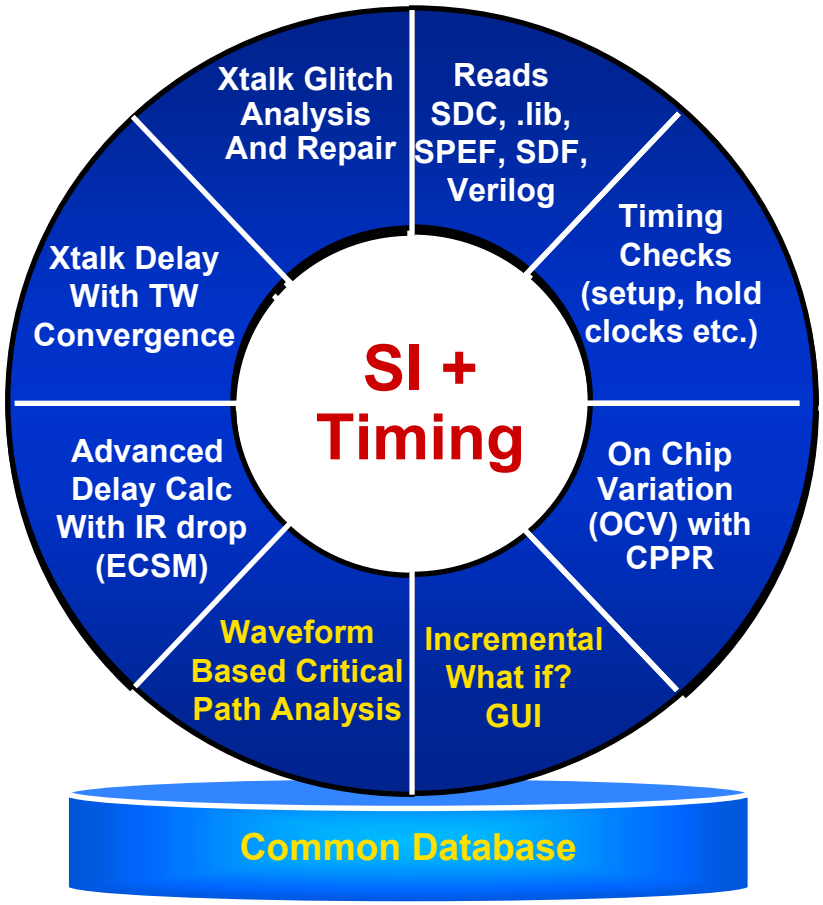
cadence

SI Repair Techniques for Crosstalk Glitch and Delay



- Minimizes disturbance to existing P&R
- On-the-fly incremental analysis of design changes
  - Both timing and glitch
- Automatic routing repair for rapid design closure
  - Spacing, layer, topology control

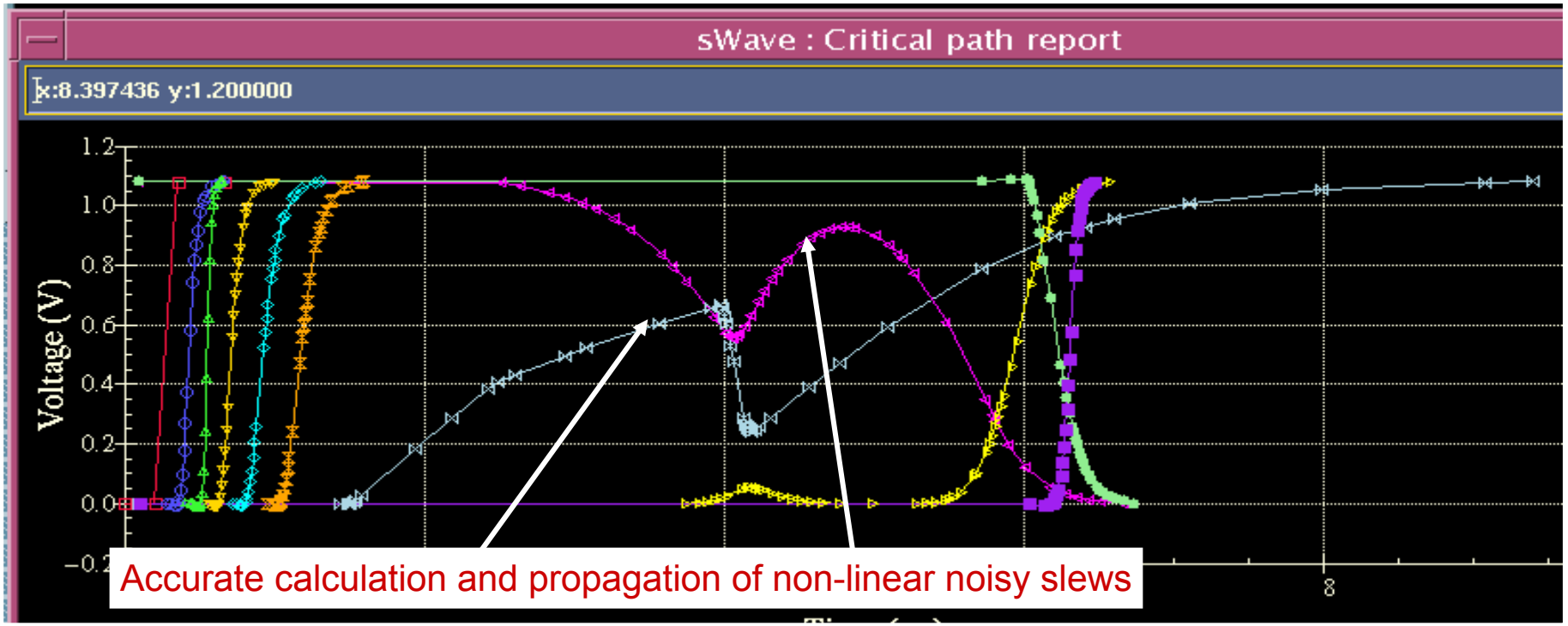
Integrated timing and SI analysis

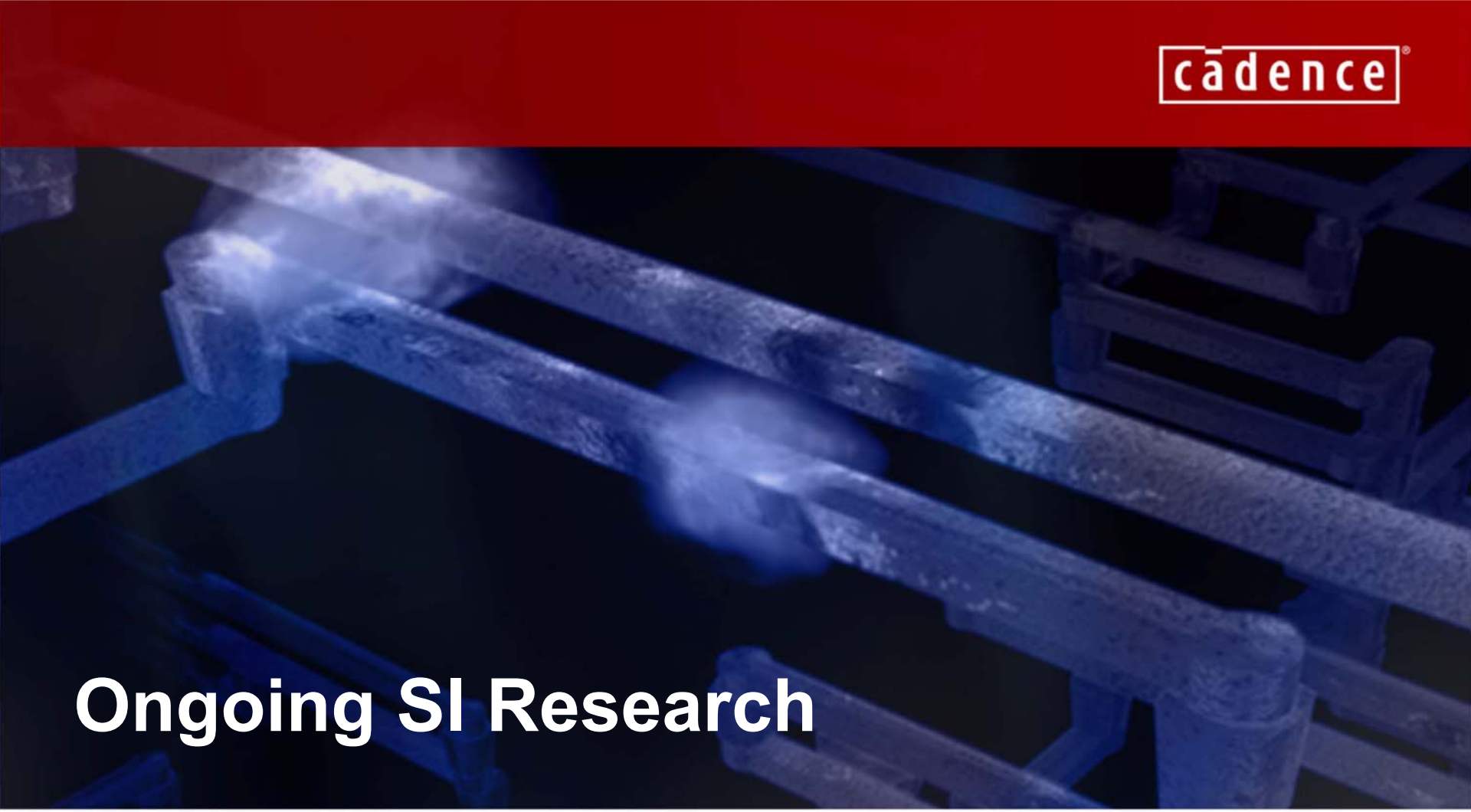


- Include conventional cell level STA with standard interfaces (sdc, .lib, verilog, spef, etc.)
- Includes advanced xtalk analysis
  - 10-100X less false glitch failures
  - Reduced xtalk delay pessimism
- Timing Window Convergence is internal
- Can use SI techniques to increase timing accuracy

Waveform Based Critical Path Analysis

- Built-in path simulation of any path
  - Must be simple to use (not all designers are comfortable with analog)
  - Includes Xtalk, IR drop effects
  - Must be fast and support incremental what if?

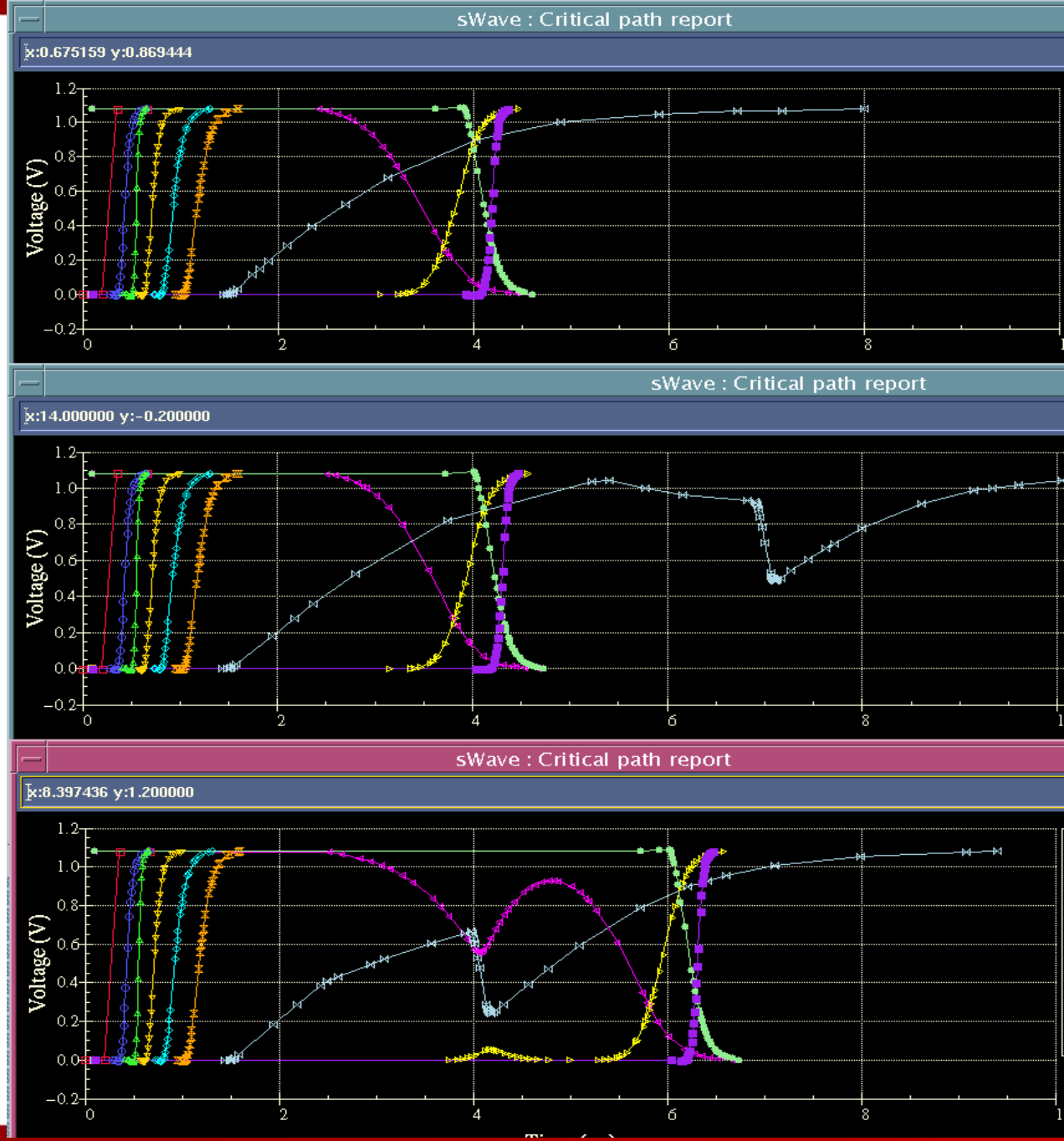




Ongoing SI Research

Path based Aggressor Alignment

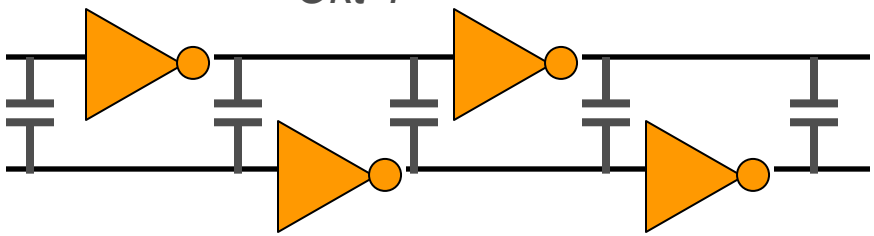
- Path delay without noise = 4ns
- Path delay with net-based alignment = 8.5ns
- Path delay with path-based alignment = 6ns
- Pessimism reduction = 2.5ns!



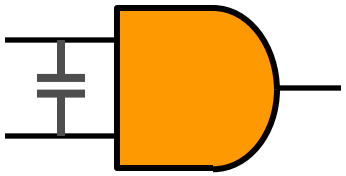
SI Timing and Logic Satisfiability

- False coupling exists in circuit topologies
- “Temporal functional Crosstalk Noise Analysis”, DAC 2003

Ckt 1



Ckt 2



	Spice sweep (ps)	Worst case (ps)	SAT analysis (ps)
Ckt 1	1235	1869 (+51%)	1250 (+1%)
Ckt 2	594	1038 (+75%)	607 (+2%)

Summary

- Electrical verification is significant problem for Nanometer designs
  - IR drop analysis
  - Signal Integrity analysis
  - Key market windows being missed due to chip failures from these
- To solve this, we need
  - Accurate analysis tools, both hierarchical and flat
  - Better libraries
  - Incorporate IR and SI into flows (prevention, repair, tool integration)
- Problems can be solved, but require attention to detail
  - If someone claims to have a solution, ask LOTS of questions!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