Signal Integrity

Lecture 22

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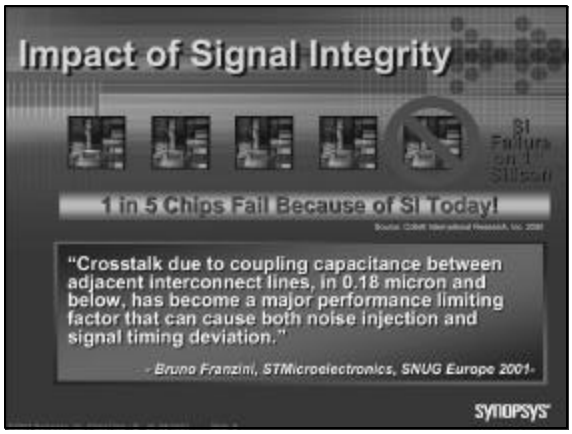
Introduction

- Signal Integrity includes all IC design effects that cause the design to malfunction due to the distortion of the signal waveform:
  - Crosstalk (for delay and noise)
  - Power/Ground (P/G) integrity
    - IR-drop
    - Ldi/dt noise
    - LC resonances
  - Substrate coupling
  - Simultaneous switching noise

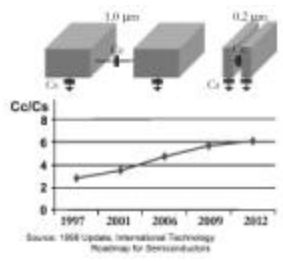
Outline

- Crosstalk ⇐
- Power/Ground (P/G) integrity
  - IR-drop
  - Ldi/dt noise
  - LC resonances
- Substrate coupling
- Simultaneous switching noise



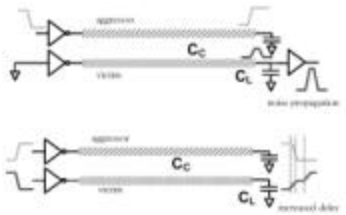
Reminder on parasitics

Coupling capacitance dominates interlayer capacitance



Crosstalk

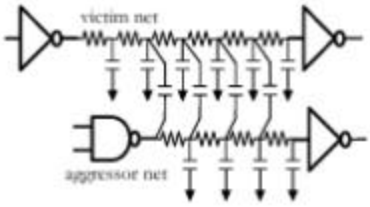
- Due to the coupling capacitance between interconnections, a signal switching on a net (aggressor) may affect the voltage waveform on a neighboring net (victim)



Noise Propagation

Increased Delay

Circuit Model for Crosstalk



Crosstalk Simulation

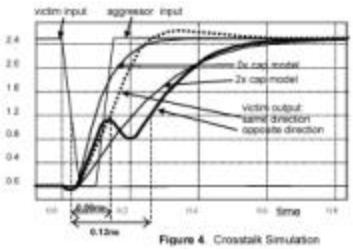
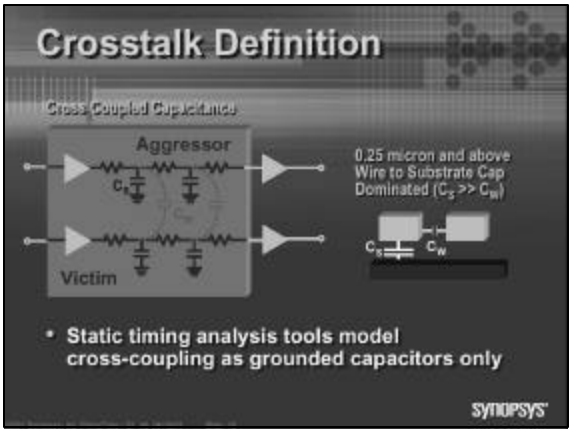
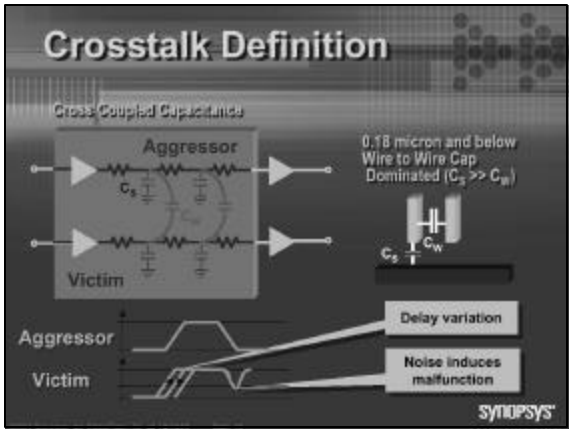


Figure 4 Crosstalk Simulation

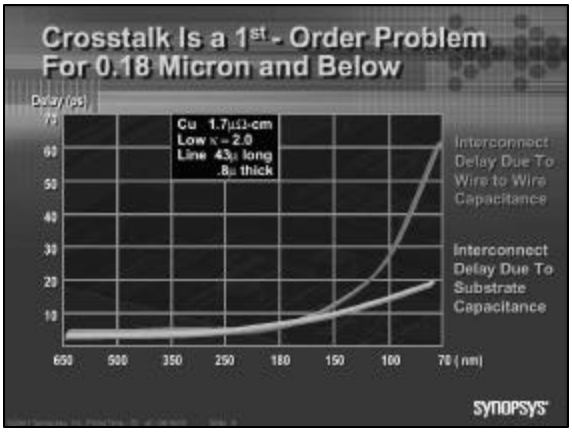
Crosstalk Definition



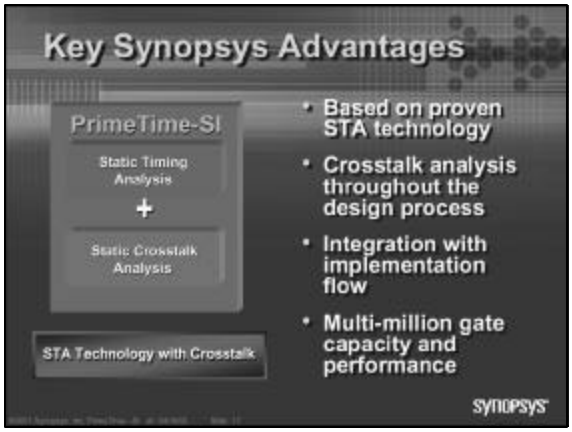
Crosstalk Definition



Crosstalk Is a 1st - Order Problem For 0.18 Micron and Below

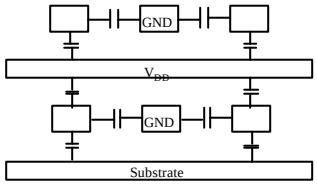


Key Synopsys Advantages



Design for Crosstalk

- It can be both capacitive and inductive
  - Capacitive is dominant at current switching speeds
- To reduce it:
  - Use of shielding layer (inter-layer)
  - Use of shielding wire (intra-layer)



Outline

- Crosstalk
- Power/Ground (P/G) integrity ⇐
  - IR-drop
  - Ldi/dt noise
  - LC resonances
- Substrate coupling
- Simultaneous switching noise

P/G Integrity

- Technology scaling imposes requirements on the reduction of power supply voltage
- Power/Ground integrity becomes a serious challenge during design
  - 10% supply voltage fluctuations may translate in more than 10% timing inaccuracy
  - Or even cause circuit to fail

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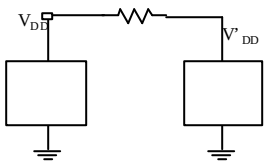
What is IR-drop?

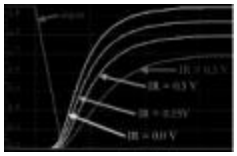
- Increased resistance affects circuit operation:
  - Increased propagation delay
  - Resistive voltage drop (IR-drop)

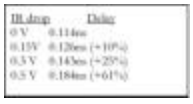
⇒ Especially for Power Distribution Network



What is IR-drop?

- IR-drop: voltage drop of the power and ground due to current flowing in the power/ground resistive network





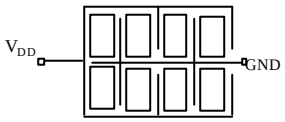
IR-drop simulations

Voltage supply

Signal Waveform

Power Distribution Network

- Most obvious solution: reduce max distance between supply pins and circuit supply connections
  - Finger-shaped power distribution network



IR-drop consequences

- Design and layout of power distribution network must be done early in the design process (then gradually refined)
- Design of the power network requires knoledge of the peak current (as opposed to power dissipation that relates to average current) ⇒ Reliability
- Delay is increased
- Noise Margins are reduced
- Technology scaling worsen the problem

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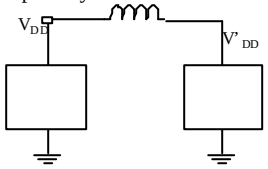
What is Ldi/dt noise?

- Increased inductance affects circuit operation:
  - Delay behaves as transmission lines
  - Inductive coupling crosstalk
  - Inductive voltage drop (also called Delta-I noise)
  - It is a high-frequency phenomenon

⇒ Especially for Power Distribution Network



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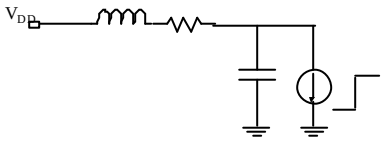
What are LC resonances ?

- May impact the circuit also at low frequencies
- May not be localized (resonance waves may travel through the whole chip)



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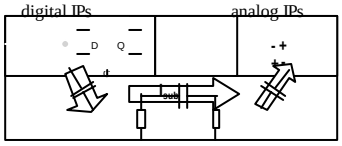
Substrate Coupling

- Substrate is not equipotential
  - It has a (resitive) model
- There are substrate voltage variations that couples to blocks sharing the same substrate



Common Substrate

Outline

- Crosstalk
- Power/Ground (P/G) integrity
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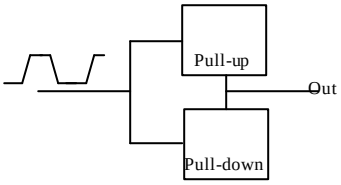
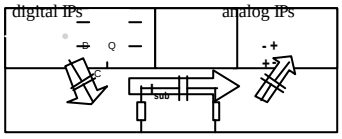
Simultaneous Switching Noise (SSN)



- Strong dependence on input-pattern
- Injection even when output is not switching

The Substrate Coupling Problem on Mixed-Signal Systems

- IPs can be safely re-used in mixed-signal system-on-a-chip designs only if they do not affect other critical components
- Digital components may inject considerable amount of **current noise** into analog components via the common substrate



Common Substrate

The Substrate Coupling Mechanisms: Need for Current Spectrum Estimation

Why substrate currents?

- Substrate potentials **may affect analog signals:**
  - though direct capacitive coupling
  - through variation of Vt (body effect)
- Digital IPs **inject current noise into the substrate** at clock frequency and its harmonics because of switching activity
- Substrate currents can easily reach analog IPs and change substrate potentials

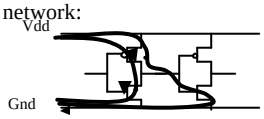
Why frequency domain?

- Analog circuits are particularly sensitive in their frequency band of operation

Need estimation of the maximum current injected by digital components for each harmonic of their clocks for safe operation!

The Timing Problem

- Digital components inject significant currents also into the power supply network:
  - **load charging currents**
  - **short circuit currents**

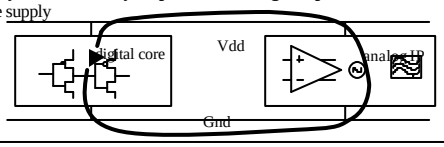


- IR drops may cause voltage variations and, consequently, **delay variations** within digital blocks.

Need estimation of the instantaneous maximum current injected for delay analysis

The Signal Integrity Problem on the Power Supply Network

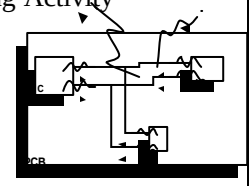
- Trend toward lower resistivity materials, e.g., copper ⇒ supply network becomes inductive and current noise may give **signal integrity** problems as in packages and PCBs:
  - Resonance with decoupling capacitors
  - Wavelength-related resonance (as frequency increases)
- Supply noise can easily **couple to the analog components** that share the same supply



Need estimation of the maximum current at each frequency of the clock harmonics for signal integrity and supply coupling

Electromagnetic Interference Problem due to Digital Switching Activity

- High frequency currents created by digital ICs supply network can leak out to the package and PCB producing **electromagnetic interference emissions at the harmonics of the clock**



Need estimation of maximum current at each frequency of the clock harmonics for EMI analysis

Estimation Techniques

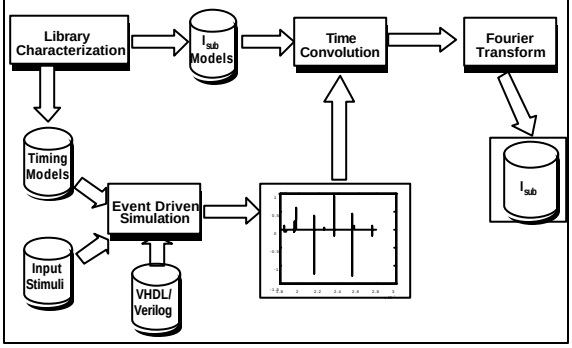
PROBLEMS	REQUIREMENTS
• Substrate coupling	max substrate current at each harmonic
• Timing	max supply current instantaneous in time
• Power consumption	average supply current over many periods in time
• Supply coupling	max supply current at each harmonic
• EMI	max supply current at each harmonic

Some Approaches for Noise Current Estimation

- Vast literature on supply current estimation for power consumption: mainly concerned with average current in time [Najim TransVLSI94]
  - Most are based on switching activity estimation with propagation of probability distributions
- Some algorithms exist for maximum current envelope estimation instantaneously in time [Bobba ISPD98]. Mainly for timing problems, not suitable for substrate coupling, signal integrity and EMI.
- Stochastic approach for current estimation in the frequency domain
  - [Demir ICCAD99]: combines the approach from power analysis based on propagation of switching activity probabilities, with an estimation of frequency spectrum for substrate or signal integrity problems
  - [Charbon TransCAD99]
- Missing an approach for current upper bound estimation in the frequency domain

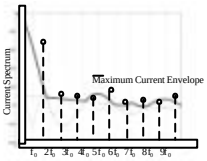
SubWave: Stochastic Noise Characterization

(Charbon, Miliozzi, Carloni, Ferrari, ASV – UCB)



Input Pattern Independent Noise Current Spectrum Upper Bound

(Nardi, Daniel, ASV – UCB)



- Note: can use same algorithm for both substrate injection and gnd/V_{DD} injection estimation
- Applications:
  - noise coupling throughgnd/ V_{DD} system or substrate on mixed-signal circuits
  - Electromagnetic interference

Summary on Signal Integrity

- Crosstalk
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  - IR-drop
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