Development and Validation of an Electromagnetic Distributed Power Grid Model for the 90nm Pentium® 4 Processor

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Abstract

In this paper, we show that it is necessary to include the distributed effects of the power grid to accurately model the power supply noise for high frequency microprocessors. We show that high frequency resonances can be entirely missed if such effects are not modeled. Finally we prove the theory with experimental validation on the 90 nm Pentium® 4 microprocessor.

Introduction

Circuit theory, as the low frequency part of Maxwell's theory, has guided VLSI design and analysis for more than three decades. During the last decade, and in the microwave regime, different approximations of Maxwell's equations have been used to describe the wave propagation effects on delay and signal integrity [1-2] in the analysis of interconnects. Recently it was shown that an electromagnetic model capturing the full-wave effects is necessary to capture the correct behavior of interconnects in the multi-GHz region [3]. In general, the wave effects on interconnects can be ignored as long as their physical dimensions remains very small compared to the wavelength the clock frequency. Typically, an interconnect structure smaller than $1/100^{th}$ of the clock wavelength can be treated as a lumped element. Evolving into the third decade, the clock frequency of microprocessors enters the gigahertz regime and is heading towards 10 GHz. At these frequencies, the global power grid is electrically large and the wave propagation effects can not be ignored. A time domain solution to Maxwell's equations treating the power grid as an electromagnetic structure is the most accurate, and most cumbersome. The complexity of such a solution is largely the reason why electromagnetic analysis tools have not made it to mainstream chip design tools and verification. In this paper we show why it is necessary to model the power grid as an electromagnetic structure and we propose a simple approach of incorporating these effects with circuit simulations. We will show that the proposed model can predict high frequency noise on the power supply much more accurately than the existing models in the literature. Such accuracy is needed to predict the circuit performance.

The Power Grid Distributed Model

Figure 1, below shows a typical power delivery model. This model is largely used by the industry. The electrical parameters of Figure 1 are defined as:

Lreg / Rreg: Voltage Regulator inductance / resistance
Cbulk: Bulk capacitance used by the voltage regulator
Rbulk / Lbulk: Series resistance / inductance of Cbulk
Lmb / Rmb: Motherboard inductance / resistance
Cmb: Medium range motherboard capacitance
Lcmb/Rcmb: Series inductance / resistance of Cmb
Cpa/ Lpa /Rpa: Package capacitance/ inductance/ resistance
Lcpa / Rcpa: Series inductance / resistance of Cpa
Cdie: on die decoupling
Rdie / Ldie: Series resistance / inductance of Cdie

Thus far, most of the literature has adopted this model or some minor variations of it [4-8]. More details can be found in [4]. As shown in [4], this model has been adequate for the analysis of power supply noise in the range of 0 to 200 MHz. It has been shown [4] that such model results in a noise spectrum composed of 3 distinct and non overlapping frequency regions. A [50 MHz - 200 MHz] band that is a function of the package inductance and package capacitance, a [1 – 10 MHz] band that is a function of the package capacitance and socket inductance, and a [0-100 KHz] range that is a function of the mother board capacitance the regulator inductance. The relation between these different types of droop and the circuit performance has been extensively treated in [4]. As can be seen in figure 1, this model treats the power grid of the microprocessor as a lumped impedance (Cdie, Ldie) with zero physical dimensions. The stimulus is also modeled as a single di/dt source.

In this paper we modeled the power grid as a distributed model. First we discretized the metal structure into a 20x20 element model as shown in figure 2. Each element is nearly 500x500 μm^2. We used a 3D electromagnetic field solver to compute resistance and inductance of each cell. The field solver computed the inductance and resistances were at several discrete frequency points from DC to 30 GHz. Figure

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3 shows the results of the field solver for the global power grid. Both the inductance and resistance of each element has the expected behavior. At higher frequencies, the current is carried only by the outer skin of the power grid and the inductance asymptotically reaches the skin inductance.

Next we obtained a circuit representation for the power grid. We fit the frequency dependent inductance and resistance of the different metal layers with an 8 R-L element cell as shown Figure 4. The number of elements needed depends on the accuracy of the required model and the bandwidth of interest. An 8 element cell provides a good match between the electromagnetic field solution and the circuit representation for both the inductance and the resistance. An 8 element model however proved to be overkill when computational efficiency is considered.

A distributed model is also used to model the die capacitance. Different time constants are used to model the different types (device and interconnect) of capacitances. The power sinks (logic gates) are also distributed over the power grid to represent the worst case stimulus as realistically as possible.

The distributed circuit model for the power grid then replaces the lumped element representation of the die in figure 1. The power supply impedance is then calculated as described in [4]. Figure 5 shows the simulated power supply impedance. As can be seen from figure 5, the distributed model predicts three additional resonances at 620 MHz, 1.12 GHz, and 2.22 GHz while the lumped model predicts only the 190 MHz package resonance

Measurements and Validation

The objective of the power supply model is to predict the minimum and maximum voltages the processor will ever experience. Once these voltage levels are known, testing at these conditions will ensure reliable operation in the application environment. To minimize the circuit fallout to power supply noise under any loading conditions, it is necessary to design a power supply with a wideband low impedance. Recently there has been progress reported in the literature on measurement techniques for the power supply impedance [5-7]. The techniques generally rely on either exciting the microprocessor with a known stimulus [5] or forcing a known stimulus thru the pins of the package to the microprocessor [6]. Both of these techniques however are not suited for resonances well above 200 MHz. The first technique [5] would require a well characterized stimulus with significant energy content in the high frequency range and the second [6] requires forcing several GHz thru a band limited package. Time domain measurements of very high frequency noise were very difficult until recently when Muhtaroglu et al. demonstrated circuit technologies capable of measuring power supply droops at several GHz [8]. Given the advantages and shortcomings of each of these techniques, we adopted a two stage approach to validating the power supply model.

First, we validated with time domain measurements that the pole locations or resonant frequencies predicted by the distributed power supply impedance model are correct. We did this by measuring the droops in the time domain and extracting the resonant frequencies using the Fourier Transform. These measurements can be done almost with any stimulus and do not contain any meaningful information on the magnitude of the noise at the resonant frequencies. Next we subjected the power supply network to an exhaustive set of stimuli, including the stimulus used in the simulation model. We recorded the worst case measured magnitude of the noise at the resonant frequencies. The minimum voltages were reasonably close to the simulation results.

To get around the package bandwidth limitation, we designed two measurement systems. The first is a direct differential connection route from the global power and ground grids to two package pins. With this design, it is possible to detect and measure resonant frequencies little above 1 GHz. The second measurement system is the on die droop detector (ODDD) published in [8]. The ODDD is capable of detecting resonant frequencies of several GHz and accurately measure the magnitude of the noise at these frequencies.

Finally, figures 6 and 7 shows the time and frequency domain measurements when the microprocessor is subjected to various high di/dt stimuli. The measured frequency components of noise on the power delivery network depended on what type of programs we ran. On the top of figure 6 is the time domain noise waveform during full-chip reset. The bottom curve is the FFT of time domain noise waveform. Figure 7 is similar measurement but running a 3-D graphics-intensive program. By comparing both figures 6 and 7, the 20x20 model successfully predicts 3 groups of frequency components at around 200 MHz, 700 MHz, and 1.1~1.2 GHz. With different stimulus, the frequency components of power delivery noise are significantly different. The ODDD droop detector measurements matched both the simulations and the oscilloscope results.

Summary and Conclusions

In this paper, we have shown that the first order lumped element model used by the industry, and widely published in the literature, is not sufficient to model high frequency resonances. We have shown that the accuracy of this model can be significantly enhanced by including a simple circuit representation of the electromagnetic model. As the frequencies of microprocessor continue to increase, the effects of the wave propagation becomes more pronounced and finer discretization than the 20x20 model will be required. Finally, we have validated the accuracy of the proposed model using time domain scope measurements and the on Die Droop Detector circuit.

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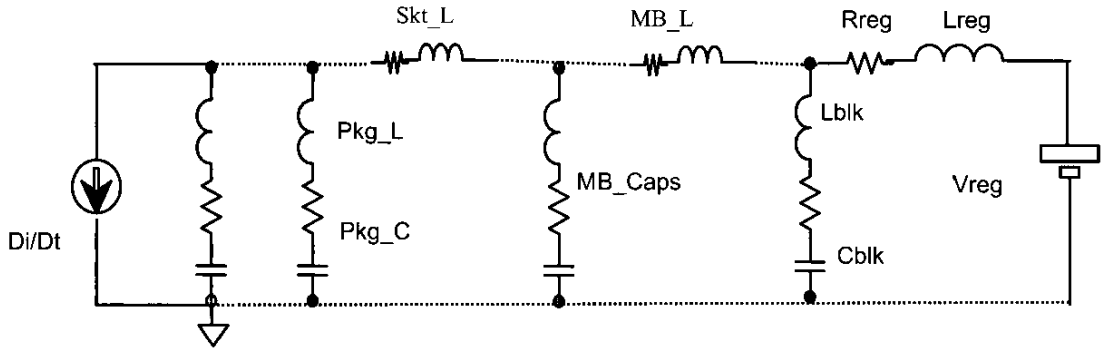

Figure 1: A typical lumped element model for the power supply network of a high speed microprocessor

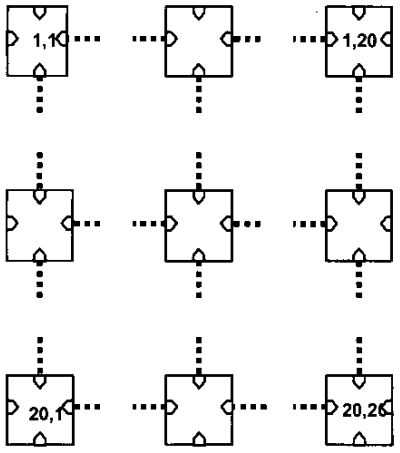

Figure 2: 20X20 cells distributed circuit model for the power grid

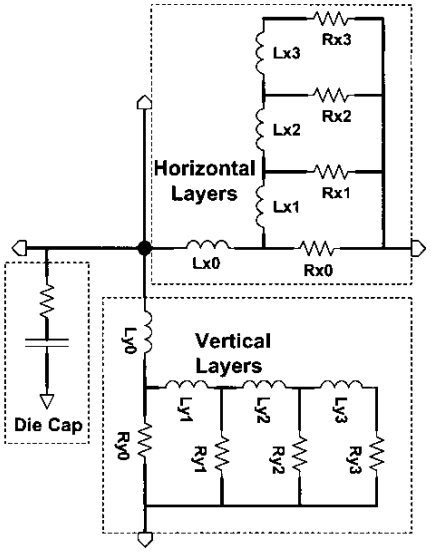

Figure 4: An 8 element circuit representation of a single cell of figure 2

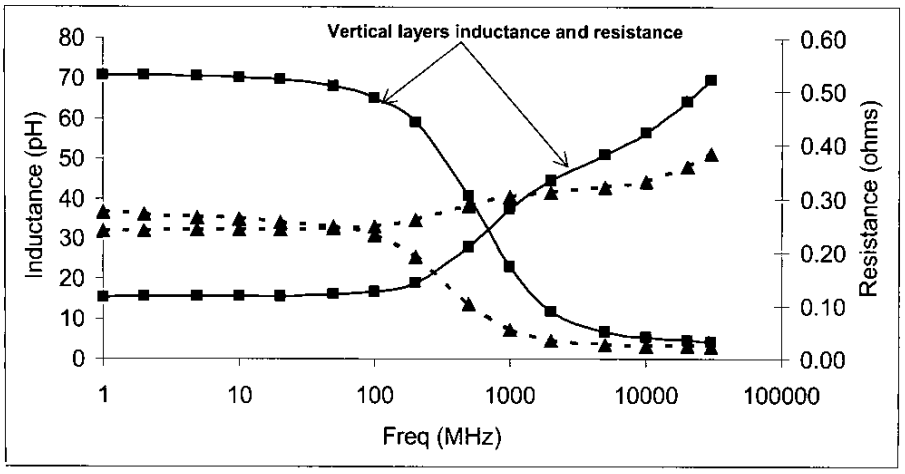

Figure 3: Frequency dependent inductance and resistance for the horizontal and vertical layers of a single cell of figure 2

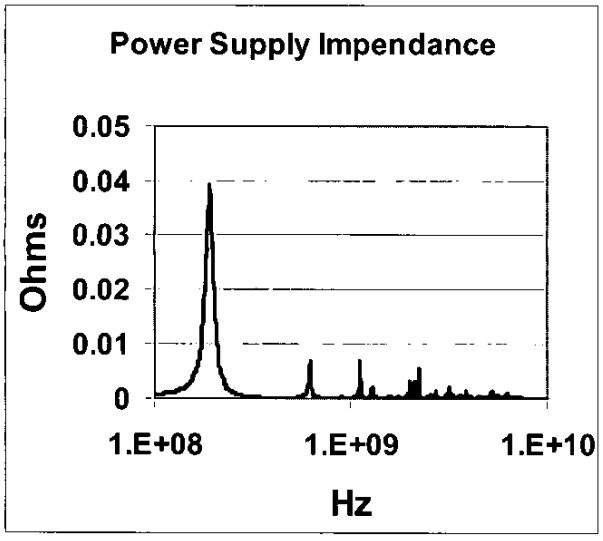

Figure 5: impedance for the power distribution network

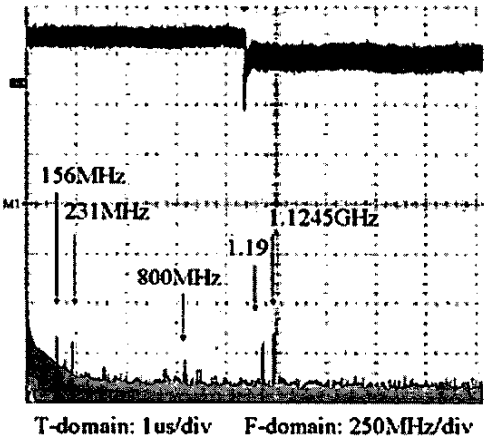

Figure 6: Time domain measurement of the noise waveform during full-chip reset (top) and the FFT (bottom)

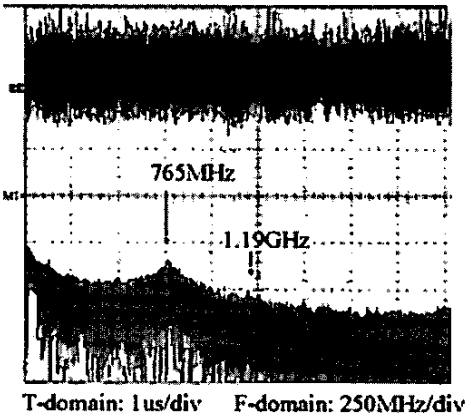

Figure 7: Time domain measurement of the noise waveform running a graphics-intensive program (top) and the FFT (bottom)