Efficient VLSI Power/Ground Network Sizing Based on Equivalent Circuit Modeling

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***Abstract*— We present an efficient method of minimizing the area of power/ground (P/G) networks in integrated circuit layouts subject to the reliability constraints. Instead of directly sizing the original P/G network extracted from a circuit layout as done previously, the new method first constructs a reduced but electrically equivalent P/G network. Then the sequence of linear programming method is applied to optimize the reduced network. The solution of the original network is then back solved from the optimized reduced network. The new method exploits the regularities in the P/G networks to reduce the complexities of P/G networks. Experimental results show that the sizes of reduced networks are typically significantly smaller than that of the original networks. The resulting algorithm is fast enough that P/G networks with more than one million branches can be sized in a few minutes on modern SUN workstations.**

I. Introduction

POWER /Ground (P/G) networks supply power from the P/G pads on a chip to the circuit modules. They experience the largest current flows in a chip and are more susceptible to current-induced reliability and functional failures. Those reliability and functional failures typically come from electromigration, excessive IR drops and delta-I (Ldi/dt) noise[1], [2]. As a result, the wires in a P/G network have to be properly sized to keep those adverse effects under control. The design of reliable, working P/G networks, however, is no longer a trivial task. Designers often attempt to over size a P/G network to avoid the reliability problems. But a substantial amount of chip area can be wasted with this conservative design strategy. The problem becomes even worse for very deep submicron designs where even more silicon area has to be dedicated to P/G network routing and the constraints from design rules and the reliability consideration become more stringent. Hence an important design task is how to use the minimum amount of chip area for wiring P/G networks while avoiding potential reliability failures due to electromigration and excessive IR drops.

P/G network design typically consists of several steps – topology design, sizing of wire segments in P/G networks and the allocations and placement of decoupling capacitances if delta-I noise is significant. Topology design of a P/G network is commonly carried out by P/G routers. In this paper, we address the second step, that is to size the wire segments with fixed topologies of P/G networks. Several methods have been developed to solve this wire sizing problem [5], [6], [7], [9], [16]. Most of these methods formulate the wire sizing problem as a constrained nonlinear programming problem. Existing approaches such as augmented Lagrangian method [5], conjugate gradient method [7], feasible direction method [9] to this problem are known to be computationally intensive and cannot be scaled to solve large P/G networks containing millions of wire segments [3], [10].

Recently, P/G optimization methods that explicitly consider the transient behavior of a P/G network were proposed in [4], [8], [11], [13], [15]. The common practice to reduce the transient noise due to capacitive and inductive effects is by means of adding decoupling capacitances. The decoupling capacitance allocation is performed in the floorplanning stage in [8], [11]. The placement issue of the decoupling capacitances was investigated in [4] by using frequency domain sensitivity analysis. But all of those methods fail to consider wire sizing for IR drop reduction. In [13] wire sizing based on time domain sensitivity analysis is employed to reduce the transient noise. But capability of this method depends on the efficiency of the underlying analysis algorithm and the method takes hours to solve P/G networks with only a few thousand nodes. Time domain sensitivity analysis was also used to reduce the transient noise by sizing and placing decoupling capacitors in [15] and by wiresizing along with signal net routing in [14]. Still reported sizes of P/G networks are quite small.

In 1999, we proposed an efficient algorithm to solve the P/G wire sizing problem [16]. Our approach is still based on the resistor-only model for the P/G wires. We consider the reduction of transient noise due to capacitive and inductive effects as a separate step before or after the wire sizing process. Our method is an extension of the relaxed two-phase optimization method by Chowdhury [7]. The idea is to further relax the nonlinear objective function and then translate the constrained nonlinear programming problem into a sequence of linear programming problems. The method was demonstrated to be orders of magnitude faster than the previously best-known method using the conjugate gradient algorithm. For P/G networks with millions of wire segments, commonly seen in typical ASIC designs, the sequence of linear programming method, however, remains too slow to handle such networks.

In this paper, we present an efficient approach to solving the

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large scale P/G optimization problem subject to reliability constraints. Some early results of this approach were published in [17]. Our method is based on the sequence of linear programming method (SLP) [16]. In our new method, we first attempt to reduce the original P/G networks by replacing many regular series resistor circuits with smaller, electrically equivalent models. The resulting networks, which typically are much smaller than the original ones, are solved by the SLP method and the solutions of original networks are finally back solved from the optimized, reduced networks. The success of the new method is based on the observation that many wire segments share the same width in a P/G circuit due to typical design rule requirements. Experimental results have shown that the proposed algorithm scales very well to attack large P/G networks with many regular structures. For instance, a P/G network with 10k branches can be solved in a few seconds and the one with more than a millions branches can be solved in a few minutes on modern SUN workstations.

This paper is organized as follows: Section II describes the formulation of the P/G network optimization problem, and reviews the sequence of linear programming method. The new method is presented in Section III. Experimental results on some large P/G networks and the comparison with the SLP method are summarized in Section IV. Section V concludes the paper.

II. Problem Formulation and Review of Sequence of Linear Programming

Following [7], [16], we formulate the wire sizing problem in terms of node voltages and branch currents. After the problem formulation, we will briefly review the sequence of linear programming method.

A. Problem Formulation

Let $G = \{N, B\}$ be a P/G network with n nodes $N = \{1, ..., n\}$ and b branches $B = \{1, ..., b\}$. Each branch i in B connects two nodes: i_1 and i_2 with current flowing from i_1 to i_2. Let l_i and w_i be the length and width of branch i, respectively. Let ρ be the sheet resistivity. Then the resistance r_i of branch i is $r_i = \frac{V_{i_1} - V_{i_2}}{I_i} = \rho \frac{l_i}{w_i}$.

1) Objective Function: We can express total P/G routing area in terms of voltages, currents and lengths of branches as follows:

$$f(\mathbf{V}, \mathbf{I}) = \sum_{i \in B} l_i w_i = \sum_{i \in B} \frac{\rho I_i l_i^2}{V_{i_1} - V_{i_2}}. \tag{1}$$

We notice that the objective function is linear for branch current variables **I** and nonlinear for node voltage variables **V**.

2) Constraints: The constraints that need to be satisfied for a reliable, working P/G network are as follows.

1) **The voltage IR drop constraints.** To ensure the correct and reliable logic operation, the voltage drop (IR drop) from the P/G pads to the leaf nodes should be restricted. We then impose the following constraints to every leaf node.

$$\begin{aligned} V_i &\geq V_{min} \text{ for power networks,} \\ V_i &\leq V_{max} \text{ for ground networks,} \end{aligned} \tag{2}$$

where V_{min} and V_{max} are given constants based on the technology and the routing layer.

2) **The minimum width constraints.** The widths of the P/G segments are technologically limited to the minimum width allowed in the layer where the segment lies. Thus, we have

$$w_i = \rho \frac{l_i I_i}{V_{i_1} - V_{i_2}} \geq w_{i,min}, \tag{3}$$

where $w_{i,min}$ are given constants.

3) **The electromigration constraints.** Electromigration on a P/G wire segment sets an upper bound on the current density of the segment [1]. For a routing layer with fixed thickness. This constraint for branch i is expressed as $|I_i| \leq w_i \sigma$, and can be re-written as the following nodal voltage constraint:

$$|V_{i_1} - V_{i_2}| \leq \rho l_i \sigma, \tag{4}$$

where, σ is a constant for a particular routing layer with a fixed thickness.

4) **Equal width constraints (coupling constraints)**. For typical chip layout designs, most commercial P/G routers do not allow the widths of P/G wire segments to be arbitrary values with respect to other wire segments. Instead, certain P/G wire segments should have the same width. For example, the wire segments in a P/G ring around macro cells in ASIC designs. The constraint can be written as $w_i = w_j$. In terms of nodal voltages and branch currents, we have

$$\frac{V_{i_1} - V_{i_2}}{l_i I_i} = \frac{V_{j_1} - V_{j_2}}{l_j I_j}. \tag{5}$$

5) **Kirchoff's current law (KCL).**

$$\sum_{i \in B(j)} I_i = 0, \tag{6}$$

for each node $j = \{1, ..., n\}$ and $B(j)$ is the set of indices of branches connected to node j.

P/G network optimization is to minimize (1) subject to constraints (2), (3), (4) (5) and (6). It will be referred to as Problem **P** thereafter. Since both the node voltage **V** and branch current **I** are chosen as variables, the objective function and some of the constraints are nonlinear. Hence, problem **P** is a constrained nonlinear optimization problem.

B. Review of Sequence of Linear Programming Method

Sequence of linear programming follows the problem formulation proposed by Chowdhury [7], which relaxes the original problem **P** by dividing the problem into two phases – **P-V** and **P-I**. The relaxed problem, whose solution space is a subset of the original one, becomes a convex problem (has only one optimal solution) and thus is much easier to solve than the original one.

But problem **P-V** is still a nonlinear programming problem as the objective function (1) is still nonlinear in terms of **V**. In the SLP method, the problem **P-V** is further relaxed by linearizing the objective function $f(\mathbf{V})$ around the initial solution $\mathbf{V}_0$,

so both **P-I** and **P-V** become linear programming problems as shown in the following:

- Phase one: **P-V**
  All node voltages become variables and all branch currents are constants. Then the objective is

$$g(\mathbf{V}) = \sum_{i \in B} \frac{2\alpha_i}{(V_{i_1}^0 - V_{i_2}^0)} - \sum_{i \in B} \frac{\alpha_i}{(V_{i_1}^0 - V_{i_2}^0)^2}(V_{i_1} - V_{i_2}). \quad (7)$$

  where $\alpha_i = \rho I_i l_i^2$.
  The optimization is subject to the following constraints (2), (3), (4), (5) and

$$\frac{V_{i_1} - V_{i_2}}{I_i} \geq 0, \quad (8)$$

  where I_i is a constant and

$$\xi sign(I_i)(V_{i_1}^0 - V_{i_2}^0) \leq sign(I_i)(V_{i_1} - V_{i_2}), \quad (9)$$

  where $\xi \in (0, 1)$.
- Phase two: **P-I**
  In this step, branch currents become variables and all nodal voltages are constants. Then the objective function can be re-written as:

$$f(\mathbf{I}) = \sum_{i \in B} \beta_i I_i, \quad (10)$$

  where $\beta_i = \frac{\rho l_i^2}{V_{i1} - V_{i2}}$, subject to constraints (3), (5) and (6).

The SLP algorithm starts with an initial feasible solution, then iteratively solves two linear programming problems **P-V**, then **P-I**.

III. New Power/Ground Optimization Method

The new method is based on the observation that many wire segments have the same width in a P/G network due to design rule requirements. As a result, not all node voltages and branch currents need to be explicitly constrained. By exploiting the regularities and their implications on the node voltages and branch currents, we can reduce a P/G network by using equivalent circuit modeling. SLP can then be applied to the reduced network to obtain the optimal solution more efficiently.

In this section, we first present how a series resistor chain can be modeled by a simple equivalent circuit. Then we show how equivalent circuits are constructed for P/G optimization and how the corresponding constraints are transformed for the reduced P/G network.

A. Equivalent Circuit Modeling of Series Resistor Chains

Consider a chain of series resistors commonly seen in a P/G network as shown in Figure 1. There exists voltage V_s, between the two series ends, N_1 and N_n, coming from the interaction of the series resistor chain with the rest of the network. Suppose the positive current direction for resistive branch (wire segment) R_i is from N_i to N_{i+1}. Since the series resistor and current chain is a linear network, its terminal behavior can be modeled by a much simpler equivalent circuit as shown in Figure 2 [12], where the positive current direction of R_s is from N_1 to N_n. The equivalent resistance R_s is just the sum of all the resistances in series,

$$R_s = \sum_{i=1}^{n-1} R_i. \quad (11)$$

By superposition, each current source divides between the two ends. For a current source, the divided current at each end can be computed by replacing all the other current sources by open circuits and replacing the voltage source V_s between node N_1 and N_n by a short circuit. The current contributions from all the current sources are the equivalent current I_{e_1} and I_{e_n} as shown in the following:

$$I_{e_1} = \sum_{i=1}^{n-2} \frac{\sum_{j=i+1}^{n-1} R_j}{R_s} I_i, \quad (12)$$

$$I_{e_n} = \sum_{i=1}^{n-2} \frac{\sum_{j=1}^{i} R_j}{R_s} I_i, \quad (13)$$

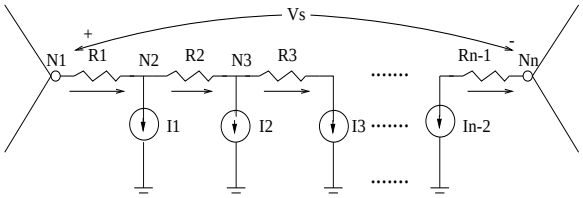

Fig. 1. A series resistor chain.

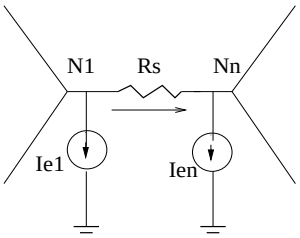

Fig. 2. The equivalent circuits for a series resistor chain.

Once the reduced network has been solved with the equivalent network and the voltages at the end nodes are known, the voltages at the intermediate nodes can be back solved one by one based on superposition as follows:

$$V_{i+1} = V_i - \frac{R_i}{R_s} V_s - R_i I_{e_i}, \quad (14)$$

$$I_{e_{i+1}} = I_{e_i} - I_i. \quad (15)$$

B. Equivalent Circuit Modeling for P/G Optimization

The equivalent circuit modeling method was originally developed for fast P/G network simulation [12]. To apply the method to our P/G optimization problem, we have to consider the following differences:

- **All the resistors in a chain should have the same current direction.**
  We observe that not all the node voltages in a series resistor chain need to be constrained by IR drop constraints.

We should consider the nodes whose voltages are either the local minimum or the local maximum. This means that not all the intermediate nodes in a series resistor chain can be suppressed. Figure 3 shows two scenarios where node voltages are the local minimum or the local maximum and the corresponding nodes cannot be suppressed. With this restriction, a physical series resistor chain has to be broken into several sub-chain circuits, and the currents of all the resistive branches in each of the sub-chains should have the same sign. In other words, currents flow in the same direction in a sub-chain. Knowing this, it is sufficient to consider the voltages at the ends of a sub-chain circuit.

Such a restriction is consistent with the requirement in the SLP method [16] that the current directions will not change after optimization. So at the end of the optimization, voltages of those nodes will still be either the minimum or the maximum in the sub-chain circuit. This means that the equivalent circuit modeling will be valid for both the optimized P/G equivalent circuit and optimized original circuit.

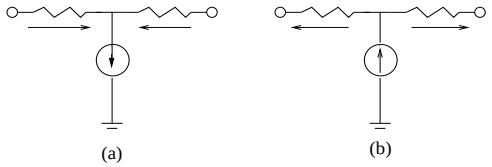

Fig. 3. Nodes can not be suppressed (a) nodes in power networks (b) nodes in ground networks.

- **All the resistors in a chain share the same width.**
  Observing the widths of all the resistive branches in a series resistor chain are typically identical, and subsequently a series resistor chain is typically extracted from a straight P/G trunk or one side of a power/ground ring that commonly are routed with one routing layer.
  With this assumption, all the equivalent currents computed in (12) and (13) will remain unchanged during optimization. The width of the each individual wire segment will be the width of the equivalent resistor and the resistance of each individual wire segment after optimization can easily be back solved. Let R_i', the unknown variable, and R_s' be the resistance of R_i and R_s after optimization, respectively, then

$$R_i' = \frac{R_s'}{R_s} R_i. \tag{16}$$

- **The Electromigration constraints.**
  Finally, electromigration constraint (4) also needs to be modified to accommodate the changes in equivalent circuit modeling.
  Consider the series resistor sub-chain in Figure 1. The current flowing through resistor R_i, I_{R_i}, has two components:

$$I_{R_i} = I_s + I_{e_i}, \tag{17}$$

where $I_s (= \frac{V_s}{R_s})$ is due to the voltage drop of V_s across R_i and it is also the current flowing through R_s in the reduced network. I_{e_i} is the current flowing through R_i when V_s is replaced by a short circuit, and I_{e_i} is computed in (15). Notice that all the currents $I_{R_i}, i \in [1, n-1]$ will have the same sign in a series resistor sub-chain. Without losing generality, we assume currents are always flowing from N_1 to N_n, i.e. $I_{R_i} > 0, i \in [1, n-1]$. Then we have

$$I_{R_i} \geq I_{R_j}, \text{for } i < j. \tag{18}$$

This is because $I_{e_i} > I_{e_j}$ for $i < j$ according to (15). So R_1 will experience the largest current. Since all the resistors in a series resistor chain share the same width, we only need to consider the current of R_1 for the electromigration problem as R_1 sees the largest current density. Similarly, for a ground network, with the same assumption of the positive current direction for each resistive branch, we only need to consider current of R_n for the electromigration problem. By using the I_{R_1} or I_{R_n} as the current for the equivalent resistor R_s, electromigration constraint (4) for R_s shown in Figure 2 will become

$$|V_{s_1} - V_{s_2}| \leq \frac{\rho l_s \sigma}{1 + \frac{I_{e_1}}{I_s}} \text{ for power networks,}$$
$$|V_{s_1} - V_{s_2}| \leq \frac{\rho l_s \sigma}{1 + \frac{I_{e_n}}{I_s}} \text{ for ground networks.} \tag{19}$$

Note that constraint (19) is a linear constraint for both **P-V** and **P-I**. Another important difference it that we have to explicitly consider the electromigration constraints in problem **P-I** now.

As an illustration, Figure 4 and Figure 5 show, respectively, a 3×3 power network and its corresponding reduced network.

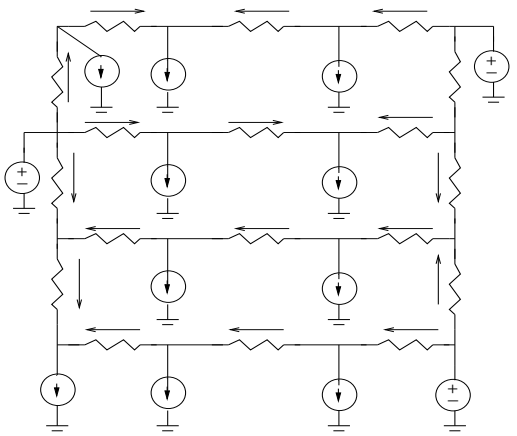

Fig. 4. A 3×3 power network; Current direction in each resistive branch is marked.

The flow chart of the entire new optimization procedure is shown in Figure 6

The detailed explanation of each step in Figure 6 is given as follows:

New P/G Optimization Algorithm

1) Analyze the network G to obtain an initial feasible solution and construct the equivalent network G_e of G and designate the initial solution in G_e as $\mathbf{V}_e^k, \mathbf{I}_e^k$ for $k = 0$.
2) Construct the minimum width constraints (3), equal width constraints (5), constraints (9) and electromigration constraints (19) using $\mathbf{I}_e^k$.

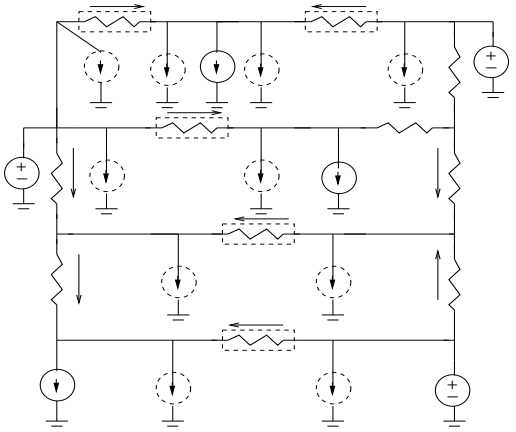

Fig. 5. The equivalent circuit of the 3×3 power network. All the equivalent resistors are marked with dotted surrounding boxes and the equivalent currents are shown at both ends of the equivalent resistors.

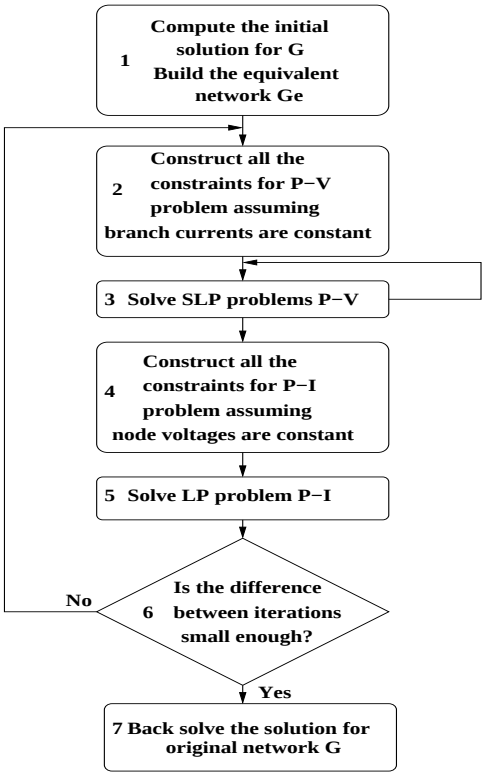

Fig. 6. The new P/G optimization algorithm.

3) Minimize $g(\mathbf{V}_e^k)$ subject to constraints (2), (3), (5), (9), and (19) by a sequence of linear programming, record the result as $\mathbf{V}_{e,l}^k$, where l begins from 1. If $f(V_{e,l}^k) > f(V_{e,l-1}^k)$, do the line search along the direction $\mathbf{d} = (V_{e,l-1}^k - V_{e,l}^k)$ until $f(V_{e,l}^k) \leq f(V_{e,l-1}^k)$. Record the result from the last iteration l and line search in step 3 as $\mathbf{V}_e^{k+1}$. Constraints (2), (3), (5), (9), and (19) are repeated respectively in the following:

$$\begin{aligned} V_i &\geq V_{min} \text{ for power networks,} \\ V_i &\leq V_{max} \text{ for ground networks,} \end{aligned}$$

$$w_i = \rho \frac{l_i I_i}{V_{i_1} - V_{i_2}} \geq w_{i,min},$$

$$\frac{V_{i_1} - V_{i_2}}{l_i I_i} = \frac{V_{j_1} - V_{j_2}}{l_j I_j},$$

$$\xi sign(I_i)(V_{i_1}^0 - V_{i_2}^0) \leq sign(I_i)(V_{i_1} - V_{i_2}),$$

$$|V_{s_1} - V_{s_2}| \leq \frac{\rho l_s \sigma}{1 + \frac{I_{e1}}{I_s}} \text{ for power networks,}$$

$$|V_{s_1} - V_{s_2}| \leq \frac{\rho l_s \sigma}{1 + \frac{I_{en}}{I_s}} \text{ for ground networks.}$$

4) Construct the minimum width constraints (3), equal width constraints (5) and electromigration constraints (19) using $\mathbf{V}_e^{k+1}$ for each branch.
5) Minimize the objective function (10) subject to the constraints (3), (5), (6), and (19) by linear programming and record the result as $\mathbf{I}_e^{k+1}$. Constraints (3), (5), (6), and (19) are repeated respectively in the following:

$$w_i = \rho \frac{l_i I_i}{V_{i_1} - V_{i_2}} \geq w_{i,min},$$

$$\frac{V_{i_1} - V_{i_2}}{l_i I_i} = \frac{V_{j_1} - V_{j_2}}{l_j I_j},$$

$$\sum_{i \in B(j)} I_i = 0,$$

$$|V_{s_1} - V_{s_2}| \leq \frac{\rho l_s \sigma}{1 + \frac{I_{e1}}{I_s}} \text{ for power networks,}$$

$$|V_{s_1} - V_{s_2}| \leq \frac{\rho l_s \sigma}{1 + \frac{I_{en}}{I_s}} \text{ for ground networks.}$$

6) If $|f(\mathbf{V}_e^{k+1}, \mathbf{I}_e^{k+1}) - f(\mathbf{V}_e^k, \mathbf{I}_e^k)| < \epsilon$, ϵ is the termination criterion, then stop, otherwise k = k + 1 and goto step 2.
7) Back solve the $\mathbf{V}$ and $\mathbf{I}$ of G from $\mathbf{V}_e^{k+1}$ and $\mathbf{I}_e^{k+1}$ and obtain the wire width for each wire segment in G.

IV. Experimental Results

A computer program for P/G network optimization has been developed based on the proposed method. We tested the program on a set of P/G networks on a SUN workstation with one 296 MHz SPARC processor and 1GB memory. The set of P/G network test cases have complexities ranging from ten to one million wire segments. The proposed method is compared against the pure SLP algorithm [16] in terms of CPU time and the quality of results. For all the test cases we assume that all the wire segments in a series resistor chain share the same width and the same width constraints are enforced in both the new method and the pure SLP method. The minimum width allowed for all the P/G circuits are $0.4\mu m$ and most of P/G wires are initially set to $0.8\mu m$. The supply voltage for all the power networks is 5.0 volt. We allow 6% (0.3 volt) IR drop for all the P/G circuits. The current sources in each P/G circuit are scaled such that the initial solutions are always feasible. The results are summarized in Table I.

In Table I, column 1 shows the names of the P/G networks tested. Columns 2 to 5 list, respectively, the number of

TABLE I
COMPARISON OF THE NEW ALGORITHM AGAINST THE SLP METHOD.

ckt	pure SLP method				new algorithm				Speedup	max IR(Be)	max IR(Af)
	#nodes	#bchs	time(sec)	area(%)	#nodes	#bchs	time(sec)	area(%)			
pg4x4	17	23	0.28	50.0	7	13	0.01+0.22	50.0	1.22	0.086	0.17
pg20x20	400	439	4.02	50.0	31	70	0.01+0.30	48.4	12.97	0.13	0.26
pg300x10	3001	3599	110.88	50.0	429	1027	0.46+6.42	50.0	16.12	0.038	0.077
pg100x100	10001	10199	1079.30	49.99	154	352	3.04+1.39	49.99	243.63	0.028	0.056
pg1000x1000	1×10^6	2×10^6	$>$70 hrs	-	3529	9089	38.04+92.31	9.85	$>$276.18.	0.27	0.3

nodes in the circuit (*#nodes*), the number of branches (*#bchs*) which accounts for the resistive branches, CPU time in seconds (*time(sec)*) and the reduced chip area of the original area in percentage (*area (%)*) for the pure SLP method. Columns 6 to 9 show the same criteria for the new algorithm. Column 10 gives the speedup of the new algorithm over the pure SLP method. The last two columns show the maximum IR drops before (*max IR(Be)*) and after (*max IR(Af)*) optimization for the new algorithm. The CPU time for the new algorithm consists of two parts. The first part is due to the construction of equivalent circuits and the second part is the time for the P/G optimization by SLP and back solving of original networks.

It is shown in Table I that equivalent circuit modeling can significantly reduce the complexities of the P/G networks. For instance, for circuit $pg100 \times 100$, 98.4% nodes and 96.5% branches have been suppressed. For $pg1000 \times 1000$, 99.6% nodes and 99.5% branches are gone. With the reduced P/G networks in which node and branch counts are no more than a few of thousands, they can be solved by SLP very efficiently. Two orders of magnitude speedup over the pure SLP method on larger test cases is a clear evidence of the effectiveness of the equivalent circuit modeling technique. With this, network $pg1000 \times 1000$, which has more than one million branches, can be optimized in a few minutes. To the best of our knowledge, this is the largest P/G network ever optimized by a P/G optimization algorithm in a reasonable time. On the contrast, the pure SLP method was unable to find any solution after a 10-hour trial.

The area reduction for most of the tested P/G networks is about 50%. The actual improvements, however, strongly depend the initial solutions. After optimization, the maximum IR drops have been increased due to downsized wires. We notice that the area reduction of the first four P/G networks is mainly bounded by the minimum width of each wire, the last circuit is mainly bounded by the given IR drop constraints. It is apparent both algorithms give the same results for most of test cases. The discrepancy in network $pg20 \times 20$ is due to some numerical issues in the linear programming process.

Also we notice that how many nodes and branches that can be suppressed depend on the topologies of the P/G networks. Table II shows how P/G network topologies affect the complexities of reduced P/G networks and normalized CPU times for the optimization process. We use a number of P/G networks with similar complexities but different topologies. All the P/G networks have 10 rows and each row has 1000 resistor-current sections. The difference is that each P/G network has a different number of vertical P/G strips and each P/G strip consists of a number of resistors connecting all the rows. With vertical P/G strips, we have mesh-structured P/G networks.

In Table II, column 1 shows the names of the P/G networks tested. Column 2 gives the number of P/G strips in the P/G networks. Columns 3 to 6 list, respectively, the number of nodes (*# nodes*), the number of resistive branches (*# bchs*) in the original network, the number of nodes (*# nodes(equ)*), the number of resistive branches (*# bchs(equ)*) in the reduced network. The last column shows the normalized CPU times (with respect to the first P/G network) for optimization.

From Table II, we can easily see that the topology of a P/G network has a large impact on the effectiveness of the new algorithm. With more P/G strips, fewer circuit nodes can be suppressed. Specifically, for the P/G networks in Table II, $\#row \times \#strip$ gives the lower bound for the number of nodes in each reduced network. The actual numbers of nodes are close to the given low bounds. In real P/G networks, the numbers of P/G strips used should be significantly smaller than that of resistor-current sections, which still renders our method very efficient.

Our work is based on the resistive-only models for P/G networks. But the capacitive and inductive effects in P/G networks with current technologies have reached a point where they are no longer second-tier effects for some high performance designs.

For the transient behavior of a P/G network due to capacitive and inductive effects, we would like to view the corresponding noise reduction as a separate step as suggested by recent publications [4], [8], [11], [15]. The common practice is by adding decoupling capacitances subject to floorplanning and placement constraints. The output of our optimization process is a working P/G network based on the steady-state current consumption for each individual current source with some noise margins for transient voltage variations. The actual transient noise at each node that goes beyond the allowed noise margin is taken care of by the decoupling capacitance allocation process where a more detailed RLC model can be used for the P/G network.

One area we would like to study in the future is how to efficiently build the steady-state current models for time-varying current consumptions of circuit modules, and how to set up the noise margins such that the worst case transient noise can be sufficiently controlled by a decoupling capacitance allocation process. To this end, the decoupling capacitance should be properly budgeted early in the design flow, for instance in floorplanning. A decoupling allocation process that can effectively honor the decoupling requirements from the wire sizing process is also an important topic.

V. CONCLUSIONS

A fast power/ground optimization method based on equivalent circuit modeling was proposed for sizing the widths of the

TABLE II

RESULTS FOR DIFFERENT TOPOLOGIES OF SIMILAR P/G NETWORKS.

ckt	# strip	# nodes	# bchs	# nodes(equ)	# bchs(equ)	norm time(sec)
pg10x1000-5	5	10001	10055	61	115	1.00
pg10x1000-10	10	10001	10100	103	202	1.37
pg10x1000-20	20	10001	10190	202	391	2.01
pg10x1000-50	50	10001	10460	501	960	8.26
pg10x1000-100	100	10001	10910	1001	1910	42.50
pg10x1000-200	200	10001	11810	2001	3810	192.59

wire segments in a power/ground network under reliability constraints.

Experimental results have shown that this new algorithm can be more than two orders of magnitude faster than the sequence of linear programming method, the best-known power/ ground optimization algorithm, on large power/ground networks with many regular structures. The power of the new algorithm was fully demonstrated with the optimization of a power/ground network with more than a million branches in a few minutes on modern SUN workstations. We have shown that the P/G network topologies and regularities have a considerable impact on the effectiveness of this new algorithm.

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