

Reliability-Constrained Area Optimization of VLSI Power/Ground Networks Via Sequence of Linear Programmings

Sheldon X.-D. Tan, *Member, IEEE*, C.-J. Richard Shi, *Senior Member, IEEE*,
Jyh-Chwen Lee, *Member, IEEE*

Abstract— This paper presents a new method of sizing the widths of the power and ground routes in integrated circuits so that the chip area required by the routes is minimized subject to electromigration and IR voltage drop constraints. The basic idea is to transform the underlying constrained nonlinear programming problem into a sequence of linear programs. Theoretically, we show that the sequence of linear programs always converges to the optimum solution of the relaxed convex optimization problem. Experimental results demonstrate that the proposed sequence-of-linear-program method is orders of magnitude faster than the best-known method based on conjugate gradients with constantly better solution qualities.

I. INTRODUCTION

POWER /Ground (P/G) networks connect the power/ground supplies in the circuit modules to the P/G pads on a chip. An important problem in P/G network design is to use the minimum amount of chip area for wiring power/ground networks while avoiding potential reliability failures due to electromigration and excessive IR drops. Specifically, we are concerned with the problem of P/G network optimization where the topologies of P/G networks are assumed to be fixed, and only the widths of wire segments are to be determined. Several methods have been developed to solve this problem [6], [7], [8], [9]. However, to the best of our knowledge, none of these methods have been incorporated into commercial computer-aided design (CAD) tools and used by industry.

One major obstacle is that these methods are based on constrained nonlinear programming, a process known to be computationally intensive (NP-hard [12]). These methods are applicable only to small size problems, while P/G networks in today's very large scale integration (VLSI) design may contain millions of wire segments (therefore, millions of variables). On the other hand, with the continuous shrinking of the chip feature size, P/G network optimization is becoming increasingly important,

Manuscript received August 20, 2000, revised August 17, 2002 and February 3, 2003. Some preliminary results of this paper were presented at *ACM/IEEE 38th Design Automation Conference (DAC'99)*, New Orleans, June 1999. The paper was recommended by Associate Editor Majid Sarrafzadeh.

Sheldon X.-D. Tan is with Department of Electrical Engineering, University of California, Riverside, Riverside, CA 92521 USA (e-mail: stan@ee.ucr.edu).

C.-J. Richard Shi is with Department of Electrical Engineering, University of Washington, Seattle, WA 98195 USA.

Jyh-Chwen Lee is with Synopsys Inc, 700 East Middlefield Road, Mountain View, CA 94043 USA.

Publisher Item Identifier TCAD.2003.3000

since more and more portions of the chip area are dedicated to power/ground routings, and the problems of IR drop and electromigration deteriorate.

In this paper, we present a new method capable of solving the power/ground optimization problem orders of magnitude faster than the best known method. Our method is inspired by a key observation made by Chowdhury that if currents in wire segments are fixed, and voltages are used as variables, then the resulting optimization problem is convex [8]. However, instead of using the conjugate gradient method as in [8], we show that the problem can be solved elegantly by a sequence of linear programs. We prove that there always exists a sequence of linear programs that converge to the optimal solution of the original convex optimization problem. Experimental results have demonstrated that usually a few linear programs are required to reach the optimal solution. The complexity of the proposed method is proportional to the complexity of linear programming (which can be solved in polynomial time [5], [12]). Therefore, our method is scalable, i.e., the CPU time increases approximately polynomially with the size of a network. In practice, we have observed that the new method is orders of magnitude faster than the conjugate gradient method with constantly better optimization results.

This paper is organized as follows. Section II reviews some previous work. Section III describes the formulation of the P/G network optimization problem. The new method is presented in Section IV. Some practical considerations are described in Section V. Experimental results from some large P/G networks are summarized in Section VI. Section VII concludes the paper.

II. PREVIOUS WORK

It is generally assumed that the average current drawn by each module is known and is modeled as an independent current source (we do not consider the temporal correlations of current sources). The constraints from reliability and design rules include:

1. IR voltage drop constraints,
2. metal-migration constraints,
3. minimum width constraints,
4. equal width constraints.

The problem of determining the widths of wire segments of a P/G network to minimize the total P/G routing area subject to all

these constraints is a constrained nonlinear optimization problem [6], [7].

In the method of Chowdhury and Breuer [6], resistance values and branch currents are selected as independent variables. Both the objective function and the IR voltage drop constraints become nonlinear. The augmented Lagrangian method combined with the steepest descent algorithm [1] is used to solve the resulting problem.

Dutta and Marek-Sadowska [9] used only resistance values as variables. All the constraints expressed in terms of nodal (terminal) voltages and branch currents, which have to be obtained by explicitly solving an electrical network, become nonlinear. The feasible direction method [4] is employed to solve the nonlinear optimization problem. At each iteration step, extra effort is required to solve the electrical network for nodal voltages and branch currents, as well as their gradients by numerical differentiation.

Chowdhury [8] proposed a very interesting approach where both the nodal voltages and the branch currents are selected as variables. The optimization problem is solved iteratively in two stages. In the first stage, all the branch currents are fixed, and this leads to a convex programming problem solved by the conjugate gradient method [1]. In the second stage, all the nodal voltages are assumed fixed with branch currents as variables, and this leads to a linear programming problem. In comparison with other methods, this method is more general and more efficient. Unfortunately, the conjugate gradient method is not efficient enough to solve large size power/ground optimization problems arising in today's VLSI design.

A method proposed by Mitsuhashi and Kuh [11] further extends power/ground network optimization to include P/G network topology selection. In this paper, we assume that the topology is fixed.

III. PROBLEM FORMULATION AND GENERAL OPTIMIZATION PROCEDURE

Our work follows the formulation and the general optimization procedure of Chowdhury [8]. His results are first reviewed briefly in this section.

A. Problem Formulation

Let $G = \{N, B\}$ be a P/G network with n nodes $N = \{1, \dots, n\}$ and b branches $B = \{1, \dots, b\}$. Each branch i in B connects two nodes $i1$ and $i2$ with nodal voltages V_{i1} and V_{i2} such that current I_i flows from $i1$ to $i2$. Let l_i and w_i be the length and width of branch i . Let ρ be the sheet resistivity. Then resistance r_i of branch i can be expressed as: $r_i = \frac{V_{i1} - V_{i2}}{I_i} = \rho \frac{l_i}{w_i}$. The total P/G routing area, which is the objective function to be minimized, can be expressed as

$$f(\mathbf{V}, \mathbf{I}) = \sum_{i \in B} l_i w_i = \sum_{i \in B} \frac{\rho I_i l_i^2}{V_{i1} - V_{i2}}. \quad (1)$$

Instead of using widths w_i , $i \in B$, as variables, we choose to solve for branch current I_i and nodal voltages V_{i1} and V_{i2} . The constraints to be satisfied are as follows.

1) The IR drop constraints.

$$\begin{aligned} V_j &\geq V_{j,min} && \text{if node } j \text{ is connected to a power pad.} \\ V_j &\leq V_{j,max} && \text{if node } j \text{ is connected to a ground pad.} \end{aligned} \quad (2)$$

where $V_{j,min}$ and $V_{j,max}$, $j = 1 \dots n$, are given constants.

2) The minimum width constraints.

$$w_i = \rho \frac{l_i I_i}{V_{i1} - V_{i2}} \geq w_{i,min}, \quad (3)$$

where $w_{i,min}$, $i = 1 \dots b$, are given constants.

3) The current density constraints (electromigration).

For a fixed thickness σ of a layer, this constraint for branch i can be expressed as [3] $|I_i| \leq w_i \sigma$. It can be re-written as the following nodal voltage constraint:

$$|V_{i1} - V_{i2}| \leq \rho l_i \sigma. \quad (4)$$

4) Equal width constraints.

The constraint can be written as $w_i = w_j$ for segment i and segment j . In terms of nodal voltages and branch currents, we have

$$\frac{V_{i1} - V_{i2}}{l_i I_i} = \frac{V_{j1} - V_{j2}}{l_j I_j}. \quad (5)$$

5) Kirchoff's current law (KCL).

$$\sum_{i \in B(j)} s_i I_i = 0, \quad (6)$$

for each node $j = \{1, \dots, n\}$ and $B(j)$ is the set of indices of branches connected to node j and s_i is 1 if the current direction for branch i is toward node j and -1 otherwise.

P/G network optimization is to minimize (1) subject to constraints (2), (3), (4), (5), and (6). It will be referred to as problem **P**. Problem **P** is a constrained nonlinear optimization problem.

B. Relaxed Two-Step Optimization Procedure

To reduce the complexity of solving problem **P**, Chowdhury proposed the following relaxed two-step optimization procedure:

- Problem **P1**: Assuming that all branch currents are fixed, the objective function becomes

$$f(\mathbf{V}) = \sum_{i \in B} \frac{\alpha_i}{V_{i1} - V_{i2}}, \quad (7)$$

where $\alpha_i = \rho I_i l_i^2$, subject to constraints (2), (4), (5)¹ and the following constraint

$$\frac{V_{i1} - V_{i2}}{I_i} \geq 0. \quad (8)$$

The constraint ensures that the current direction will not change during the optimization process.

¹Constraint (5) was not considered in [8].

- **Problem P2:** Assuming that all nodal voltages are fixed, the objective function becomes

$$f(\mathbf{I}) = \sum_{i \in B} \beta_i I_i, \quad (9)$$

where $\beta_i = \frac{\rho_i^2}{V_{i1} - V_{i2}}$, subject to (3), (5), (6), and the following fixed current direction constraint

$$\frac{I_i}{V_{i1} - V_{i2}} \geq 0. \quad (10)$$

Chowdhury showed that problem **P1** can be converted to an un-constrained convex programming problem and solved by the conjugate gradient method. **P2** is a linear programming problem. Therefore, solving **P** is to start with an initial feasible solution, then iteratively solve **P1**, then **P2**.

IV. NEW LINEAR-PROGRAMMING BASED ALGORITHM

The new method uses a sequence of linear programmings to solve the nonlinear programming problem **P1**. In this section, we present the method and prove that it always converges to the optimum solution of problem **P1**.

The basic idea is to linearize nonlinear objective function (7). To see this, we define branch voltage drop variable as $v_i = \text{sign}(I_i)(V_{i1} - V_{i2})$ for each branch i , where $\text{sign}(x) = 1$ if $x > 0$ and $\text{sign}(x) = -1$ if $x < 0$. Note that $v_i \geq 0$. Then in terms of $v_i, i = 1, \dots, b$, the objective function (7) can be expressed as

$$f(\mathbf{v}) = \sum_{i \in B} \frac{|\alpha_i|}{v_i}, \quad (11)$$

where $\mathbf{v} = \{v_1, v_2, \dots, v_b\}^T$. Suppose that we have an initial feasible solution \mathbf{v}^0 and corresponding \mathbf{v}^0 satisfying all the constraints. We then take the Taylor expansion of $f(\mathbf{v})$ around \mathbf{v}^0 and keep only the constant and linear terms. The resulting objective function is called $g(\mathbf{v})$,

$$g(\mathbf{v}) = f(\mathbf{v}^0) + \frac{\partial f(\mathbf{v}^0)}{\partial \mathbf{v}}(\mathbf{v} - \mathbf{v}^0) = \sum_{i \in B} \frac{2|\alpha_i|}{v_i^0} - \sum_{i \in B} \frac{|\alpha_i|}{v_i^0{}^2} v_i. \quad (12)$$

Instead of minimizing $f(\mathbf{v})$, we minimize $g(\mathbf{v})$ as long as these two functions satisfy the following property:

$$g(X) > g(Y) \implies f(X) > f(Y), \quad (13)$$

where \implies means *imply*. This requirement essentially says that as long as we reduce $g(X)$ we always can reduce $f(X)$.

To motivate our method, we first consider each individual term in the objective function (11), which has the following form $h(x) = c/x, x > 0$, where c is a constant and $c > 0$. Figure 1 draws function $h(x) = c/x$ with $c = 1$ and its linearized first-order Taylor expansion function $H(x)$ at expansion point $x_0 = 0.04$. We note that both $h(x)$ and $H(x)$ are monotonically decreasing functions in x in the range $(0, \infty)$ with the property that $h(x) > H(x)$.

Considering $f(\mathbf{v})$ and $g(\mathbf{v})$, we have the following two optimization scenarios:

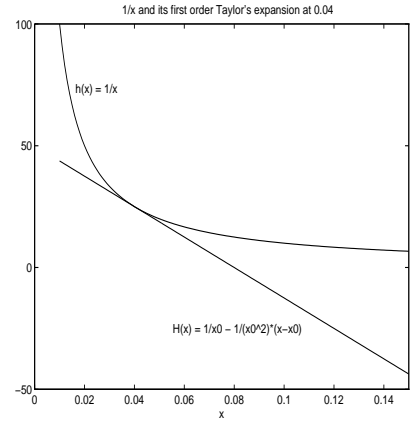


Fig. 1. $h(x) = 1/x$ and its first-order expansion at 0.04.

1. If all the branch voltage drops, v_i , increase after optimization, we have $f(\mathbf{v}^0) > f(\mathbf{v})$ and $g(\mathbf{v}^0) > g(\mathbf{v})$. Because all the terms in both $f(\mathbf{v}^0)$ and $g(\mathbf{v}^0)$ monotonically decrease as each v_i increases, property (13) is always satisfied.

2. If only some branch voltage drops increase and others decrease or stay unchanged, then property (13) may not be satisfied due to the fact that for $x < x_0$, $h(x)$ will increase very quickly, while $H(x)$ only increases linearly. As a result, we may end up with $f(\mathbf{v}) > f(\mathbf{v}^0)$ while $g(\mathbf{v}) < g(\mathbf{v}^0)$.

In this case, we can limit the solution space to the neighborhood of \mathbf{v}^0 such that property (13) holds by imposing the following constraint for each branch i :

$$\xi \cdot v_i^0 \leq v_i \leq (2 - \xi) \cdot v_i^0, \quad (14)$$

where ξ is called the *restriction factor*, $0 < \xi < 1$. As will be shown in Theorem 1, we can always satisfy property (13) by choosing \mathbf{v} to be sufficiently close to \mathbf{v}^0 (ξ is close enough to 1) as $g(\mathbf{v})$ is essentially the first-order approximation of $f(\mathbf{v})$.

On the other hand, an increase in any branch voltage drop $v_i, i \in \{1, \dots, b\}$ always decreases $f(\mathbf{v})$ and $g(\mathbf{v})$ according to scenario 1. This implies that the upper bound in (14) is redundant, and we can combine the solution space, where relation (13) holds in both scenarios, into a single space:

$$\xi \cdot v_i^0 \leq v_i. \quad (15)$$

In terms of nodal voltages, the linearized objective function and the restriction constraint can be rewritten as:

$$g(\mathbf{v}) = \sum_{i \in B} \frac{2\alpha_i}{(V_{i1}^0 - V_{i2}^0)} - \sum_{i \in B} \frac{\alpha_i}{(V_{i1}^0 - V_{i2}^0)^2} (V_{i1} - V_{i2}), \quad (16)$$

$$\xi \cdot \text{sign}(I_i)(V_{i1}^0 - V_{i2}^0) \leq \text{sign}(I_i)(V_{i1} - V_{i2}). \quad (17)$$

Note that constraint (17) does not necessarily require that nodal voltage $V_{ix}, i \in \{1, \dots, n\}$, be close to their initial values. Because constraint (17) already implies constraint (8), we have the following optimization problem, denoted as **P3**:

minimize (16):

$$g(\mathbf{V}) = \sum_{i \in B} \frac{2\alpha_i}{(V_{i1}^0 - V_{i2}^0)} - \sum_{i \in B} \frac{\alpha_i}{(V_{i1}^0 - V_{i2}^0)^2} (V_{i1} - V_{i2}),$$

subject to

- (2) : $V_j \geq V_{j,min}$ if node j is connected to a power pad,
 $V_j \leq V_{j,max}$ if node j is connected to a ground pad,
- (3) : $\frac{V_{i1} - V_{i2}}{I_i} \leq \frac{\rho l_i}{w_{i,min}}$,
- (4) : $|V_{i1} - V_{i2}| \leq \rho l_i \sigma$.
- (5) : $\frac{V_{i1} - V_{i2}}{l_i I_i} = \frac{V_{j1} - V_{j2}}{l_j I_j}$,
- (17) : $\xi \cdot \text{sign}(I_i)(V_{i1}^0 - V_{i2}^0) \leq \text{sign}(I_i)(V_{i1} - V_{i2})$.

Problem **P3** is a linear programming problem. For convenience, we use Γ to denote the feasible region of problem **P3** defined by (2), (3), (4), (5), and (17). We use Ω to denote the feasible region of problem **P1** as defined by constraints (2), (3), (4), (5), and (8). Clearly $\Gamma \subseteq \Omega$.

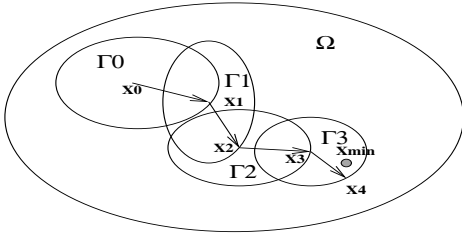


Fig. 2. An illustration of sequence of linear programmings.

The procedure for solving problem **P1** can be transformed to the problem of repeatedly choosing ξ and solving **P3** until the optimum solution is found. This sequence of linear programming process is illustrated in Fig. 2 in terms of solution space of problem **P1** (Ω) and solution spaces of problem **P3** (Γ_0 to Γ_n). X_{min} is the global minimum of convex problem **P1**. It shows how the new method approaches the global minimum by several linear programming processes iteratively.

The entire optimization procedure is summarized as follows:

New Power/Ground Network Optimization Algorithm

- 1) Analyze network G to obtain initial $\mathbf{V}^k, \mathbf{I}^k$ for $k = 0$.
- 2) Construct the minimum width constraints (3), current density constraints (4), equal width constraints (5), additional constraints (17) using \mathbf{I}^k .
- 3) Minimize $g(\mathbf{V}^k)$ subject to constraints (2), (4), (5), (3), and (17) by a sequence of linear programmings, record the result as \mathbf{V}_l^k , l begins from 1. If $f(\mathbf{V}_l^k) > f(\mathbf{V}_{l-1}^k)$, perform line search along the direction $\mathbf{d} = (\mathbf{V}_{l-1}^k - f(\mathbf{V}_l^k))$ until $f(\mathbf{V}_l^k) \leq f(\mathbf{V}_{l-1}^k)$. Record the result from the last iteration l as \mathbf{V}^{k+1} .
- 4) Construct the minimum width and its companion constraint (3), (5), and (10) using \mathbf{V}^{k+1} for each branch.

- 5) Minimize objective function (9) subject to the constraints (3), (5), (6), and (10) by linear programming and record the result as \mathbf{I}^{k+1} .
- 6) If $|f(\mathbf{V}^{k+1}, \mathbf{I}^{k+1}) - f(\mathbf{V}^k, \mathbf{I}^k)| < \epsilon$, ϵ is the termination criterion, then stop, otherwise set $k = k + 1$ and goto step 2.

For the new P/G optimization algorithm, we have the following theoretical result:

Theorem 1: There exists a ξ so that step 3 always converges to the global minimum in Ω .

The proof of this theorem can be found in the Appendix.

Although we show theoretically that given $g(\mathbf{V}_l^k) < g(\mathbf{V}_{l-1}^k)$ we can always find a ξ in step 3 such that $f(\mathbf{V}_l^k) < f(\mathbf{V}_{l-1}^k)$. But in practice, it is not very efficient to find such a ξ by repeatedly decreasing ξ and solving **P3** in case of $f(\mathbf{V}_l^k) \geq f(\mathbf{V}_{l-1}^k)$. In our implementation, we perform one-dimensional line search to find the solution point.

Specifically, given \mathbf{V}_l^k and \mathbf{V}_{l-1}^k , we define the search direction as $\mathbf{d}_l^k = \mathbf{V}_l^k - \mathbf{V}_{l-1}^k$. Line search finds an $\alpha \in [0, 1]$ such that

$$f(\alpha \mathbf{d}_l^k + \mathbf{V}_{l-1}^k) < f(\mathbf{V}_{l-1}^k), \quad (18)$$

$\alpha \mathbf{d}_l^k + \mathbf{V}_{l-1}^k$ becomes new \mathbf{V}_l^k for the next iteration. This can be accomplished by any line search algorithm. In our implementation, the golden section method [10] is used.

We note that a similar technique, called *successive linear programming (SLP)* [1], was first proposed by Griffith and Stewart to solve problems in oil and chemical industries [10]. A similar idea was also used by M. Sarrafzadeh, *et. al.*, to compute the best delay budget constraints for timing-driven placement [13].

V. PRACTICAL CONSIDERATIONS AND IMPLEMENTATION ISSUES

In this section, we describe some practical considerations on how to apply the proposed method to optimize power/ground networks in practice.

- **Algorithm scalability.** In practice, the number of linear programmings needed to reach the optimum solution is only a few. Thus the time complexity of our method is proportional to that of linear programming. It is known that linear programs can be solved in polynomial time using the interior point method [1]. This makes our method very promising for optimizing very large P/G networks.
- **Input data scaling.** For practical P/G networks, the module currents are usually in the range of $1 \times 10^{-9} A$. Branch currents and branch voltages could become very small without using scaling. This would cause some numerical problems for linear program solvers. In our implementation, scaling is used.
- **Converting power networks to ground networks.** Power networks should be transferred into ground networks to further improve the numerical stability. This is due to the fact that voltage drops close to zero can be represented more precisely than the voltage drops close to any other values. For example, the voltage drop of 2.5×10^{-5} has to be represented by 4.999975 if the source voltage is

5 volt. If we apply data scaling by multiplying 10^5 to all the voltage drops, 2.5×10^{-5} become 2.5 which are more linear-solver friendly than 4999975. As 499975 can easily lead to ill-conditions or round errors in solving linear equations. It can be shown that a power network can be transferred into a ground network by using the following transformation rules:

1. short-circuit all the VDD pads to the ground,
 2. inverse the directions of all the independent current sources.
- **Zero branch voltages.** The branch voltage v_i in objective function (11) can be zero or take a very small numerical value. In this case, we just simply ignore the branch (and its incident nodal voltages and branch currents) in the objective function and all the constraints. The corresponding branch will take the minimum width after the optimization.

VI. EXPERIMENTAL RESULTS

A CAD tool for P/G network optimization has been developed based on the proposed sequence-of-linear-programming method. For comparison, Chowdhury's conjugate gradient method [8] has also been carefully implemented². A set of P/G networks with ten to more than ten thousand segments has been tested. All experiments are performed on a SUN workstation with 296MHz clock rate.

Table I compares the result of the new algorithm with that of the conjugate gradient method. No equal width constraints are considered here since Chowdhury's conjugate gradient method cannot handle these constraints well. In Table I, columns 1 to 3 list, respectively, the P/G network name, the number of nodes in the P/G network, (*#node*), and the number of branches, (*#bch*). Notice that name *pg100x100* means that the circuit consists of 100 rows and 100 columns P/G strips. So the sizes of the circuits in terms of nodes are approximately equal to *#rows* \times *#columns* as shown in column 2. The number of iterations (*#iter*) (solving **P1-P2**), CPU time in seconds (*CPU*), and the reduced chip area of the original area in percentage (*area reduced (%)*) are reported in columns 4, 5 and 6 for the new algorithm and columns 7, 8 and 9 for the conjugate gradient method. For example, for P/G network *pg20x20*, the new method reduces the chip area used by 90.6%, while the conjugate gradient method reduces the chip area used by 85.3%. Note that the area improvement strongly depends on the original layouts.

We have the following observations:

- For large P/G networks *pg3x500*, *pg300x10*, *pg100x100*, the conjugate gradient method finds solutions that use chip areas much more than that of the new method.
- The new algorithm is orders of magnitude faster than the conjugate gradient method.
- We have observed that for all the P/G networks tested, with one iteration, the new algorithm is able to reduce most of the chip area that can be reduced, i.e., finds a solution that

is very close to the optimum. Figure 3 shows how the objective function decreases with the number of iterations for an example network.

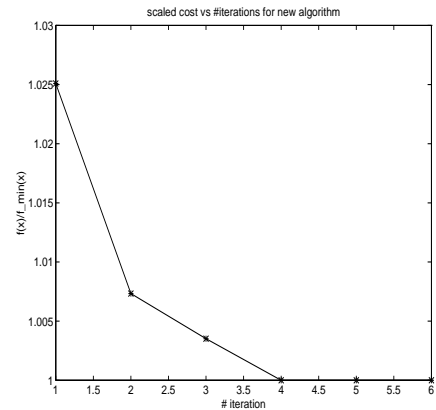


Fig. 3. The cost reduction with the number of iterations.

Analysis:

- Theoretically, both the conjugate gradient method and the sequence-of-linear-programming method should converge to an optimal solution. However, in practice, due to the numerical problem inherent in the conjugate gradient method, the conjugate directions may deteriorate during the process of optimization such that the algorithm gets stuck at a solution far away from the optimum. In our implementation, we reinitialize the direction vector if no improvement can be made along the present direction. This process is repeated until the reinitialized direction cannot further reduce the cost function.
- The way the penalty function is constructed also affects the solution quality of the conjugate gradient method. After solving problem **P2** for branch currents by linear programming, some widths of P/G segment may be reduced to a minimum value. Those segments will lead to the infinite penalty cost and the infinite conjugate direction vector, the whole process will stall after only one **P1-P2** iteration. Therefore, it is hard for the conjugate gradient method to find the optimal solution. As a remedy, in our implementation, we slightly increase the required minimum width value when solving **P2**.
- In the experiments above, the restriction factor ξ is set to 0.85. Recall that the feasible region Γ for linear program **P3** is controlled by ξ . The closer ξ to 1, the smaller the region Γ , and the better $g(\mathbf{V})$ approximates $f(\mathbf{V})$. This implies that the total number of linear programming iterations (solving **P1-P3**) will increase, but the chance to find the minimum solution of the original problem increases. On the other hand, if we reduce ξ closer to 0, the feasible region Γ of problem **P3** enlarges. Then the linearized function $g(\mathbf{V})$ may not be able to approximate the original function $f(\mathbf{V})$ well. As a result, the sequence of linear programmings may converge to a solution with the cost higher than the optimum one. This observation has been confirmed by the experiment on the example network *pg4x4* without using line search in step 3 as shown in Figs. 4

²In fact, our research was motivated by our initial attempt in applying the conjugate gradient method for power/ground network optimization in an industry setting.

TABLE I
COMPARISON OF THE NEW ALGORITHM AGAINST THE CONJUGATE GRADIENT METHOD.

P/G network	#node	#bch	new algorithm			conjugate gradient			speedup
			#iter	CPU time	area reduced(%)	#iter	CPU time	area reduced(%)	
pg4x4	17	23	2	0.4	95.1	12	117.3	95.0	239.3
pg20x20	402	439	3	4.33	90.6	24	17554.1	85.3	4082.3
pg3x500	1502	1505	2	64.6	52.1	22	9035.5	29.2	139.9
pg300x10	3002	3599	2	237.6	93.7	25	10811.7	85.9	45.5
pg100x100	10002	10199	2	1801.8	80.7	24	52597.1	49.6	29.2

and 5.

In addition to Γ , the number of linear programs in **P3** also depends on the initial solutions as shown in Fig. 1. But for the given P/G networks, we find that it takes a few (less than 10) linear programs to reach a solution for all the cases. Therefore, the new algorithm converges very quickly.

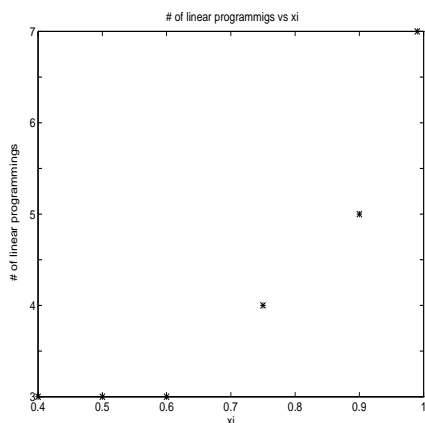


Fig. 4. The number of linear programs versus $\xi (xi)$.

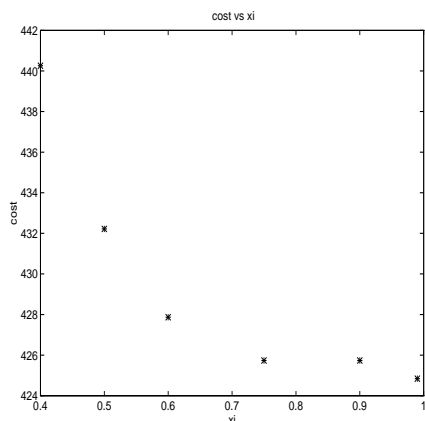


Fig. 5. The final cost versus $\xi (xi)$.

Table II describes the results of applying the new algorithm to the same set of P/G networks but with practical equal-width constraints. Here we require widths of all the wire segments along the same chain to be equal. The number of such constraints, $\#eq-consts$, is listed in the second column for each network. Not surprisingly, we can see from the table that the area reduced may not be as much as we can achieve without

equal-width constraints. In comparison to the instances without equal-width constraints, the CPU time used can be more (*pg100x100*) or less (*pg300x10*). The reason for using less CPU time as in case of *pg300x10* is due to the reduction of number of iterations in solving **P3** since a reduced search space is considered. The reason for more CPU time as in case *pg100x100* is due to more constraints in each linear program and more CPU time for each iteration.

VII. CONCLUSIONS AND FUTURE WORK

A sequence-of-linear-programming based method has been proposed and implemented for determining the widths of wire segments in a power/ground network so that the chip area required by the power/ground network is minimized while ensuring IR voltage drops and electromigration constraints. We have shown theoretically that the new method is capable of finding the solution as good as that by the best known method based on conjugate gradient scheme. Experimental results have demonstrated that the proposed method is orders of magnitude faster than the best-known method with constantly *better* quality solutions.

In this work, we model P/G networks as resistor-only networks. We notice that capacitive and inductive induced transient voltage fluctuations are major concerns for P/G networks in current and future technologies. However, we view our P/G optimization technique as one essential step toward designing robust power delivery networks. It was shown in [2] that transient voltage noise on some P/G segments can be efficiently suppressed by adding decoupling capacitors (decaps) around those P/G wires. Such decap allocation scheme will make the resulting P/G grids more like resistive networks as decaps serve as low-pass filters. The IR drops due to the DC components of the voltages on the P/G networks and electromigration related current density problems have to be addressed by wire sizing or topology changes. Further work will be extended towards P/G network optimization with capacitive and inductive parasitics driven by time-varying current sources.

Acknowledgment: The authors wish to thank Dr. Li-Peng Yuan, Dr. Dragos Lungeanu of Synopsys Corporation, and Professor Ernest Kuh of University of California, Berkeley for several helpful discussions on power/ground network design.

APPENDIX

Let $f(\mathbf{x})$ be the objective function of problem **P1** and $g(\mathbf{x})$ be the linearized version of $f(\mathbf{x})$. Consider an initial starting point

TABLE II
EXPERIMENTAL RESULTS OF RUNNING THE NEW ALGORITHM WITH EQUAL WIDTH CONSTRAINTS.

P/G network	#eq-consts	#iter	CPU	percentage of area reduced
pg4x4	12	2	0.3	50.0
pg20x20	56	2	5.2	90.3
pg3x500	503	2	366.9	51.1
pg300x10	200	2	198.4	93.7
pg100x100	397	2	5154.2	80.6

\mathbf{x}_0 and a solution point \mathbf{x} found by solving LP problem **P3**.

Let Γ denote the feasible region of problem **P3** defined by (2), (3), (4), and (17). Since Γ is a function of restriction factor ξ defined in (17), we also rewrite it as $\Gamma(\xi)$.

We begin our proof by first proving the following lemma.

Lemma 1: For each \mathbf{x}_0 , there exists a ξ and a nonempty vicinity $\Gamma(\xi)$ of \mathbf{x}_0 such that if $g(\mathbf{x}) < g(\mathbf{x}_0)$, $\mathbf{x} \in \Gamma(\xi)$, then $f(\mathbf{x}) < f(\mathbf{x}_0)$.

Proof: Let $\mathbf{d} = \mathbf{x} - \mathbf{x}_0$ be the moving direction. According to the Taylor expansion, we have

$$f(\mathbf{x}_0 + \alpha \mathbf{d}) = f(\mathbf{x}_0) + \alpha \nabla f(\mathbf{x}_0) \mathbf{d} + o(\alpha) \quad (19)$$

where $o(\alpha)$ is a lower order infinity than α , i.e.

$$\lim_{\alpha \rightarrow 0} \frac{o(\alpha)}{\alpha} = 0.$$

Notice that $g(\mathbf{x}) = g(\mathbf{x}_0) + \nabla g(\mathbf{x}_0)(\mathbf{x} - \mathbf{x}_0)$ and $g(\mathbf{x}) < g(\mathbf{x}_0)$ as given by Lemma 1, so

$$g(\mathbf{x}_0) - g(\mathbf{x}) = -\nabla g(\mathbf{x}_0)(\mathbf{x} - \mathbf{x}_0) > 0, \quad (20)$$

$$\nabla g(\mathbf{x}_0)(\mathbf{x} - \mathbf{x}_0) = \nabla g(\mathbf{x}_0) \mathbf{d} < 0. \quad (21)$$

Rewriting (19), we have

$$f(\mathbf{x}_0 + \alpha \mathbf{d}) = f(\mathbf{x}_0) + \alpha (\nabla f(\mathbf{x}_0) \mathbf{d} + \frac{o(\alpha)}{\alpha}). \quad (22)$$

It is easy to see that we can always select a small enough α such that

$$\nabla f(\mathbf{x}_0) \mathbf{d} + \frac{o(\alpha)}{\alpha} < 0. \quad (23)$$

Hence

$$f(\mathbf{x}_0 + \alpha \mathbf{d}) < f(\mathbf{x}_0). \quad (24)$$

As we can make ξ as close to one as possible, thus $|\mathbf{d}|$ as small as possible, we can always obtain a ξ so that α can be 1, i.e. $f(\mathbf{x}_0 + \mathbf{d}) < f(\mathbf{x}_0)$. If $\xi = 1$, there still exists a nonzero \mathbf{d} such that $g(\mathbf{x}_0 + \mathbf{d}) < g(\mathbf{x}_0)$. Therefore, it must follow that $f(\mathbf{x}_0 + \mathbf{d}) < f(\mathbf{x}_0)$ as both $f(\mathbf{x})$ and $g(\mathbf{x})$ are monotonically decreasing functions in \mathbf{x} . Lemma 1 is proved.

Now, we are ready to prove Theorem 1.

Theorem 1 *There exists a ξ so that step 3 always converges to the global minimum in Ω .*

Proof: For function $f(\mathbf{x}) = \sum_{i=1}^n \frac{1}{x_i}$, the truncated linear Taylor expansion around \mathbf{x}_0 is $g(\mathbf{x}) = \sum_{i=1}^n (\frac{1}{x_{0i}} - \frac{x_i - x_{0i}}{x_{0i}^2})$. According to Lemma 1, given an initial point $\mathbf{x}_0 = \mathbf{V}_l^k$, one can always find a non-empty vicinity of \mathbf{x}_0 , by increasing ξ close

enough to 1 such that minimizing the linear expansion g at \mathbf{V}_{l+1}^k also decreases the original function f .

Hence a decreasing sequence $\{f(\mathbf{V}_1^k), f(\mathbf{V}_2^k), \dots, f(\mathbf{V}_l^k)\}$ is generated and guarantees to converge to a local minimum. Since $f(X)$ is a convex function, the local minimum is also the global minimum, therefore step 3 in the new algorithm will converge to the global minimum in Ω .

REFERENCES

- [1] M. S. Bazaraa, H. D. Sherali and C. M. Shetty, *Nonlinear Programming: Theory and Algorithm*, John-Wiley & Sons, New York, 1993.
- [2] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Reading, Massachusetts: Addison-Wesley Publishing Company, 1990.
- [3] J. R. Black, "Electromigration failure modes in aluminum metallization for semiconductor devices," *Proc. of IEEE*, vol. 57, pp. 1587-1597, Sept. 1996.
- [4] R. K. Brayton, G.D. Hatchel and A. Sangiovanni-Vincentelli, "A survey of optimization techniques for integrated circuit design," *Proc. of IEEE*, vol. 69, no. 10, pp. 1334-1362, Oct. 1981.
- [5] E. K. P. Chong and S. H. Zak, *An introduction to optimization*, John-Wiley & Sons, New York, 1996.
- [6] S. Chowdhury and M. A. Breuer, "Minimal area design of power/ground nets having graph topologies," *IEEE Trans. Circuits and Systems*, vol. CAS-34, no. 12, pp. 1441-1451, Dec. 1987.
- [7] S. Chowdhury and M. A. Breuer, "Optimum design of IC power/ground networks subject to reliability constraints," *IEEE Trans. Computer-Aided Design*, vol. 7, no. 7, pp. 787-796, July 1988.
- [8] S. Chowdhury, "Optimum design of reliable IC power networks having general graph topologies," in *Proc. 26th ACM/IEEE Design Automation Conf.*, pp. 787-790, 1989.
- [9] R. Dutta and M. Marek-Sadowska, "Automatic sizing of power/ground (p/g) networks VLSI," in *Proc. 26th ACM/IEEE Design Automation Conf.*, pp. 783-786, 1989.
- [10] R. E. Griffith and R. A. Stewart, "A nonlinear programming technique for the optimization of continuous process systems," *Management Science*, no. 7, pp. 379-392, 1961.
- [11] T. Mitsuhashi and E. S. Kuh, "Power and ground network topology optimization," in *Proc. 29th ACM/IEEE Design Automation Conf.*, pp. 524-529, 1992.
- [12] C. H. Papadimitriou and K. Steiglitz, *Combinatorial Optimization Algorithms and Complexity*, Prentice-Hall Inc., New York, 1992.
- [13] M. Sarrafzadeh, D. A. Knol, and G.E. Tellez, "A delay budgeting algorithm ensuring maximum flexibility in placement", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, no. 11, pp. 1332-1341, Nov. 1997.
- [14] X.-D. Tan, C.-J. Shi, D. Lungeanu, J.-C. Lee, and L.-P. Yuan, "Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings", in *Proc. 36th ACM/IEEE Design Automation Conf.*, pp. 78-83, 1999.