HiPRIME: Hierarchical and Passivity Preserved Interconnect Macromodeling Engine for RLKC Power Delivery

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Abstract

This paper proposes a general hierarchical analysis methodology, HiPRIME, to efficiently analyze RLKC power delivery systems. After partitioning the circuits into blocks, we develop and apply the IEKS (Improved Extended Krylov Subspace) method to build the multi-port Norton equivalent circuits which transform all the internal sources to Norton current sources at ports. Since there are no active elements inside the Norton circuits, passive or realizable model order reduction techniques such as PRIMA can be applied. The significant speed improvement, 700 times faster than Spice with less than 0.2% error and 7 times faster than a state-of-the-art solver, InductWise, is observed. To further reduce the top-level hierarchy runtime, we develop a second-level model reduction algorithm and prove its passivity.

I. Introduction

With the UDSM (Ultra Deep Sub-Micron) technology, several features of today's chips (higher operating frequencies, larger number of transistors, smaller feature size and lower power supply voltage) have pushed the power delivery noise analysis onto the designers' list of high priority concerns [1], [2], [3], [4]. Basically, the power delivery noise consists of IR drop, Ldi/dt drop and resonance fluctuations. The IR drop has been widely discussed and extensively studied in the literatures [5], [6] and [7]. Due to the roaring clock frequency, increasing current consumption, and even the clock gating feature, Ldi/dt noise is quickly emerging as another power fluctuation concern [6]. Power delivery noise causing the power voltage to deviate from the ideal value can severely degrade the performance and even make the gate function erroneously. Therefore, the extensive analysis of RLKC power delivery systems is required to ensure them to meet the targeted performance and reliability goals.

Generally speaking, one of the major difficulties for the power delivery analysis is size explosion. Tens of millions of devices and parasitics are required to be modeled and simulated over a long time period.

However, it is computationally expensive to simultaneously simulate all transistors with the power delivery structure. To enhance the simulation speed, it has been proposed to decouple the power delivery structure simulation and transistors' simulation [6]. First, the current profiles of transistors can be estimated by several current extraction methods [8], [9]. After that, the power delivery network is modeled by a suitable RLC circuit attached with many current sources. In this way, the simulation can be effectively done since there are fewer elements in the circuit, and the RLC circuit can be simulated with one LU decomposition. However, due to the large size and grid nature of linear circuits, the traditional circuit simulation engines such as Spice [10] cannot fulfill the demanding task in a time efficient manner. For this reason, the hierarchical simulation technique has been applied by [6] to speed up the power delivery network simulation.

The model order reduction technique is another efficient way which can be utilized to speed up the circuit analysis [11], [12], and has been widely studied and improved over the last decade [5], [13], [14], [15], [16]. Starting from AWE [13] (Asymptotic Waveform Evaluation) to PRIMA [16] (Passive Reduced-order Interconnect Macromodeling Algorithm), model order reduction techniques have been successfully extended to consider the inductance effects with reasonable accuracy. Later, an extended Krylov subspace method, EKS [5] (Extended Krylov Subspace), has been developed to simulate large scale power delivery circuits with many PWL (piece wise linear) current sources. To resolve the source waveform modeling issues, EKS need to perform the moment shifting procedure to recover the proper moments.

In this paper, we utilize these two techniques, hierarchical analysis and model order reduction, to develop a novel hierarchical power delivery analysis engine. The contributions of our method are listed as follows. First, we establish a novel hierarchical power delivery macromodeling methodology, which integrates the multiple port Norton equivalent theorem [17] with the model order reduction algorithm to generate compact and accurate model, and achieve significant runtime improvements. Then, we enhance the EKS method such that it no longer needs to perform moment shifting for source waveform modeling.

Therefore, the highly accurate simulation results are observed. Finally, to further reduce the runtime, we develop a multiple level passive model reduction algorithm and prove its passivity.

The remainder of this paper is organized as follows. Section II introduces the basic power delivery network modeling, circuit formulations, and the concepts of model order reduction. Section III presents our hierarchical and passive order-reduced macromodeling methodology. Section IV shows several experimental results. Finally, Section V concludes the work.

II. Preliminary

The RLKC elements are applied to model the power delivery system as shown in Fig. 1. To reduce the simulation runtime, we decouple the linear simulation from the nonlinear simulation [6]. Once the nonlinear simulation is done, the current sources and capacitors are used to model the gate current consumption, and diffusion and gate capacitance, respectively. Therefore, the task of power grid analysis is simplified to simulate a linear RLKC network with linear time-varying current sources, and measure the voltage drop at each grid.

A linear RLKC circuit can be represented as a set of circuit equations by using the MNA (modified nodal analysis) method as follow

$$\mathbf{G}x + \mathbf{C}\frac{d}{dt}x \;=\; \mathbf{B}u, \tag{1}$$

where x is the variable vector consisting of nodal voltages, and the currents flowing through the inductor and voltage sources, u denotes the vector of the port voltage sources and internal current sources, $\mathbf{G}$ is the conductance matrix, and $\mathbf{C}$ is the susceptance matrix. They can be rewritten as

$$\mathbf{G} \;=\; \begin{bmatrix} \mathbf{N} & \mathbf{E} \\ -\mathbf{E}^T & \mathbf{0} \end{bmatrix}, \tag{2}$$

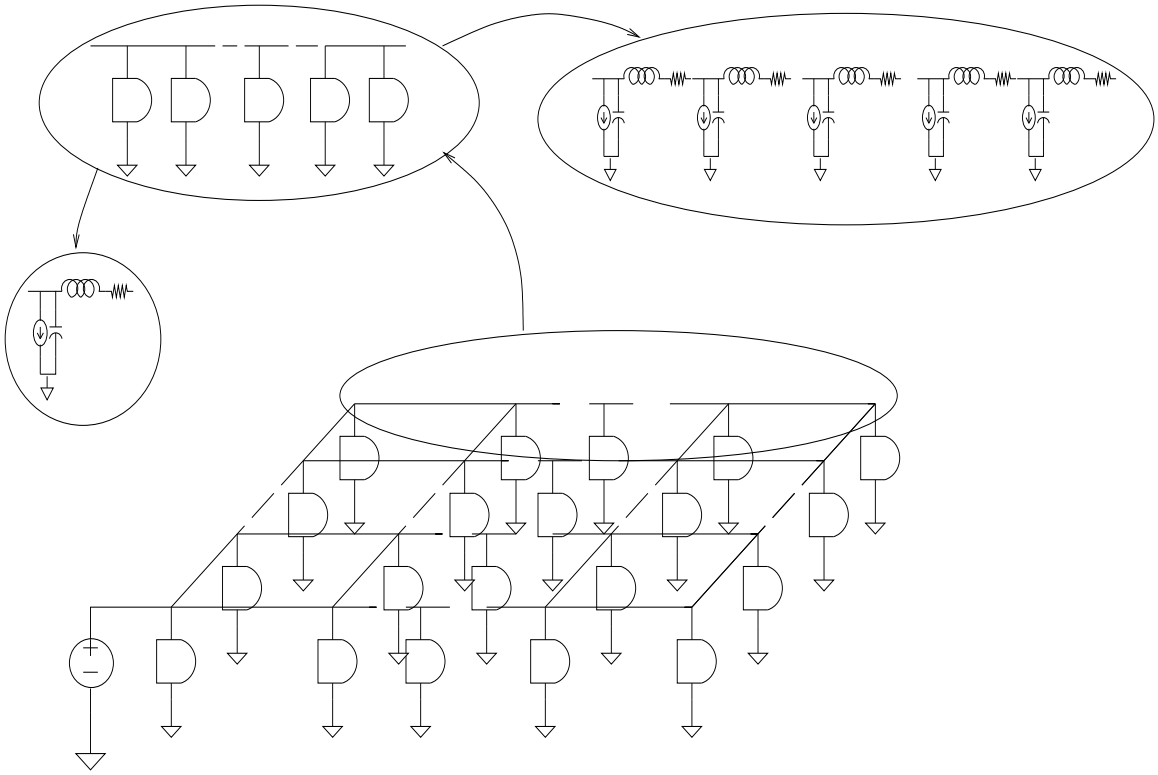

Fig. 1. Modeling of the power delivery network

$$\mathbf{C} \;=\; \begin{bmatrix} \mathbf{Q} & \mathbf{0} \\ \mathbf{0} & \mathbf{H} \end{bmatrix}, \tag{3}$$

The **N**, **Q**, and **H** contain the stamping of resistors, capacitors and inductors. Note that **H** contains both self and mutual inductance (K elements). **E** corresponds to the MNA current variables' contribution to the KCL (Kirchhoff's Current Law) equations. Circuit equations as shown in Equation (1) can be transformed to the $s-$ domain by the Laplace transformation

$$\mathbf{Gx} + s\mathbf{Cx} \;=\; \mathbf{Bu}. \tag{4}$$

The model order reduction generates an analytical model which is a compact description of the original circuit by matching its moments or poles. To illustrate the idea of moment matching, we expand both

side of the Equation (4) into a Taylor series around zero frequency

$$(\mathbf{G} + s\mathbf{C})(m_0 + m_1 s + m_2 s^2 + \cdots) \;=\; \mathbf{B}(u_0 + u_1 s + u_2 s^2 + \cdots), \tag{5}$$

where m_i and u_i, the coefficients of the i_{th} term in the Taylor series, are the i_{th} moment of $\mathbf{x}$ and $\mathbf{u}$ respectively. The basic idea of moment matching is to represent the finite, unknown moments of the left hand side of the above equation in terms of the known moments of the right hand side. During the moment matching process, PRIMA uses impulse sources to preserve the input-output transfer characteristics. The impulse sources are constants in the frequency domain. Therefore, the Taylor expansion becomes to

$$(\mathbf{G} + s\mathbf{C})(m_0 + m_1 s + m_2 s^2 + \cdots) \;=\; \mathbf{B}u_0. \tag{6}$$

The above equation produces an iterative relationship between the moments of $\mathbf{x}$, and $\mathbf{u}$: $\mathbf{G}m_0 = \mathbf{B}u_0$, $\mathbf{G}m_i + \mathbf{C}m_{i-1} = 0$. This explicit moments matching method is seldom used because it has numerical stability problem, especially in the higher order iterations. To avoid the numerical errors, a set of orthogonal bases is built to span a subspace which is the same one spanned by the finite moments of $\mathbf{x}$. The set of the above orthogonal bases can be represented as a matrix $\mathbf{V}$ which is equivalent to the Krylov subspace of ($\mathbf{A} = -\mathbf{G}^{-1}\mathbf{C}$, $\mathbf{R} = \mathbf{G}^{-1}\mathbf{B}$), and is defined as $K_q(\mathbf{A}, \mathbf{R}) = colsp(\mathbf{R}, \mathbf{AR}, \mathbf{A}^2\mathbf{R}...\mathbf{A}^{q-1}\mathbf{R})$. The dimension of the original circuit ($\mathbf{G}$,$\mathbf{C}$,$\mathbf{B}$) is reduced because the rank of $\mathbf{V}$ is much smaller than that of the original matrix $\mathbf{A}$. The order-reduced model can be obtained by projecting the original model ($\mathbf{G}$,$\mathbf{C}$,$\mathbf{B}$) onto the Krylov subspace, $K_q(\mathbf{A}, \mathbf{R})$, by using the congruent transformation. The system matrices of the reduced system are denoted as $\widetilde{\mathbf{G}} = \mathbf{V}^T\mathbf{G}\mathbf{V}$, $\widetilde{\mathbf{C}} = \mathbf{V}^T\mathbf{C}\mathbf{V}$ and $\widetilde{\mathbf{B}} = \mathbf{V}^T\mathbf{B}$. This compact model can be represented by the following MNA equation in the time domain,

$$\widetilde{\mathbf{G}}\widetilde{x} + \widetilde{\mathbf{C}}\frac{d}{dt}\widetilde{x} \;=\; \widetilde{\mathbf{B}}u. \tag{7}$$

III. Hierarchical and Passive Order-Reduced Macromodeling

Our hierarchical and passive model order reduction engine consists of three steps. First, the power delivery networks are partitioned into multiple blocks. Each block may contain RLKC interconnect networks and many internal switching currents. Second, the Norton equivalent order-reduced model for each block is constructed by three phases. Phase 1 is to find the passive order-reduced model for the RLKC interconnect networks of each block. Phase 2 is to calculate the Norton equivalent currents of the internal current sources at each block. Phase 3 attaches those Norton equivalent currents at the ports of the order-reduced RLKC model. Finally, an integration algorithm is developed to integrate those macromodels, and the higher level model order reduction can be performed when necessary.

The outline, and flowchart of the proposed algorithm are shown in Fig. 2 and Fig. 3, respectively. The step $A2.1$, $A2.2$ and $A3$ shown in Fig. 2 are discussed in the following subsections.

Algorithm: HiPRIME (Hierarchical and Passivity Preserved Interconnect Macromodeling Engine)
A1. Partition the given circuit into multiple blocks
A2. For each block, its multi-port Norton equivalent order reduced circuit is generated by the following procedure:
- **A2.1** Set all the active sources to zeros and perform passive model order reduction for the linear circuit using any passivity guaranteed model reduction algorithm such as PRIMA.
- **A2.2** Activate all sources and short all the ports nodes to ground and find out the Norton equivalent source at each port by IEKS or SPICE simulation.
- **A2.3** Form the Norton equivalent circuit by attaching the Norton equivalent source at each port to the reduced circuit generated by **Step A2.1**.

A3. Form the integrated circuit by combining all reduced modules. Perform the higher level model order reduction by using IEKS or PRIMA when necessary.

Fig. 2. HiPRIME Algorithm

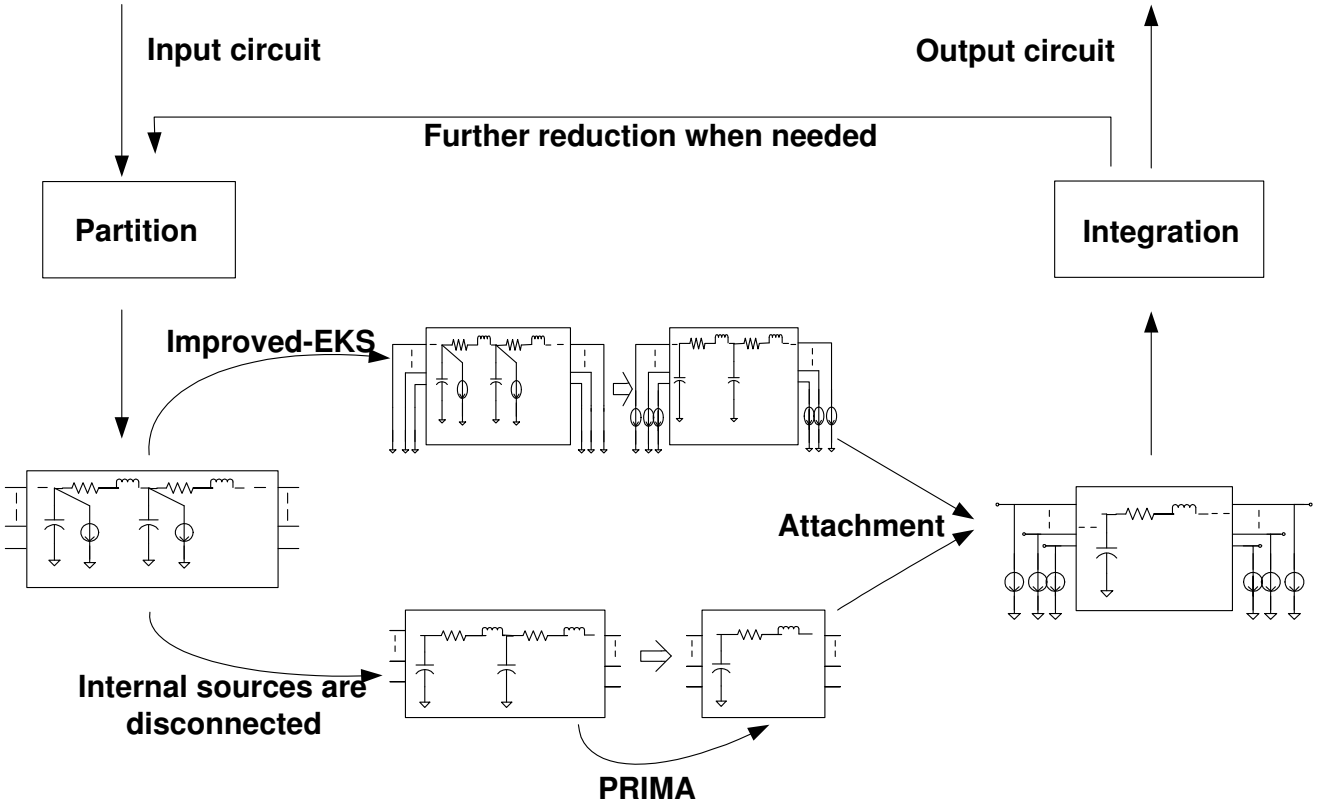

Fig. 3. Flowchart for the hierarchical and passivity preserved interconnect macromodeling engine

A. Passive Reduced-Order Macromodeling of RLKC Networks

After the power delivery network is partitioned into multiple blocks, each block may contain passive RLKC interconnects and internal switching current sources. In order to obtain a passive order-reduced model, all the internal current sources are disconnected to make this block a passive RLKC network. The effect of those current sources on grid voltages will be considered later. We may apply a conventional passive model order reduction algorithm, such as PRIMA, to each block. Let the MNA equation for the RLKC interconnect network of the i_{th} block be

$$\mathbf{G}_i x_i + \mathbf{C}_i \frac{d}{dt} x_i \quad = \quad \mathbf{B}_i u_i, \tag{8}$$

where u_i is the port voltage vector of the i_{th} block. PRIMA constructs a transfer matrix $\mathbf{V}_i$, and transfers the $\mathbf{G}_i$,$\mathbf{C}_i$ and $\mathbf{B}_i$ into $\widetilde{\mathbf{G}}_i, \widetilde{\mathbf{C}}_i$ and $\widetilde{\mathbf{B}}_i$ whose dimensions are reduced. The compact MNA equation of the

reduced block is

$$\widetilde{\mathbf{G}}_i\widetilde{x}_i + \widetilde{\mathbf{C}}_i\frac{d}{dt}\widetilde{x}_i \;\; = \;\; \widetilde{\mathbf{B}}_i u_i. \tag{9}$$

One advantage of model order reduction after partition is that the size of the circuit handled by the model order reduction algorithm is much smaller. Therefore, the limit of memory might be eased. It also makes parallel order reduction for different blocks possible, and the speed of analysis can be improved. Furthermore, each reduced block is a marcomodel which means that it can be reused to save the runtime. For example, if one of the blocks has been modified, HiPRIME only need to regenerate the reduced model of this block. However, the flat method need to regenerate the reduced model from scratch.

B. Efficient Way of Finding the Norton Equivalent Current

In this section, we consider the effects of the internal current sources ignored in the previous procedure. The Norton equivalent theory [17] is utilized to find out the equivalent current source at each port, and used to replace all the internal current sources so that the port responses of each block are preserved. To distinguish the port voltage sources from the internal current sources, the Equation (8) can be modified as

$$\mathbf{G}_i x_i + \mathbf{C}_i\frac{d}{dt}x_i \;\; = \;\; \left[\begin{array}{cc} \mathbf{B}_i & \mathbf{B}'_i \end{array}\right] \left[\begin{array}{c} v_i \\ \\ i_{gi} \end{array}\right], \tag{10}$$

where v_i, and i_{gi} denote the independent voltage sources and the internal switching current sources in the i_{th} block respectively. The $\mathbf{B}_i$, and $\mathbf{B}'_i$ denote the positions of the voltage sources and the current sources relative to the whole network. The procedure of calculating the equivalent current sources at the ports is illustrated in Fig. 4. The port currents, with the port voltages set to zeros, are the Norton equivalent current sources, and the port currents can be obtained by $i_{Ni} = \mathbf{B}_i^T x_i$. Several methods can be applied to solve Equation (10) with the voltage sources v_i set to zeros. In our approach, we develop the IEKS

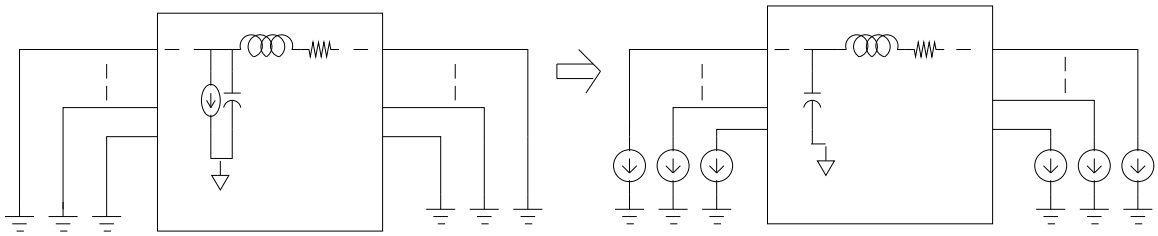

Fig. 4. Finding the equivalent current of internal sources

method, an improved version of EKS such that no moment shifting needed, to solve Equation (10). The description of IEKS is presented in the next two sessions.

B.1 Improved Extended Krylov Subspace

Developed by Janet, et al. at [5], EKS directly calculates the orthogonalized moments of the response when multiple sources are turned on at the same time. Therefore, unlike PRIMA whose runtime is heavily dependent on the number of ports, the runtime of EKS is independent of that. The EKS models an independent PWL source as a sum of delayed ramps in the Laplace domain,

$$u(s) \quad = \quad \frac{1}{s^2} \sum_{i=0}^{K} r_i \exp(-\beta_i s). \tag{11}$$

This expression contains $1/s$, and $1/s^2$ terms. Unfortunately the traditional Krylov subspace methods start the moment matching from the 0_{th} moment. Therefore, EKS need to extend the Krylov subspace by shifting the moments toward right in the frequency spectrum. This moment shifting in EKS is tedious and error-prone. We develop an improved moment calculation method which ensures that the -1_{st} and -2_{nd} order moments are all zeros for any arbitrary finite time PWL waveform, and hence the moment shifting process can be removed. Since for simulation purpose we are only interested in a specific time period, the finite-time assumption is quite general. We believe this procedure is numerically more sound than the original EKS method.

IEKS Moments Calculating Algorithm

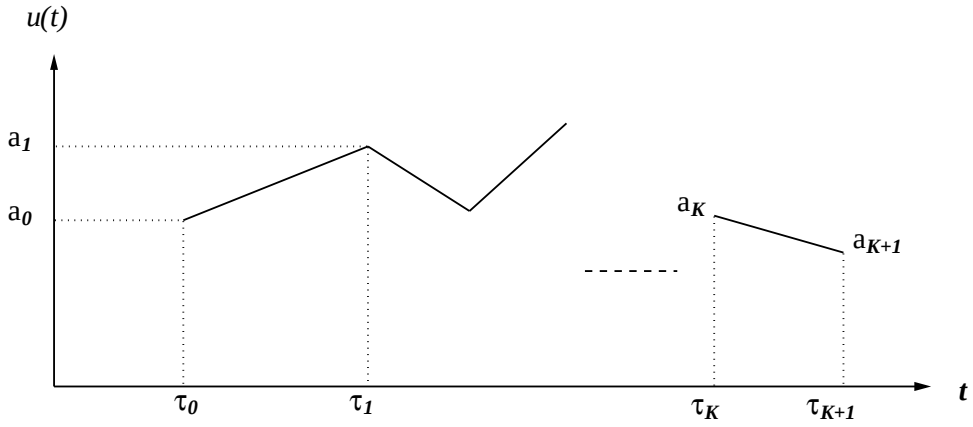

Fig. 5. Waveform of the source

Given a finite-time PWL source $u(t)$ as shown in Fig. 5, $u(t)$ can be written as

$$u(t) = \sum_{i=0}^{K} \left\{ [a_i + \gamma_i(t-\tau_i)]\, \mathrm{E}_{(\mathrm{t}-\tau_\mathrm{i})} - [\mathrm{a_{i+1}} + \gamma_\mathrm{i}(\mathrm{t}-\tau_{\mathrm{i+1}})]\, \mathrm{E}_{(\mathrm{t}-\tau_{\mathrm{i+1}})} \right\} \tag{12}$$

where $\gamma_i = (a_{i+1} - a_i)/(\tau_{i+1} - \tau_i)$ is the slope of line segment between time τ_i and τ_{i+1}, and $\mathrm{E}_{(\mathrm{t}-\tau_\mathrm{i})}$ is an unit-step function with delay τ_i. By taking the Laplace transform of Equation (12) and expanding the transform to its Taylor expansion, we have

$$\mathcal{L}\{u(t)\} = \frac{1}{s^2} \sum_{i=0}^{K} \left\{ a_i s \sum_{l=0}^{\infty} (-1)^l \frac{\tau_i^l}{l!} s^l + \gamma_i \sum_{l=0}^{\infty} (-1)^l \frac{\tau_i^l}{l!} s^l - a_{i+1} s \sum_{l=0}^{\infty} (-1)^l \frac{\tau_{i+1}^l}{l!} s^l - \gamma_i \sum_{l=0}^{\infty} (-1)^l \frac{\tau_{i+1}^l}{l!} s^l \right\}. \tag{13}$$

Let $\tilde{u}_i$ denote the coefficient of the s^i term. The Taylor expansion of $\mathcal{L}(u(t))$ can be represented as

$$\mathcal{L}\{u(t)\} = \left\{ \tilde{u}_{-2} s^{-2} + \tilde{u}_{-1} s^{-1} + \tilde{u}_0 + \tilde{u}_1 s + \tilde{u}_2 s^2 + \cdots + \tilde{u}_m s^m + \cdots \right\}. \tag{14}$$

After calculating the first two coefficients, we conclude

$$\tilde{u}_{-2} = \sum_{i=0}^{K} (\gamma_i - \gamma_i) = 0 \tag{15}$$

$$\begin{aligned} \tilde{u}_{-1} &= \sum_{i=0}^{K} (a_i - \gamma_i \tau_i - a_{i+1} + \gamma_i \tau_{i+1}) \\ &= \sum_{i=0}^{K} (a_i - a_{i+1} - \gamma_i(\tau_i - \tau_{i+1})) = 0. \end{aligned} \tag{16}$$

Algorithm: IEKS Moments Calculating Algorithm
Input: 1) A PWL source $u(t)$ with $\{(a_0,\tau_0),(a_1,\tau_1)\cdots,(a_{K+1},\tau_{K+1})\}$
2) M, the number of moments to calculate
Output: $\mathbf{u}_m = \{\ u_1,\ \ u_2,\ \ \cdots,\ \ u_M\ \}$, the first M moments of the PWL source.
Begin
for $i = 0 : K$
$\gamma_i = \dfrac{(a_{i+1} - a_i)}{(\tau_{i+1} - \tau_i)}$
$\beta_i^{(1)} = -\tau_i$
end
for $m = 1 : M$
for $i = 0 : K+1$
$\beta_i^{(m+1)} = \dfrac{-\tau_i}{m+1}\beta_i^{(m)}$
end
$u_{m-1} = (a_0 - \gamma_0\dfrac{\tau_0}{m+1})\beta_0^{(m)} - \sum_{i=0}^{K-1}(\gamma_i - \gamma_{i+1})\beta_{i+1}^{(m+1)} - (a_{K+1} - \gamma_K\dfrac{\tau_{K+1}}{m+1})\beta_{K+1}^{(m)}$
end
End

Fig. 6. IEKS Moments calculating algorithm

Finally, we derive the explicit formulas for the rest coefficients, $\tilde{u}_0$, $\tilde{u}_1$, $\cdots$, etc. This procedure is summarized in Fig. 6. The first two terms are eliminated and Equation (14) can be rewritten as a moment representation starting from the 0_{th} moment.

$$\mathcal{L}\{u(t)\} \ = \ \left\{\tilde{u}_0 + \tilde{u}_1 s + \tilde{u}_2 s^2 + \cdots + \tilde{u}_m s^m + \cdots\right\} \tag{17}$$

Lemma 1: Given a finite-time PWL source, IEKS constructs its moment representation which the -1_{st} and -2_{nd} order moments are zeros.

B.2 System Solution by IEKS

IEKS generates a system transform matrix $\mathbf{V}_i$, by which the i_{th} block of the original system is transformed into a compact description,

$$\widetilde{\mathbf{G}}_i\widetilde{x}_i + \widetilde{\mathbf{C}}_i\frac{d}{dt}\widetilde{x}_i \ = \ \left[\begin{array}{cc} \widetilde{\mathbf{B}}_i & \widetilde{\mathbf{B}}_i' \end{array}\right]\left[\begin{array}{c} \mathbf{0} \\ \\ i_{gi} \end{array}\right]. \tag{18}$$

This compact form can be solved quickly in the time domain by standard integration algorithms. The solution of the i_{th} block is recovered by $x_i \approx \mathbf{V}_i \widetilde{x}_i$, and the desired port currents can be directly obtained by $i_{Ni} = \mathbf{B}^T x_i \approx \widetilde{\mathbf{B}}^T \widetilde{x}_i$.

C. Macromodel Integration and Top Level Reduced-Model Simulation

After the step $A2$ of HiPRIME as illustrated in Fig. 2, a block consisting of RLKC segments with many internal PWL currents is transformed into a passive order reduced block with current sources attached only at the ports. The new macromodel of each block is illustrated in Fig. 7, and each port response of the original block is preserved. Each macromodel is generated for each specific block, and the entire

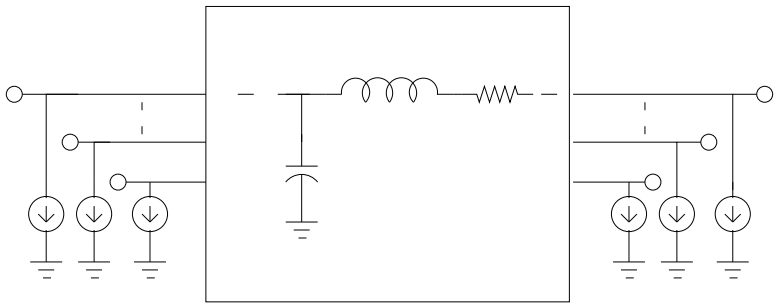

Fig. 7. Equivalent circuit for each block

network is integrated by combining those macromodels together. Each block is viewed as a node of the integrated network, and is stamped into the MNA equation of the entire network. The combination of i_{th} block and j_{th} block can be represented as

$$\begin{bmatrix} \widetilde{\mathbf{G}}_i & \mathbf{0} & -\widetilde{\mathbf{B}}_{ij} \\ \mathbf{0} & \widetilde{\mathbf{G}}_j & -\widetilde{\mathbf{B}}_{ji} \\ \widetilde{\mathbf{B}}_{ij}^T & \widetilde{\mathbf{B}}_{ji}^T & \mathbf{0} \end{bmatrix} \begin{bmatrix} \widetilde{x}_i \\ \widetilde{x}_j \\ u_{ij} \end{bmatrix} + \begin{bmatrix} \widetilde{\mathbf{C}}_i & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \widetilde{\mathbf{C}}_j & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \widetilde{x}_i \\ \widetilde{x}_j \\ u_{ij} \end{bmatrix} = \begin{bmatrix} \widetilde{\mathbf{B}}_{ii} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \widetilde{\mathbf{B}}_{jj} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{E}_i^T & \mathbf{E}_j^T \end{bmatrix} \begin{bmatrix} u_i \\ u_j \\ i_{N_i} \\ i_{N_j} \end{bmatrix}, \tag{19}$$

where

u_{ij} : nodal voltages at the common ports of i_{th}, and j_{th} block.

u_i : nodal voltages of the i_{th} block's ports which are not connected to the j_{th} block.

u_j : nodal voltages of the j_{th} block's ports which are not connected to the i_{th} block.

$\widetilde{\mathbf{B}}_{ii}$: connection between the i_{th} block's internal nodes and ports which are exclusive of j_{th} block.

$\widetilde{\mathbf{B}}_{jj}$: connection between the j_{th} block's internal nodes and ports which are exclusive of i_{th} block.

$\widetilde{\mathbf{B}}_{ij}$: connection of the i_{th} block's internal nodes to the j_{th} block.

$\widetilde{\mathbf{B}}_{ji}$: connection of the j_{th} block's internal nodes to the i_{th} block.

i_{N_i} : equivalent ports' currents of the i_{th} block which are extracted from the i_{th} block.

i_{N_j} : equivalent ports' currents of the j_{th} block which are extracted from the j_{th} block.

$\mathbf{E}_i$: connection of the internal nodes to the equivalent port currents for the i_{th} block.

$\mathbf{E}_j$: connection of the internal nodes to the equivalent port currents for the j_{th} block.

Given this glued macromodel in Equation (19), the model order reduction, and simulation techniques such as PRIMA or IEKS can be further applied to the top level to save runtime. Since there may be more than two hierarchical levels, the higher level model order reduction is introduced as follows. First, some block system matrices for the i_{th}, and j_{th} block are defined as

$$\mathbf{G}' = \begin{bmatrix} \widetilde{\mathbf{G}}_i & \mathbf{0} & -\widetilde{\mathbf{B}}_{ij} \\ \mathbf{0} & \widetilde{\mathbf{G}}_j & -\widetilde{\mathbf{B}}_{ji} \\ \widetilde{\mathbf{B}}_{ij}^T & \widetilde{\mathbf{B}}_{ji}^T & \mathbf{0} \end{bmatrix}, \tag{20}$$

$$\mathbf{C}' = \begin{bmatrix} \widetilde{\mathbf{C}}_i & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \widetilde{\mathbf{C}}_j & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix}, \tag{21}$$

$$\mathbf{B}' = \begin{bmatrix} \widetilde{\mathbf{B}}_{ii} & \mathbf{0} \\ \mathbf{0} & \widetilde{\mathbf{B}}_{jj} \\ \mathbf{0} & \mathbf{0} \end{bmatrix}. \tag{22}$$

Then, with the internal current sources disconnected, the system becomes to

$$\mathbf{G}' \begin{bmatrix} \widetilde{x}_i \\ \widetilde{x}_j \\ u_{ij} \end{bmatrix} + \mathbf{C}' \frac{d}{dt} \begin{bmatrix} \widetilde{x}_i \\ \widetilde{x}_i \\ u_{ij} \end{bmatrix} = \mathbf{B}' \begin{bmatrix} u_i \\ u_j \end{bmatrix}. \tag{23}$$

Let $\widetilde{\mathbf{V}} = [\ \widetilde{\mathbf{V}}_1^T \quad \widetilde{\mathbf{V}}_2^T \quad \widetilde{\mathbf{V}}_3^T\ ]^T$ be the orthogonal bases of the subspace spanned by the moments of $[\ \widetilde{x}_i^T \quad \widetilde{x}_j^T \quad u_{ij}^T\ ]^T$, and denote $\widetilde{\mathbf{G}}' = \widetilde{\mathbf{V}}^T\mathbf{G}'\widetilde{\mathbf{V}}$, $\widetilde{\mathbf{C}}' = \widetilde{\mathbf{V}}^T\mathbf{C}'\widetilde{\mathbf{V}}$, $\widetilde{\mathbf{B}}' = \widetilde{\mathbf{V}}^T\mathbf{B}'$, $[\ \widetilde{x}_i^T \quad \widetilde{x}_j^T \quad u_{ij}^T\ ]^T \approx \widetilde{\mathbf{V}}\widetilde{z}$. The MNA equation generated by the higher level order-reduction is

$$\widetilde{\mathbf{G}}'\widetilde{z} + \widetilde{\mathbf{C}}' \frac{d}{dt}\widetilde{z} = \widetilde{\mathbf{B}}' \begin{bmatrix} u_i \\ u_j \end{bmatrix}. \tag{24}$$

D. Preservation of Passivity

In order to apply PRIMA or IEKS to the reduced model (as described in the previous section) , the higher level order-reduced model must be also passive. The warrant is given by the following theorem.

Theorem 1: During the hierarchical model order reduction, the passivity of the higher level order-reduced macromodel is preserved. That is to say, the transfer function, $\mathbf{Y}(s)$, of the higher level order-reduced system satisfies

1. $\mathbf{Y}(s^\star) = \mathbf{Y}^\star(s)$ for all complex s.

2. $\mathbf{Y}(s)$ is a positive matrix, that means, $Z^{\star T}(\mathbf{Y}(s)+\mathbf{Y}^T(s^\star))Z \succeq 0$ for any complex s satisfying $Re(s) \succ 0$ and for any complex vector Z.

Proof: With the impulse voltages stimulating at ports, and applying Laplace transform to Equation (24), the transfer function can be obtained as

$$\mathbf{Y}(s) \;=\; \widetilde{\mathbf{B}'}^{T}(\widetilde{\mathbf{G}'}+s\cdot\widetilde{\mathbf{C}'})^{-1}\widetilde{\mathbf{B}}'. \tag{25}$$

Since the system matrices are all real, the first condition is met naturally. To prove that the second condition is also met, we start from

$$Z^{\star T}(\mathbf{Y}(s)+\mathbf{Y}^{T}(s^{\star}))Z \;=\; Z^{\star T}(\widetilde{\mathbf{B}'}^{T}(\widetilde{\mathbf{G}'}+s\cdot\widetilde{\mathbf{C}'})^{-1}\widetilde{\mathbf{B}}'+\widetilde{\mathbf{B}'}^{T}(\widetilde{\mathbf{G}'}+s^{\star}\cdot\widetilde{\mathbf{C}'})^{-T}\widetilde{\mathbf{B}}')Z. \tag{26}$$

By plugging $w=(\widetilde{\mathbf{G}'}+s^{\star}\cdot\widetilde{\mathbf{C}'})^{-T}\widetilde{\mathbf{B}}'Z$, and $s=j\varpi+\sigma$ into Equation (26), it becomes to

$$\begin{aligned} Z^{\star T}(\mathbf{Y}(s)+\mathbf{Y}^{T}(s^{\star}))Z &= w^{\star T}\left[(\widetilde{\mathbf{G}'}+(j\varpi+\sigma)\cdot\widetilde{\mathbf{C}'})+(\widetilde{\mathbf{G}'}+(-j\varpi+\sigma)\cdot\widetilde{\mathbf{C}'})^{T}\right]w \\ &= w^{\star T}\left(\widetilde{\mathbf{G}'}+\widetilde{\mathbf{G}'}^{T}\right)w+w^{\star T}\cdot\sigma\cdot\left(\widetilde{\mathbf{C}'}+\widetilde{\mathbf{C}'}^{T}\right)w. \end{aligned} \tag{27}$$

Since $\mathbf{C}_i$,and $\mathbf{C}_j$ are symmetric, $\mathbf{C}_i^T+\mathbf{C}_i=2\mathbf{C}_i$, and $\mathbf{C}_j^T+\mathbf{C}_j=2\mathbf{C}_j$. Along with the fact that $\mathbf{C}_i$, and $\mathbf{C}_j$ are nonnegative definite, it yields

$$w^{\star T}\cdot\sigma\cdot\left(\widetilde{\mathbf{C}'}+\widetilde{\mathbf{C}'}^{T}\right)w=\sigma\cdot w^{\star T}\widetilde{\mathbf{V}}_1^{T}\mathbf{V}_i^{T}2\mathbf{C}_i\mathbf{V}_i\widetilde{\mathbf{V}}_1w+\sigma\cdot w^{\star T}\widetilde{\mathbf{V}}_2^{T}\mathbf{V}_j^{T}2\mathbf{C}_j\mathbf{V}_j\widetilde{\mathbf{V}}_2w\succeq 0, \tag{28}$$

for any complex vector Z, and positive σ. Since $\mathbf{N}_i$, and $\mathbf{N}_j$ are symmetric, nonnegative definite matrices, we have

$$\begin{aligned} w^{\star T}\left(\widetilde{\mathbf{G}'}+\widetilde{\mathbf{G}'}^{T}\right)w &= w^{\star T}\widetilde{\mathbf{V}}_1^{T}\mathbf{V}_i^{T}(\mathbf{G}_i^{T}+\mathbf{G}_i)\mathbf{V}_i\widetilde{\mathbf{V}}_1w+w^{\star T}\widetilde{\mathbf{V}}_2^{T}\mathbf{V}_j^{T}\left(\mathbf{G}_j^{T}+\mathbf{G}_j\right)\mathbf{V}_j\widetilde{\mathbf{V}}_2w \\ &= w^{\star T}\widetilde{\mathbf{V}}_1^{T}\mathbf{V}_i^{T}\begin{bmatrix}2\mathbf{N}_i & \mathbf{0}\\ \mathbf{0} & \mathbf{0}\end{bmatrix}\mathbf{V}_i\widetilde{\mathbf{V}}_1w+w^{\star T}\widetilde{\mathbf{V}}_2^{T}\mathbf{V}_j^{T}\begin{bmatrix}2\mathbf{N}_j & \mathbf{0}\\ \mathbf{0} & \mathbf{0}\end{bmatrix}\mathbf{V}_j\widetilde{\mathbf{V}}_2w\succeq 0, \end{aligned}$$

for any complex vector Z. Hence, the second condition is also satisfied. Therefore, the passivity of the higher level order-reduced macromodel is preserved. ♢

IV. Experimental Results

This section demonstrates the speed and accuracy of HiPRIME and IEKS, and compares them with other methods. We use mesh networks to model the power delivery networks, which consist of lumped RC/RLKC segments with many current sources attached inside. The first example is a 5,000 node RLC

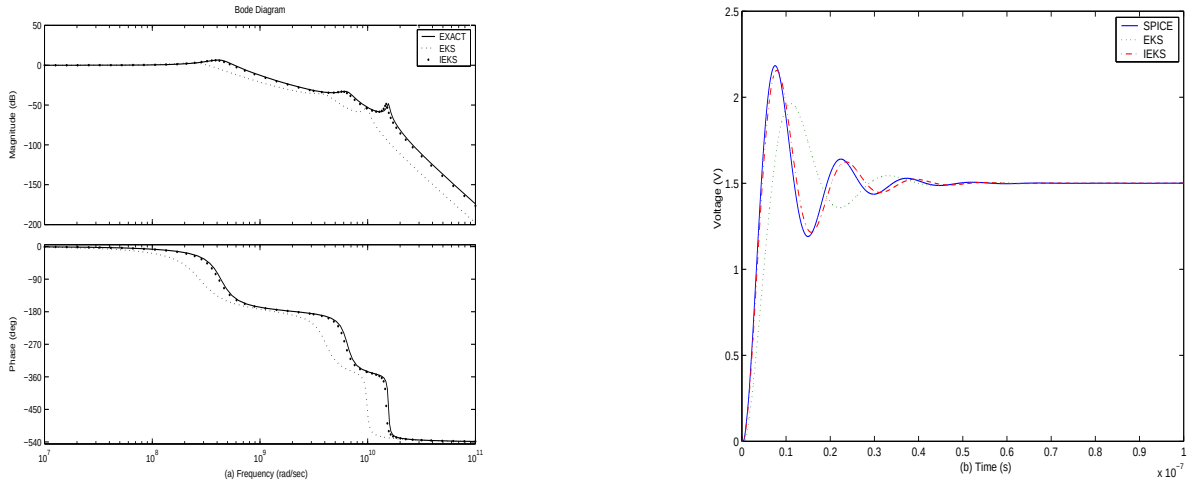

Fig. 8. Comparison of EKS, IEKS and EXACT (a) frequency domain simulations result of IEKS, EKS and EXACT with regard to both magnitude and phase (b)timing domain simulation results of IEKS, EKS and SPICE

circuit, with wire resistance as 0.01 Ω p.u.l. (per unit length), wire capacitance as 1pF p.u.l., wire inductance as 10hH p.u.l., and load capacitance as 40pF. The bode diagram is in Fig. 8(a). Starting from 1GHz, EKS shows noticeable difference with the exact value (theoretical calculation) and IEKS results. The results of IEKS matche very well with the EXACT results with regard to both magnitude and phase from low frequency up to over 10GHz. Fig. 8(b) shows the transient simulation results. The EXACT result is generated by SPICE.

For the rest of the examples, each lumped RC/RLKC segment uses $R = 0.2\Omega$, $L = 1.0pH$ and $C = 0.024fF$, and HiPRIME partitions each original circuit into two blocks. The accuracy of HiPRIME for the RC and RLC circuits is tested and the results are shown in Fig. 9, and Fig. 10, respectively. A grid node is randomly picked and its voltage waveforms of HiPRIME are compared with those of IEKS(flat),

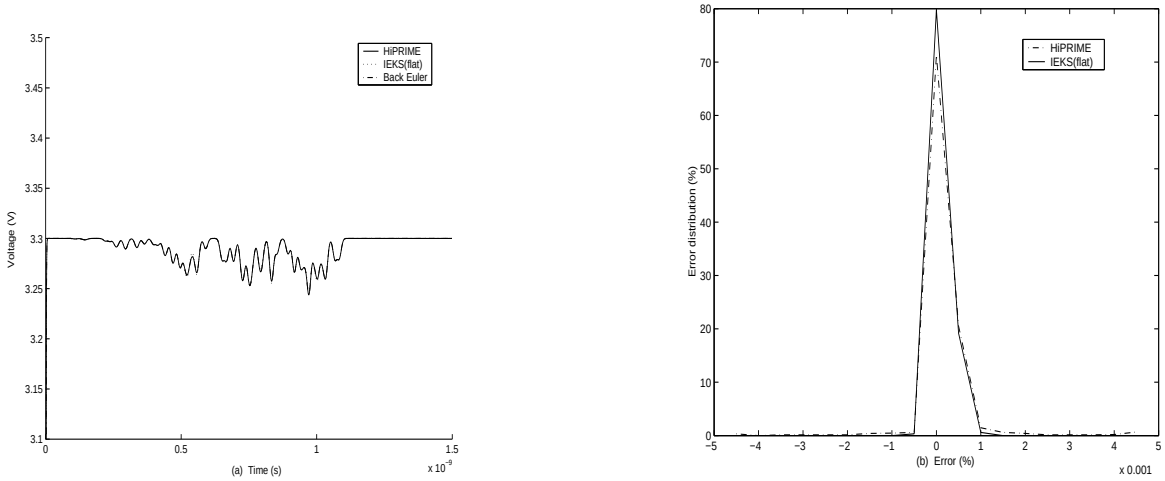

Fig. 9. Accuracy analysis of RC circuit case: (a) waveform result of HiPRIME, IEKS(flat) and Back Euler (b) error spectrum of HiPRIME and IEKS(flat)

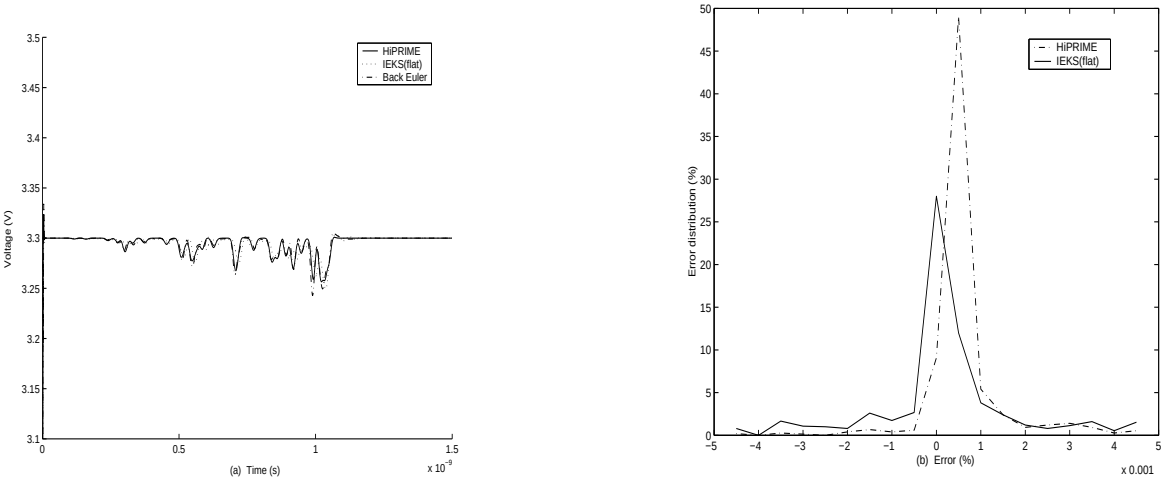

Fig. 10. Accuracy analysis of RLC circuit case: (a) waveform result of HiPRIME, IEKS(flat) and Back Euler (b) error spectrum of HiPRIME and IEKS(flat)

and Back Euler. In the RC circuit as shown in Fig. 9, the voltage waveforms of HiPRIME, IEKS(flat), and Back Euler are indistinguishable, the error percentage of HiPRIME, and IEKS(flat) for 80% time intervals is within 0.001%, and their maximum error is less than 4.5%. In the RLC circuit as shown in Fig. 10, the voltage waveforms of HiPRIME, and IEKS(flat) match the result obtained by Back Euler method very well, and the error percentage for 50% time intervals is within 0.001%.

Circuit Size	IEKS(flat) (s)	InductWise (s)	Speedup (X)	Spice (s)	Speedup (X)
7861	1.46	14.76	10.1	697.13	477.48
14081	3.88	29.77	7.67	2728.18	703.14
43541	13.49	107.05	7.93	–	–
89201	35.33	244.95	6.93	–	–

TABLE I
RUNTIME OF IEKS(FLAT), INDUCTWISE AND SPICE

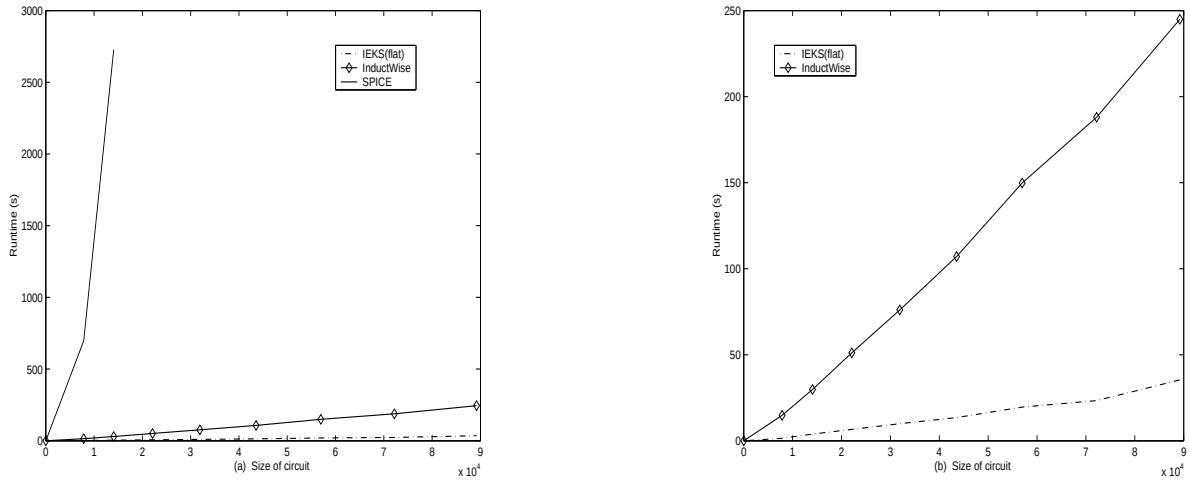

Fig. 11. Runtime Analysis of (a) IEKS(flat), InductWise and Spice (b) IEKS(flat) and InductWise

We implement IEKS(flat) in C++ language and test it on a PIII 933MHz machine. The results are compared with Spice, and an efficient time domain solver InductWise [18], [19]. Table I summarizes the runtime results, and the runtime comparisons are shown in Fig. 11. The significant speed improvement, 700 times faster than Spice, is observed and the same tendency that the speed up increases with larger circuit size is shown. The IEKS is also around 7 times faster than the InductWise.

We also implement HiPRIME, IEKS(flat), and Back Euler in Matlab, and test them on Sun Ultrasparc V. Each circuit is partitioned into two sub-circuits in HiPRIME. Table II, and III summarize the runtime results, and the runtime comparisons are shown in Fig. 12 and Fig. 13 for the RC and RLC circuits respectively. From the figures, we can see the tendency that the speed up gets more impressive as the

Circuit Size	HiPRIME (s)	IEKS(flat) (s)	Speedup (X)	Back Euler (s)	Speedup (X)
203	2.52	0.89	0.36	17.1	6.79
803	2.98	1.97	0.66	78.3	26.3
2403	4.39	6.17	1.40	288.9	65.8
5003	7.93	13.18	1.66	760.1	95.8

TABLE II
RUNTIME OF RC CIRCUIT CASE

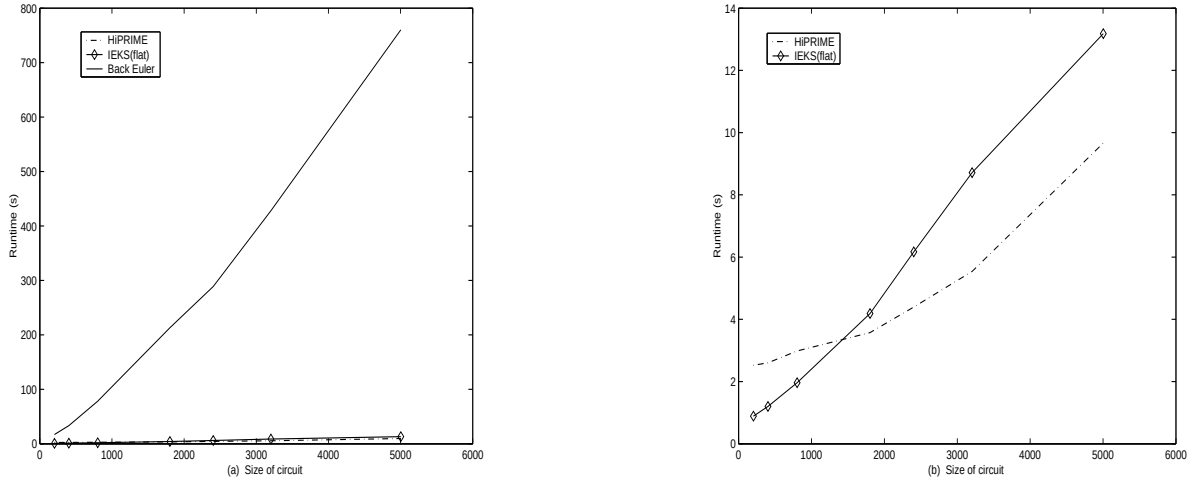

Fig. 12. Runtime analysis of RC circuit case: (a) runtime of HiPRIME, IEKS(flat) and Back Euler (b) runtime of HiPRIME and IEKS(flat)

circuit size increases.

Finally, we compare the runtime between HiPRIME and IEKS(flat). The program is implemented in C++ language and tested on a Pentium IV 3.0GHz machine with 3.0GB memory. The number of partitions is two in HiPRIME. The result is summarized in Table IV. The HiPRIME is about two times faster than the IEKS(flat), and the speed up gets more impressive as the circuit size increases.

V. CONCLUSION

A novel hierarchical power delivery analysis methodology is presented. This methodology integrates the multiple-port Norton equivalent theorem with the model order reduction algorithm to generate compact models from the original circuit. Experimental results show that the simulation is accurate and fast. The

Circuit Size	HiPRIME (s)	IEKS(flat) (s)	Speedup (X)	Back Euler (s)	Speedup (X)
443	2.76	1.29	0.47	29.5	10.7
1883	3.87	5.08	1.31	129.8	33.5
3843	6.72	12.94	1.92	276.9	41.2
5803	11.81	27.15	2.29	427.2	36.6

TABLE III
RUNTIME OF RLC CIRCUIT CASE

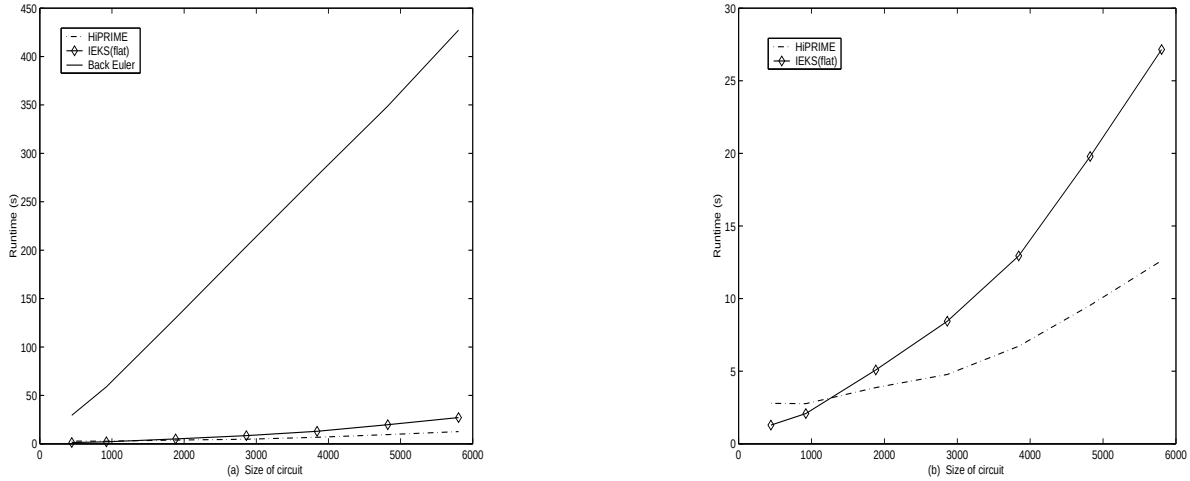

Fig. 13. Runtime analysis of RLC circuit case: (a) runtime of HiPRIME, IEKS(flat) and Back Euler (b) runtime of HiPRIME and IEKS(flat)

Circuit Size	HiPRIME (s)	IEKS(flat) (s)	Speedup (X)
12300	0.359	0.735	2.047
49600	1.406	3.015	2.144
199200	7.157	15.890	2.220
448800	18.719	43.094	2.569

TABLE IV
RUNTIME COMPARISON BETWEEN HIPRIME AND IKES(FLAT)

procedure of generating compact models involves an improved IEKS method which it no longer needs to perform moment shifting for the source waveform modeling. To further reduce runtime, a multiple level passive model reduction algorithm is developed and its passivity has been proved.

It has been known that the runtime of PRIMA is proportional to the number of ports. Although we use PRIMA to generate the reduced system in the simulation, we can also utilize IEKS to generate both the

reduced system and the Norton equivalent current sources. We plan to investigate the realizable model order reduction algorithms whose runtime are port size independent. we would also like to point out that the focus of of this paper is not on the partition algorithms. However, a good partition algorithm is important for the performance of hierarchical and passive model order reduction algorithms.

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