On-Chip Power Integrity, Including Package Effects

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On-chip power integrity effects and their influence on the entire power delivery system have become a major concern in the design of large and complex high-speed SoC designs. Today's extreme design challenges require a complete power-aware solution that encompasses the global effects of the entire power delivery system, including the realistic effects of the package and the PC board on the functional operation of the IC.

There is a prevalent desire to closely link package-level and IC-level design processes so that package-to-chip and chip-to-package dependencies can be considered during the design process. The solution is a revolutionary co-design and co-simulation approach that simultaneously analyzes the entire power delivery network, from the PC board voltage supply, through the package power planes and pins, to the on-chip power grid, to insure the creation of operational designs.

Increasing Design Complexity

Large SoC designs up to 20x20mm or larger provide more usable silicon area, enabling opportunities for advanced functionality through creative customization of more on-chip logic and IP blocks. As a result of the increasing number of on-chip devices, the size of the full-chip electrical power grid model has grown exponentially large. And as current technology advances from 90nm to 65nm, the number of on-chip layers needed to supply sufficient power to the additional logic will continue to increase. Multiple power grid domains and multiple voltages are made more complex with the addition of up to 12 or more metal power grid layers, each with thousands of metal lines and tens of millions of metal sections with very high via densities. The increase in both the chip size and the number of layers has resulted in a significantly more complex design effort of the on-chip power delivery system.

In advanced technologies at 90nm and below, the global power delivery that connects to the IC power grid becomes increasingly important. In large high-speed designs, power delivery from the edge-based I/O pads to logic devices in the center of the IC has become inadequate, regardless of the power grid design complexity. As a result, the power delivery mechanism has progressed from edge-connected wire-bond technology to flip-chip technology, consisting of C4 (Controlled Collapse Chip Connection) bumps to provide power distribution from the package power planes to the top-level metal layer of the chip.

In line with today's design trends toward higher clock speeds, larger chips with more devices, and higher I/O counts, flip-chip is becoming the technology of choice, providing a more direct power delivery path from the package power planes, through the C4 bumps to the center core-area of the chip, where extreme power delivery requirements must be met. With the use of flip-chip technology in large high-speed designs, the connection between the chip and the package is more closely related, requiring critical interdependent analysis.

Increased Levels of Design Abstraction

To adequately analyze large complex IC designs, current EDA power analysis tools stress their limitations as they try to consume larger amounts of design data, execute multiple analysis runs, and produce significant amounts of analysis data. In order to maintain the fixed design schedules for on-time product delivery and meet market window dependent time-to-profits goals, designers often are forced circumvent these tool limitations by sacrificing detailed design representation in favor of higher levels of design data abstraction.

In EDA tools, one area of prevalent design data abstraction is the parasitic model representation of the chip. A compete RLC model of the on-chip IC power grid is required for an accurate representation of the interdependent interaction among all the layers and vias. However, to reduce the tremendous amount of data and minimize long run times, the on-chip parasitics often are represented with only resistance models. And, in most cases, the resistance models are further filtered and combined to a higher level of abstraction. If the capacitance of the complete power grid is even considered, it is often only a self-capacitance model, ignoring important interactive effects of mutual capacitance. And almost all power grid extraction techniques ignore the self-inductance and mutual inductance effects of the on-chip power grid system.

Existing EDA solutions also often are incapable of adequately representing the complete parasitic model of the package. The typical "ideal voltage" or fixed potential assignment at C4 bumps is not indicative of the actual voltage variation that exists on the bumps during actual operation. Most tools provide a lumped RLC parasitic model for the C4 bumps, ignoring the interactive mutual coupling between each bump. When more accurate port S-parameter models are used to represent the C4 bumps, they often incorrectly lump a large number of the power and ground bumps together, destroying the spatial voltage variations between the bumps during actual operation.

These inaccurate parasitic model abstractions of the chip and the package fail to accurately represent the distributed interactions in the global chip-package power delivery system, producing incorrect power integrity simulation results that force the over-design of power integrity margins.

A Global Look at the Power Delivery System

During the normal operation of a chip, on-chip circuits utilize current through the power supply for the logic transfer operation. As an on-chip circuit draws power through the power supply lines, the power grid impedance causes voltage fluctuations at the circuit location. These voltage fluctuations, or "voltage noise," propagate through the IC power grid, affecting the voltage levels for other circuits in other areas of the design.

Relative to the package C4 bumps and power planes, the on-chip power grid is a high-loss system. As a result, voltage noise is more likely to propagate from one on-chip circuit to another chip location through the package power structure, rather than through the chip power grid. The electromagnetic interactions and wave propagation effects inside the package structure affect the magnitude of the IC power grid voltage noise. Therefore, it is imperative that IC power integrity analysis includes the entire representation of both the chip and the package power delivery system. If the chip is analyzed in the absence of the package power planes and C4 bumps, or if the C4 bump interface is incorrectly represented as an abstraction of simple lumped RLC parasitic models, the spatial variation of the voltage noise propagation through the package is incorrectly modeled.

The absence of the propagation path through the C4 bumps and the package power planes is not a realistic representation of the actual design operation. IC designs that increasingly appear to be functional during the IC-only simulation often fail to be operational when the chip is inserted into the realistic operating environment of the package, as shown in Figure 1.

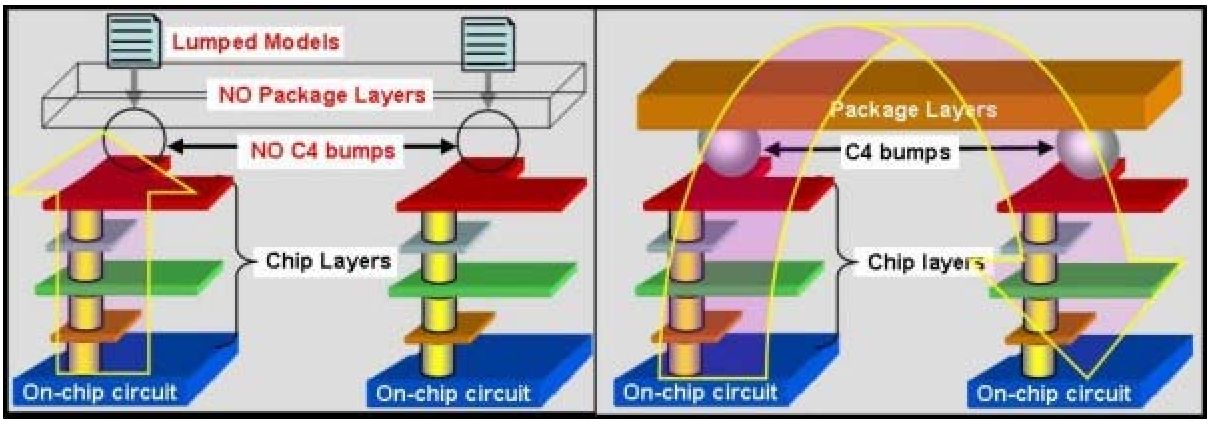

Figure 1. Chip through Package Voltage Noise Propagation
a) Without the package (left figure), voltage noise tends to locally dissipate.
b) With the package (right figure), voltage noise realistically propagates from one on-chip circuit, through the package, to other on-chip circuit locations, affecting voltage levels of other circuits.

IC Designers Require Operational Designs

A common set of design objectives is often targeted to achieve the goal of operational designs in a timely fashion. The design objectives are described as:

- **Timing:** *Designs that work when first fabricated.*
  Signal integrity issues that affect timing require the inclusion of voltage noise variation dependencies that result from IR-drop and power/ground bounce effects.
- **Reliability:** *Designs that continue to work after a period of time in the field.*
  Issues that affect reliability include power supply electromigration, signal self-heat, hot-electron issues, and thermal issues, all of which must include the voltage variation dependencies.
- **Manufacturability:** *Designs that can be fabricated.*
  CMP-related issues that affect manufacturability, solved with slotting and metal-fill, require the inclusion of accurate parasitics that affect voltage noise variation analysis of the power grid. For these voltage noise dependencies to be accurate, the package must be included in the full-chip analysis of these effects.

To achieve operational designs, an IC environment that considers package-level power variation dependencies throughout the chip implementation flow must consist of chip-package co-design and co-simulation functionality that includes the interdependent effects of the package during the design and analysis process.

Elevating IC Power Integrity to the Next Level

The solution that resolves the design and analysis complexities found in separate package and IC design systems is to converge both levels into a single, unified chip-package co-design environment.

A key component of the global chip-package co-design solution is the complete and accurate parasitic extraction of the entire chip-package power delivery system. The parasitic model must be derived from complete IC power grid extraction between all layers, vias, and conductors, and the complete package extraction between all power planes, vias, and C4 bumps. The full RLC parasitic model must include all distributed resistances, as well as all the self and mutual capacitance and inductance couplings in the entire power delivery system, thereby representing an accurate model of both the chip and the package.

The chip-package model representation in the co-design environment must provide fast extraction execution, on the order of only minutes for large complex SoC designs and their associated packages, for the most efficient analysis throughout the chip implementation phases of the design flow.

The co-design environment must specify the design and simulation of the IC properties (chip size, power grid layers, circuit floorplanning, decoupling cap placement), as shown in Figure 2.

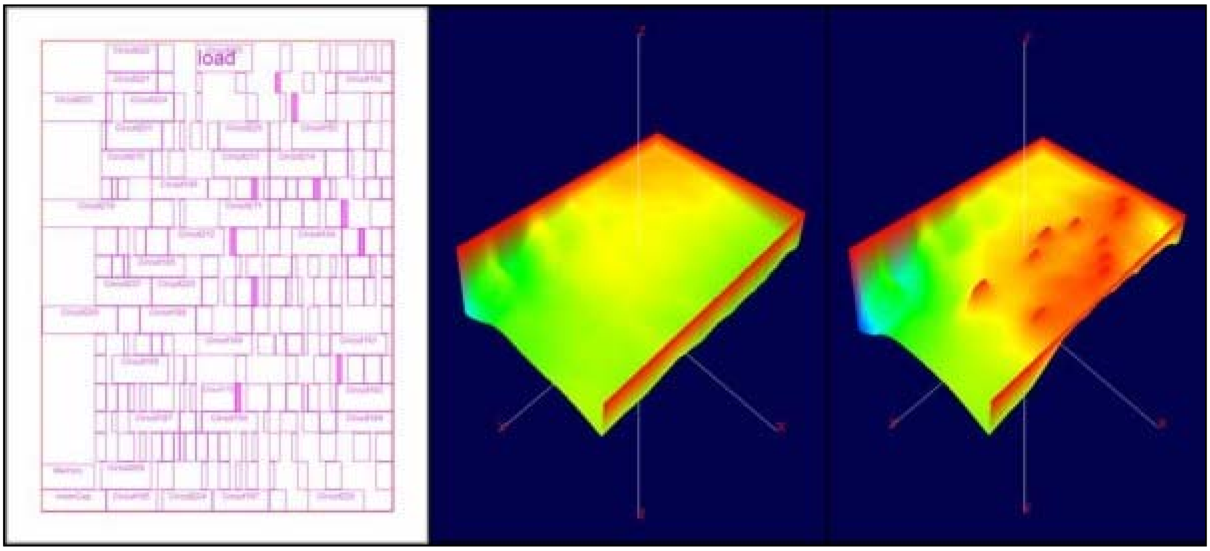

Figure 2. An accurate IC power analysis requires realistic simulation of the on-chip decoupling capacitors
a) The chip-package co-design floorplan (left), shows the circuit placement with highlighted chip-level decoupling caps.
b) The 3D real-time simulation of chip-level voltage noise (middle), without chip- level decoupling capacitors, shows voltage noise fluctuations across the chip.
c) The 3D real-time voltage noise simulation (right), including on-chip decoupling capacitors, shows a more stable on-chip power supply.

The co-design environment must also specify the design and simulation of the package properties (package size, power plane layers, C4 bump interface, decoupling cap placement), as shown in Figure 3.

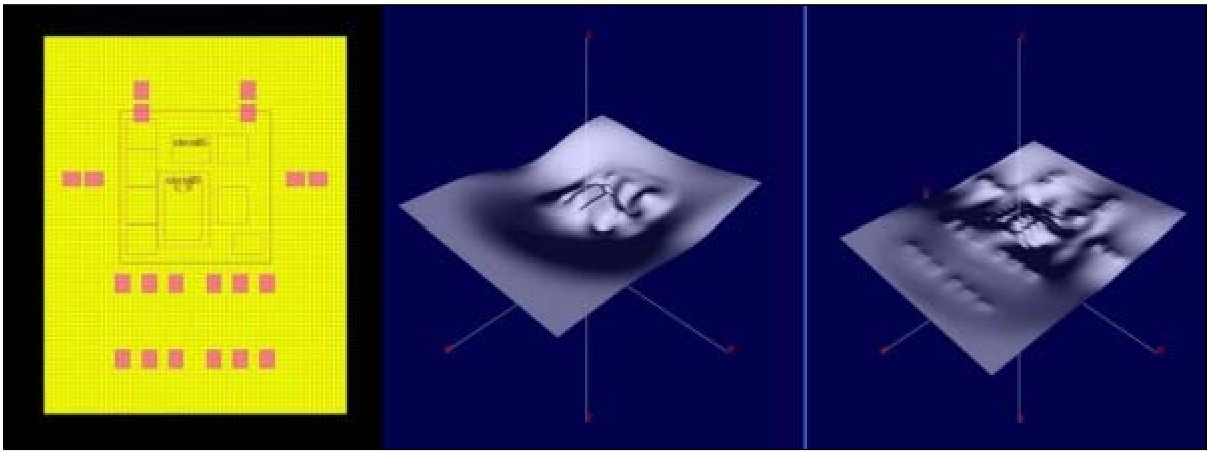

Figure 3. A realistic package power analysis result depends on the effects of both the chip and the package
a) The chip-package co-design floorplan (left) shows chip and package circuit placement with highlighted package-level decoupling caps.
b) The 3D real-time simulation of package voltage noise (middle), without decoupling capacitors, shows critical power supply voltage variations on the package.
c) The 3D real-time simulation of voltage noise (right), including on-package decoupling capacitors, shows a much more stable package power supply level.

The global chip-package co-design solution must provide the accurate co-simulation of the entire power delivery system. Utilizing the accurate parasitic representation of both the chip and the package, simultaneous simulation must occur in synchronized co-simulation time steps, in which each IC time-step simulation takes into consideration the complete package effect, and each package time-step simulation takes into consideration the complete IC effect. By passing package simulation data from the package to the chip and complete chip simulation data from the chip to the package through the connection interface of the C4 bumps, an operationally correct power integrity analysis is performed. It includes the realistic voltage noise propagation effects of the package, as seen from the chip, and the voltage noise propagation effects of the chip, through the package.

System and IC Power-Analysis-Aware Flows

A single power system co-design creation and co-simulation validation system must be applied early enough in the design cycle to reduce downstream design dependencies, and often enough throughout the design cycle to include the realistic physical design characteristics that appear as the design cycle progresses through implementation. Optimizing power system performance in the complete chip-package environment requires a solution that can identify voltage noise issues early and often in the IC design flow for critical design exploration and intuitive what-if analysis.

Only a single co-design and co-simulation solution that is consistently applied throughout the design cycle can deliver an accurate power integrity solution of the converged chip-package design. And only a unified chip and package solution can shorten the overall design cycle by avoiding costly design iterations and re-spins between the package and IC engineering teams. As a result, the chip-package co-design solution can enable the creation of operational designs by applying the flow to both the system-level analysis of the pre-floorplan design, as well as the chip-level analysis of the post-floorplan design.

Chip-Package Environment for Operational Designs

By designing the package and the IC together, the entire power system can be realistically analyzed early and often throughout the IC design flow by including the interdependent chip and package effects in the global analysis solution.

System, package, and IC engineers finally can perform the simultaneous co-design of the IC and package, including all of the dependent physical characteristics between the chip and package, in an intuitive and easy-to-use design environment. The realistic representation of the chip and package, through full RLC parasitic representation of the complete IC and package power delivery system, eliminates the need for inaccurate package or IC model abstraction. In addition, the simultaneous co-simulation of the chip and the package provides an accurate analysis of the effects of the package on the operation of the chip.

Today's large and complex high-speed SoC designs require a global chip-package co-design solution that results in the creation of operational designs. Combining the chip and package interdependencies into a unified co-design environment elevates IC power integrity to the next level by including the critically important effects of the package in the chip design process, avoiding costly design iterations and re-spins, and helping to achieve time-to-profit goals in a shorter design timeframe.

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