Weekly Report for YiYu Shi's work in week1

January 16, 2006

1 Work1: Implementing the code for via insertion

I have developed the code for the ISLPED paper, and now I am debugging it using the parameters obtained from others' papers. This work is expected to be done by the end of this week.

2 Work2: Progress on multi-net routing and on critical path aware routing

I have read several papers provided by Prof. Jing. Now I am thinking of formulating the critical path aware routing problem.

After I discuss with Prof. Jing last time, it is not so accurate to simply minimize the total wirelength from the source to the critical sink, as the delay is not directly proportional to the wirelength from source to sink due to the branches on the path. To some extent the delay model must be introduced.

Also, I have worked with Paul to polish the code for the single net routing. In addition, the framework MATLAB part for the multi-net routing is done. In the next stage we need to try different models to see how to minimize the total wirelength under the capacity constraints.

3 Work3: Reading papers for project on 209S

The project in 209S is much more involved than the one we have last quarter. So I am reading several papers to help get the project done as early as possible.