Time-Domain Macromodels for VLSI Interconnect Analysis

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Abstract— **This paper presents a method of obtaining time-domain macromodels of VLSI interconnection networks for circuit simulation. The goal of this work is to include interconnect parasitics in a circuit simulation as efficiently as possible, without significantly compromising accuracy. Stability issues and enhancements to incorporate transmission line interconnects are also discussed. A unified circuit simulation framework, incorporating different classes of interconnects and based on the proposed macromodels, is described. The simplicity and generality of the macromodels is demonstrated through examples employing RC- and RLC-interconnects.**

I. Introduction

IN ORDER to optimize the design phase of high-speed VLSI systems, it is important for designers to observe the timing behavior of component blocks as early as possible. One of the major goals in the timing-level simulation of these circuit blocks is to be able to simulate the entire signal path (comprising nonlinear devices and interconnections) as efficiently as possible without compromising accuracy to any great extent.

As switching speeds and levels of integration continue to rise, the analog effects due to interconnect have to be considered for the accurate estimation of the signal timing. A signal in a complex VLSI system may typically pass through several levels of interconnect structures, including on-chip interconnect, packaging structures, board-level interconnects, and transmission wires. One approach to modeling these different levels of interconnects, such that they can be jointly simulated, is using passive, lumped, linear circuit models [8] that permit analysis in both time and frequency domains. However, since the associated nonlinear models are simulated in the time domain, it is necessary to focus on the analysis in this domain only.

Unfortunately, circuit simulation of interconnect parasitics using conventional methods of circuit simulation is a notoriously inefficient process. It has been shown that circuit simulation run-time increases super-linearly with the number of nodes in the circuit [33]. The inclusion of elaborate interconnect models, which typically contain a large number of nodes, is therefore not desirable for circuit simulation. In addition, the stiff nature of these circuit models forces the transient time-step of the simulator to be small, thereby contributing to a further degradation in performance.

In this paper, a two-step procedure is proposed for improving the efficiency of circuit simulation for RLC interconnect by:

1) macromodeling the general forms of interconnect blocks independently of (non)linear drivers and terminations using the minimum number of circuit nodes, and
2) incorporating these compact macromodels into existing circuit simulators.

The macromodels mentioned above are approximations of the terminal behavior of the interconnect within an *effective* bandwidth and are synthesized from the s-domain, rational-function approximations of the y-parameters of the interconnect. These y-parameters can be efficiently calculated by applying reduced-order modeling techniques such as the Asymptotic Waveform Evaluation (AWE) method, either on equivalent lumped circuit models [12], or on distributed parameter models [3], [16] of the isolated interconnect blocks. This y-parameter calculation can be considered as a one-time, pre-characterization step for a given interconnect; the synthesized macromodel can then be included in a full circuit simulation with nonlinear devices and accessed as device model calls in general-purpose circuit simulators. The convolution problem involved in converting from s-domain descriptions to time-domain descriptions is solved through the combination of a canonical realization technique and numerical integration methods. No assumptions are made concerning the voltage wave-shapes at the ports, and any numerical integration method can be used in deriving macromodels. The main benefits of the proposed macromodels are the optimality of size, while maintaining the merits of lumped-circuit models, and the reduction of stiffness, resulting in increased simulation efficiency. Also, the simplicity of this macromodeling scheme provides a unified simulation framework for most interconnection networks, whether they are characterized as on-chip interconnect, transmission lines, etc.

In the following section, some background on modeling issues for VLSI interconnect is addressed. In particular, efficient reduced-order modeling techniques for interconnects are discussed. Section III discusses the pre-characterization of these

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interconnect models using multi-port descriptors that are independent of interconnect-terminal conditions. This preserves the validity of the macromodel in the presence of nonlinear drivers and/or terminations. Some related stability issues are also discussed. In Section IV, the development of interconnect macromodels from the pre-characterized multi-port descriptors is presented, and the associated local truncation errors are analyzed. A typical simulator interface is presented in Section V along with examples of employing the proposed approaches on several interconnect circuit configurations obtained from industry. Section VI concludes the paper by summarizing the proposed approach.

II. VLSI Interconnect Modeling Issues

A. Interconnect Modeling

The modeling of VLSI interconnects has been the focus of many recent papers [3], [4], [6], [8], [9], [12], [19], [26], [28], [29], [30], [31], [34], and can essentially be divided into two broad categories: 1) RC-class and 2) RLC-class. RC-class models include most of the on-chip interconnects in mid- to high-frequency MOS integrated circuits, where the inductance effects of the lines are dominated by the resistance effects. These on-chip interconnections typically possess high values of line resistance due to their small cross-sections, and they can be modeled to a fair degree of accuracy by linear RC-circuits such as RC-trees and -meshes [9]. These RC-class models have been efficiently analyzed using the first-order approximations (the Elmore delay) and higher, qth-order approximations [21]. RLC-class models, which include most of the off-chip interconnects, have been analyzed mostly using transmission-line analysis techniques [4], [6], [8], [9], [24], [28], [30], [31], [34]. To efficiently analyze transmission lines, methods based on reduced-order modeling techniques have been reported in [24], [31]. In [31], the distributed equations of the transmission line are incorporated as submatrices in the system matrix of the overall circuit including other circuit components. The response moments needed for the AWE analysis of the circuit are generated from the derivatives of the system matrix, which yields a qth-order approximation for the overall circuit. Obtaining macromodels of a general multi-port in terms of its admittance (y-parameter) matrix is described in [24], which utilizes the AWE method to precharacterize the linear RLC interconnects. This macromodel is directly stenciled into the system matrix of the overall circuit. The response of the overall circuit is then computed using conventional circuit simulation techniques.

The first step in building the reduced-order model of an interconnect is to determine a finite, approximate bandwidth of interest. In most digital applications, the minimum wavelength of interest of the propagating signal can be approximated. For instance, while a saturated ramp has an energy spectrum spread over an infinite frequency range, most of the signal energy is low-frequency in nature, and decreases rapidly and monotonically, with increase in frequency, as shown in Fig. 1 [8].

Further, the high-frequency components in the signal energy spectrum correspond to the "artificial" discontinuity of the saturated ramp at $t = t_r$, the rise-time, and are rarely present in real, physical signals. Hence, ignoring the high-frequency components of the spectrum above a certain value of maximum angular frequency, $\omega_{\max}$, introduces minimum distortion in the overall signal shape. Consequently, for all practical purposes, the width of the spectrum can be assumed to be finite. In other words, the signal energy of interest is assumed to be contained in the major lobe of the spectrum. Hence, $\omega_{\max}$ can be defined as the 3-dB bandwidth point [6], i.e.,

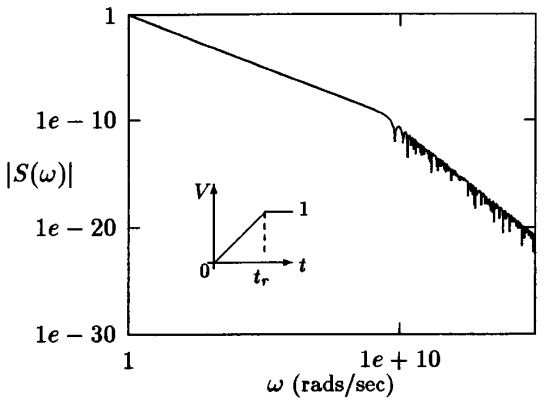


Fig. 1. Saturated ramp signal ($t_r = 1$ ns) and associated amplitude spectrum.

$$\omega_{\max} \approx \frac{2.2}{t_r}, \tag{1}$$

or more conservatively [8] as

$$\omega_{\max} \approx \frac{2\pi}{t_r}. \tag{2}$$

This approximate bandwidth of interest can be employed in the selection of the number of lumped sections when the interconnect is modeled using lumped circuit segments.

By modeling an interconnect with a lumped circuit, it is implied that the lumped model captures the asymptotic behavior of the interconnect, which in turn is dictated by its transmission and loading characteristics, i.e., the propagation constant, $\gamma(\omega)$, and the characteristic impedance, $Z_0(\omega)$, of the interconnect. The number of sections required for the lumped model of a uniform transmission line, N, can then be bounded based on the relative errors on γ and Z_0. For example, an acceptable error of 2.5% on the characteristic impedance in the case of a simple lossless line yields [6]:

$$N \geq 2.25\omega_{\max}T_f, \tag{3}$$

where T_f denotes the time of flight (phase delay) of the line. Similar expressions can be developed for the case of lossy lines, and coupled lines [6], [14].

In the above scheme, the lumped models of uniform interconnects is essentially considered to be a cascade connection of identical, bidirectional, lumped sections. General forms of nonuniform interconnects such as lines with periodic and nonperiodic loadings or discontinuities, and tapered lines, can be modeled as a series of uniform interconnects using *piece-wise uniform* assumption [5]. The configuration of the

individual sections of each uniform interconnect depends on the interconnect parasitics being considered.

The lumped models obtained above, though optimal in the number of sections for each segment, are still stiff for the system-level analysis and cannot be evaluated efficiently using conventional circuit-simulation methods. A more efficient approach would be to employ the use of recently developed model-order reduction methods, such as AWE technique [21], briefly described in the following section.

B. Asymptotic Waveform Evaluation

AWE permits us to model large (and possibly high-order), linear, lumped, finite (LLF) circuits using reduced-order, rational-function models. The method of order-reduction is based on a moment-matching technique, which is a Padé approximation [2]. Simply stated, AWE approximates the impulse response of a large, high-order circuit using a finite, reduced-order, rational-function approximation of the form:

$$\tilde{H}(s) \approx \frac{a_{q-1}s^{q-1} + a_{q-2}s^{q-2} + \cdots + a_1 s + a_0}{s^q + b_{q-1}s^{q-1} + \cdots + b_1 s + b_0}, \quad (4)$$

where the order of approximation is denoted by q. The values of the numerator coefficients a_i and the denominator coefficients b_i are obtained by matching the first $2q$ coefficients (termed 'moments' for stable systems) of the MacLaurin series expansions of $\tilde{H}(s)$ with those of the actual impulse response $H(s)$. The method of model-order reduction such as AWE is based on the fact that for many large, physical systems, the coefficients of the series expansion of the transfer function are much more easier to obtain than an exact, closed form of the transfer function itself. These coefficients a_i and b_i reflect the influence of only the dominant modes of the circuit, which have been shown to largely determine the response of physical systems such as interconnect [22]. The underlying theory of AWE is well documented in [20], [21], and subsequent work relating to stability issues, determination of model-order, and applications are presented in [1], [7], [10], [9], among others.

The inherent efficiency of AWE lies in the computation of the actual circuit moments. The AWE methodology also lends itself to highly efficient implementations such as the Rapid Interconnect Circuit Evaluator (RICE) [26], which obtain even greater improvements in speed by exploiting the interconnect circuit topology. The development of these implementations thus provides a means of evaluating the lumped models of complex interconnect configurations much more efficiently than possible using a conventional circuit simulator.

The precharacterization of the interconnect models using s-domain, multi-port descriptions is necessary for the macromodeling approach. This precharacterization can be done either by preprocessing the equivalent lumped circuit configurations using AWE, or through other reduced-order modeling methods applied directly on distributed models of transmission lines [16]. Since it is more efficient to integrate the extraction method and the simulation method of VLSI interconnects for the systematic design automation environment, we need to consider the way in which the extractor generates the parasitic information when we choose the precharacterization method.

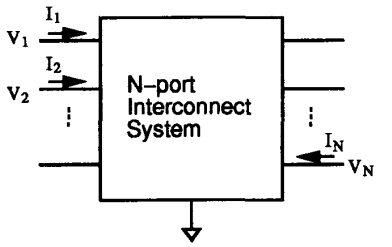


Fig. 2. Modeling a general VLSI interconnection network as an N-port network.

It is noted that some extractors inherently adopt the concept of "lumped" elements in an infinitesimal dimension of frequency-dependent lines. In such cases, the multiport descriptions of the interconnect models are efficiently obtained through a preprocess using AWE.

III. Multi-Port Characterization of Interconnects

The asymptotic VLSI interconnection network models can be considered to be multi-ports, as shown in Fig 2. Such networks are usually characterized in terms of one of the following sets of interchangeable descriptors, namely, y (admittance), z (impedance), h (hybrid), or transmission parameters. To facilitate the interface with general-purpose circuit simulators such as SPICE [23], which employs Modified Nodal Analysis (MNA), in this paper the y-parameters are used to characterize the multi-port networks using the following notation:

$$\begin{bmatrix} Y_{11}(s) & \cdots & Y_{1N}(s) \\ Y_{21}(s) & \cdots & Y_{2N}(s) \\ \vdots & \ddots & \vdots \\ Y_{N1}(s) & \cdots & Y_{NN}(s) \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \\ \vdots \\ V_N(s) \end{bmatrix} = \begin{bmatrix} I_1(s) \\ I_2(s) \\ \vdots \\ I_N(s) \end{bmatrix}. \quad (5)$$

For lumped circuits, each term $Y_{ij}(s)$, $1 \le i, j \le N$, in (5) can be expressed in rational-form, as shown below:

$$Y_{ij}(s) = \frac{b_{ijq}s^q + \cdots + b_{ij1}s + b_{ij0}}{s^q + a_{ij(q-1)}s^{q-1} + \cdots + a_{ij1}s + a_{ij0}}. \quad (6)$$

In the following sections, the pre-characterization of interconnects using y-parameter descriptions is detailed. These y-parameters are calculated using the AWE technique applied to the equivalent lumped circuit models of interconnection networks and are shown to be quite accurate, and yet general enough, to handle most of complicated LLF networks. Also, stability issues related to these y-parameters are discussed.

A. Interconnect Pre-Characterization

To begin, the original circuit is roughly partitioned into nonlinear and linear subcircuits, the latter including all the different classes of interconnect that can be present. Each linear, connected subcircuit is then modeled using the appropriate equivalent lumped-circuit models. The terminal nodes of this model, corresponding to the terminal nodes of the linear subcircuit in the original circuit partition, are identified. Based on these terminal nodes, the y-parameter description of the subcircuit is obtained.

The generation of the y-parameters for a specified multiport network is achieved by exciting the network with an impulse voltage at one of the ports while shorting all other ports. Measuring the currents at each of the ports then yields one column of the Y-matrix. This procedure is repeated at each of the network ports to obtain the complete description. Some reduction in computational effort can be achieved by noting that for reciprocal networks consisting only of bilateral, linear passive elements, $Y_{ij}(s) = Y_{ji}(s)$.

Using AWE, each entry of the Y-matrix in (5) is approximated by a reduced-order model of the form:

$$\tilde{Y}_{ij}(s) \approx \sum_{m=1}^{q} \frac{\tilde{k}_{(ij)m}}{(s+\tilde{p}_m)} + d = \frac{b_{ijq}s^q + \cdots + b_{ij1}s + b_{ij0}}{s^q + a_{q-1}s^{q-1} + \cdots + a_1 s + a_0}, \quad (7)$$

where $1 \leq i, j \leq N$, $\tilde{p}$ and $\tilde{k}$ are the dominant pole and corresponding residue approximations, respectively, q is the order of approximation, and d represents any direct coupling between ports. The order of approximation can be determined through the iteration that terminates when the magnitude of the largest pole in the AWE approximation becomes greater than $\omega_{\max}$. The development of this reduced-order, rational-function model is such that it largely retains the asymptotic behavior of the original N-port network.

To avoid the computational expense of calculating pole approximations at every port, a common set of dominant poles at all the nodes of the circuit is assumed. The concept of the *common denominator* can be validated by the following arguments:

1) for the *numerical* simulation of circuits, we can assume there is no cancellation between pole-factors and zero-factors,
2) private-pole[1] factors in $Y_{ii}(s)$, $1 \leq i \leq N$, can be artificially inserted as cancelling factors in both the denominator and numerator of $Y_{ij}(s), 1 \leq i \neq j \leq N$.

Calculation of the common denominator is facilitated by the use of *moment-shifting* method, as described in [1], to obtain accurate small-magnitude pole approximations using AWE. Further increase in computational efficiency can be obtained through the use of highly efficient implementations of AWE, such as the Rapid Interconnect Circuit Evaluator (RICE).

B. y-Parameter Stability Issues

For the subsequent discussion, it is necessary to define the following terminology:

Definition 1: If the driving-point impedance $Z(s)$, of a one-port LLF network Ξ, has all its poles in the left-half of the s-plane, then Ξ is called open-circuit stable (OCS) [17].

Definition 2: If the driving-point admittance $Y(s)$, of a one-port LLF network Ξ, has all its poles in the left-half of the s-plane, then Ξ is short-circuit stable (SCS) [17].

Definition 3: A one-port LLF network is called internally stable if it is OCS and SCS.

[1]Private poles are defined as the poles in $Y_{ii}(s)$ but not in $Y_{ij}(s), i \neq j$. This situation occurs if there is any shunt-connected network at any port [32].

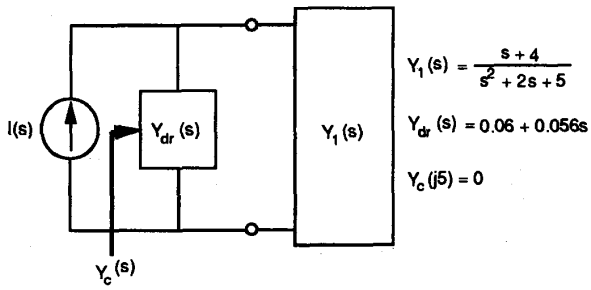


Fig. 3. An example network that shows a potential instability.

As described in the previous section, an interconnect can be asymptotically pre-characterized as a multiport described by rational-function, s-domain, y-parameters, which in turn can be interpreted to represent an LLF network. Each element of this Y-matrix, denoted as $\tilde{Y}_{ij}$ in (7), is in fact a driving-point admittance since all other ports are short-circuit terminated except the j-th port. These $\tilde{Y}_{ij}$ can be assured to be SCS by the combination of a partial-Padé technique and a moment-shifting method, as documented in [1]. However, when a stable, LLF network is attached to other stable LLF networks, such as the internal impedance of a driving gate, the overall system stability may change. As an example, a one-port network, $Y_1(s)$, which is internally stable, is shown in Fig. 3 connected in parallel to a driving-point impedance $Y_{\rm dr}(s)$, composed only of passive LLF elements (i.e., a stable network). Checking the roots of the combined admittance, $Y_c(s) = Y_{\rm dr}(s) + Y_1(s)$, as seen by the driving source, it is seen that the stability of the combined system cannot be assured. In this context, we define the following terminology:

Definition 4: A multi-port LLF network Ξ, is unconditionally stable if it is internally stable at every port, for all possible passive, terminating impedances.

Definition 5: An LLF network Ξ, is potentially unstable if it is not unconditionally stable.

For the class of *reciprocal* LLF networks, a multi-port is unconditionally stable if, and only if it is passive [25]. The forms of the y-parameters obtained using AWE, are reduced-order models characterizing the original higher-order, linear, passive interconnect circuits, which can, however, correspond to either active or passive networks. Hence, though the y-parameters themselves are internally stable, the overall multi-port realization may be potentially unstable. In this respect, the following tests on the y-parameters obtained using AWE are proposed in order to reduce the possibility of potential instability during simulation.

The necessary conditions for the y-parameters of a reciprocal LLF network to be unconditionally stable are:

Property 1: $Y_{ii}(s), 1 \leq i \leq N$, are positive-real functions,

Property 2: $Y_{ij}(s), 1 \leq i \neq j \leq N$, are real functions of s,

Property 3: for a two-port network, the real parts of y-parameters are related by:

$$\varphi_{11}\varphi_{22} - \varphi_{12}^2 > 0 \quad (8)$$

for all values of ω, where φ_{ij} is the real part of $Y_{ij}(j\omega)$ [15].

Property 1 can be easily proved if we consider the fact that an N-port network is converted to a one-port network

by shorting all other ports except one, and driving-point immittances of passive one-ports are always positive-real functions. Assuming a common set of poles, Property 1 can be translated to the following set of conditions, in terms of the a- and b-coefficients in the rational-function description in (7):
Condition 1.1 each $Y_{ii}(s)$ is internally stable, and
Condition 1.2

$$A_1(\omega^2) = \sum_{k=0}^{q} (-1)^k \left[\sum_{m=0}^{2k} a_m b_{ii(2k-m)} \right] \omega^{2k} > 0 \quad (9)$$

for all values of ω.

Property 3 can also be reduced to a similar form:

$$\begin{aligned} A_2(\omega^2) = &\left[\sum_{k=0}^{q} (-1)^k \left(\sum_{m=0}^{2k} a_m b_{11(2k-m)} \right) \omega^{2k} \right] \\ &\times \left[\sum_{k=0}^{q} (-1)^k \left(\sum_{m=0}^{2k} a_m b_{22(2k-m)} \right) \omega^{2k} \right] \\ &- \left[\sum_{k=0}^{q} (-1)^k \left(\sum_{m=0}^{2k} a_m b_{12(2k-m)} \right) \omega^{2k} \right]^2 > 0 \end{aligned} \quad (10)$$

for all values of ω.

The condition, $A_i(\omega^2) > 0$, for all ω, can be easily tested using Sturm's theorem [15]. Property 3 can be extended to multi-port cases, but it does not yield a termination-independent form such as (8). From these properties, it is seen that the stability of a multi-port network does not change under arbitrary lossless terminations [27].

IV. y-Parameter Macromodels

This section addresses the development of time-domain, macromodel stencils within the environment of general-purpose circuit simulators, with y-parameters obtained using the methods explained in the previous section. The proposed development is accomplished through the combination of a canonical realization technique and numerical integration methods [12]. The resultant macromodels are fully compatible with general-purpose circuit simulators, optimal in size (containing the terminal nodes only), and successful at minimizing the difficulties associated with stiff circuits.

Following the development of the macromodels, the local truncation error (LTE) associated with these macromodels are analyzed, which is used for adjusting the simulation time-step in some simulators. In addition, the numerical scaling method that help minimize the associated numerical errors is discussed. Finally, an enhancement of these macromodels, to include the pure delay factor that is present in the responses of transmission lines, is presented.

A. A Simple Synthesis Example

For purposes of clarity, a synthesis procedure is explained using 2nd-order AWE approximations for the y-parameters of a 1-port network, i.e., a driving-point synthesis. Extensions to multi-port networks are described in the section that follows.

The port voltage and current of a 1-port are related by the expression:

$$\begin{aligned} I_{\text{in}}(s) &= \tilde{Y}_{\text{in}}(s) \cdot V_{\text{in}}(s) \\ &= \frac{b_2 s^2 + b_1 s + b_0}{s^2 + a_1 s + a_0} \cdot V_{\text{in}}(s) \end{aligned} \quad (11)$$

Let

$$\phi(s) = \frac{V_{\text{in}}(s)}{s^2 + a_1 s + a_0}. \quad (12)$$

Assuming zero initial conditions, the differential equation corresponding to (12) is

$$\ddot{\phi}(t) + a_1 \dot{\phi}(t) + a_0 \phi(t) = v_{\text{in}}(t). \quad (13)$$

We can define two internal state variables as follows:

$$\begin{aligned} x_1(t) &= \dot{x}_2(t), \\ x_2(t) &= \phi(t). \end{aligned} \quad (14)$$

Combining (13) and (14), we have:

$$\begin{aligned} \dot{x}_1(t) &= v_{\text{in}}(t) - a_1 x_1 - a_0 x_2, \\ \dot{x}_2(t) &= x_1(t). \end{aligned} \quad (15)$$

Then, the 2nd-order system given by (11) can be realized in the time-domain using a controller canonical form [11], where the port current in terms of these state variables is expressed as:

$$i_{\text{in}}(t) = b_2 \ddot{\phi}(t) + b_1 \phi(t) + b_0 \phi(t), \quad (16)$$

or

$$i_{\text{in}}(t) = b_2 \dot{x}_1(t) + b_1 x_1(t) + b_0 x_2(t). \quad (17)$$

To relate the state variables x_i, $i = 1, 2$, with the port current and voltage, x_i is evaluated at $t = t_k$ as follows:

$$x_i(t_k) = x_i(t_{k-1}) + \int_{t_{k-1}}^{t_k} \dot{x}_i(\tau) d\tau, \quad i = 1, 2. \quad (18)$$

Assuming the trapezoidal integration method, and substituting (15) into (18) yields the updating rule for the internal state variables:

$$\begin{aligned} x_1(t_k) = \frac{1}{\Omega_{k-1}} \Bigg[&\frac{h_{k-1}}{2} \{ v_{\text{in}}(t_{k-1}) + v_{\text{in}}(t_k) \} \\ &\times \left\{ 1 - \left(\frac{h_{k-1}}{2} \right) a_1 - \left(\frac{h_{k-1}}{2} \right)^2 a_0 \right\} \\ &\times x_1(t_{k-1}) - a_0 h_{k-1} x_2(t_{k-1}) \Bigg], \\ x_2(t_k) = x_2(t_{k-1}) + &\frac{h_{k-1}}{2} [x_1(t_{k-1}) + x_1(t_k)], \end{aligned} \quad (19)$$

where $h_{k-1} = (t_k - t_{k-1}), k \geq 1$, is the internal time-step of the base simulator, and

$$\Omega_{k-1} = \left[1 + \left(\frac{h_{k-1}}{2} \right) a_1 + \left(\frac{h_{k-1}}{2} \right)^2 a_0 \right]. \quad (20)$$

Plugging (15) and (19) into (17) yields the equation describing the macromodel in the circuit simulator:

$$i_{\text{in}}(t_{k+1}) = G_{\text{eq}}(t_k) v_{\text{in}}(t_{k+1}) + I_{\text{eq}}(t_k), \quad (21)$$

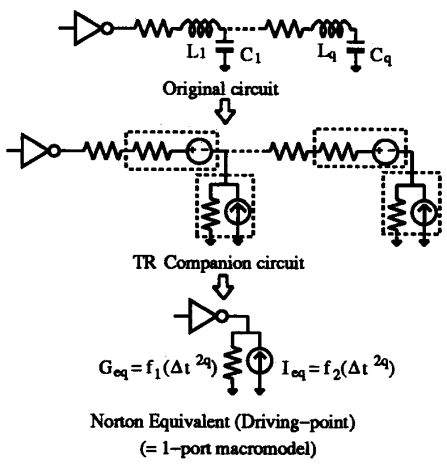


Fig. 4. Computing the equivalent Norton circuit at the driving-point of a simple interconnect circuit.

where G_{eq} and I_{eq} are as specified in (22) and (23).

$$G_{\text{eq}}(t_k) = b_2 - \frac{1}{\Omega_k} \times \left[\left(\frac{h_k}{2}\right)(b_2a_1 - b_1) + \left(\frac{h_k}{2}\right)^2 (b_2a_0 - b_0)\right], \tag{22}$$

$$\begin{aligned} I_{\text{eq}}(t_k) = {} & -(b_2 - G_{\text{eq}}(t_k))v_{\text{in}}(t_k) \\ & - \frac{1}{\Omega_k}\left[(b_2a_1 - b_1)\left\{1 - \left(\frac{h_k}{2}\right)a_1 - \left(\frac{h_k}{2}\right)^2 a_0\right\}\right. \\ & \left. + h_k(b_2a_0 - b_0)\right]x_1(t_k) \\ & - \frac{1}{\Omega_k}\left[(b_2a_0 - b_0)\left\{1 + \left(\frac{h_k}{2}\right)a_1 - \left(\frac{h_k}{2}\right)^2 a_0\right\}\right. \\ & \left. - a_0h_k(b_2a_1 - b_1)\right]x_2(t_k). \end{aligned} \tag{23}$$

In the case of a driving-point synthesis, the macromodel thus obtained, (22) and (23), is a Norton equivalent circuit at the driven network port. If this driving-point admittance is physically realizable, the description of (22) and (23) is equivalent to replacing energy storage elements by their numerical integration companion models and then collapsing the circuit at the driving-point (see Fig. 4).

B. Macromodel Development

In the s-domain, the relationship between the port current and voltage at the pth-port of an N-port network, described by the y-parameters can be expressed as:

$$I_p(s) = \sum_{j=1}^{j=N} Y_{pj}(s) \cdot V_j(s), \quad 1 \le p \le N. \tag{24}$$

Assuming the notation for each $Y_{pj}(s)$ as in (7)[2] and zero initial conditions,[3] the N-port network can be realized in controller-canonical form, as shown in Fig. 5.

Corresponding to the above system, the following set of internal state variables are defined at each port:

$$\begin{aligned} \dot{x}_{i1}(t) &= v_i(t) - \sum_{j=0}^{q-1} a_j x_{i(q-j)}(t), \\ \dot{x}_{ij}(t) &= x_{i(j-1)}(t), \quad 1 \le i \le N, \ 2 \le j \le q. \end{aligned} \tag{25}$$

Then, the port current, at the pth-port, in terms of these state variables is given by:

$$i_p(t) = \sum_{i=1}^{N} \left[b_{piq}\dot{x}_{i1} + \sum_{j=0}^{q-1} b_{pij}x_{i(q-j)}(t)\right], \qquad 1 \le p \le N. \tag{26}$$

To obtain expressions for the state variables x_{ij} in terms of the port parameters, the values of x_{ij} are evaluated at $t = t_k$ as follows:

$$x_{ij}(t_k) = x_{ij}(t_{k-1}) + \int_{t_{k-1}}^{t_k} \dot{x}_{ij}(\tau)d\tau, \ \ 1 \le i \le N, \ \ 1 \le j \le q. \tag{27}$$

Various numerical integration methods can be used for integrating (27), including Backward Euler (BE), Forward Euler (FE) or TRapezoidal (TR) methods, or multi-step methods such as Gear's second-order or Runge-Kutta's method [18]. The precise selection of the integration scheme used may depend on that employed in the base simulator.

Assuming the TR method of integration, and substituting (25) into (27) yields the updating rule for the internal state variables:

$$\begin{aligned} x_{i1}(t_k) = {} & \frac{1}{\Omega_{k-1}}\left[\frac{h_{k-1}}{2}\{v_i(t_{k-1}) + v_i(t_k)\}\right. \\ & + (2 - \Omega_{k-1})x_{i1}(t_{k-1}) \\ & - h_{k-1}\sum_{m=0}^{q-2}\left\{x_{i(m+2)}(t_{k-1})\right. \\ & \left.\left.\times\left(\sum_{l=0}^{q-m-2}\left(\frac{h_{k-1}}{2}\right)^l a_{q-m-l-2}\right)\right\}\right], \\ x_{ij}(t_k) = {} & x_{ij}(t_{k-1}) + \frac{h_{k-1}}{2}\left[x_{i(j-1)}(t_{k-1}) + x_{i(j-1)}(t_k)\right], \\ & 1 \le i \le N, \quad 2 \le j \le q, \end{aligned} \tag{28}$$

where $h_{k-1} = (t_k - t_{k-1})$, and

$$\Omega_{k-1} = \sum_{l=0}^{q}\left(\frac{h_{k-1}}{2}\right)^l a_{q-l}.$$

Substituting (25) and (28) into (26) yields the equation characterizing the pth-port in the time-domain macromodel:

$$\begin{aligned} i_p(t_{k+1}) = {} & G_{p(\text{eq})}(t_k)v_p(t_{k+1}) + \sum_{j=1, j\ne p}^{N} g_{pj}(t_k)v_j(t_{k+1}) \\ & + I_{p(\text{eq})}(t_k), \qquad 1 \le p \le N, \end{aligned} \tag{29}$$

[2]This macromodeling method is not limited to the case of common set of poles, and the extension of the method to the case of different set of poles is straightforward.

[3]Nonzero initial conditions affect only the constant b_{ij0} term in (7) and can be easily incorporated if the derivatives of either the port current or voltage at t_0 are available.

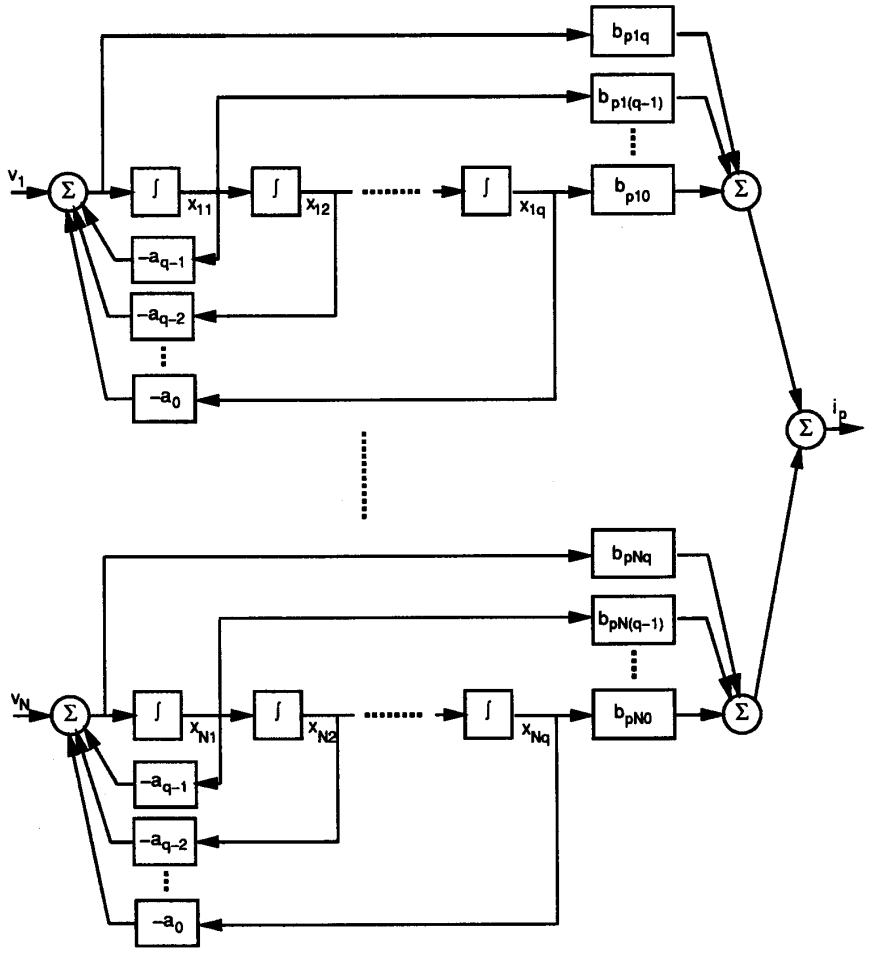


Fig. 5. Port realization at pth-port in an N-port network with controller canonical form.

where $G_{p(\mathrm{eq})}$, g_{pj}, and $I_{p(\mathrm{eq})}$ are represented by (30), (31), and (32), respectively.

$$G_{p(\mathrm{eq})}(t_k) = b_{ppq} - \frac{1}{\Omega_k}\sum_{l=1}^{q}\left(\frac{h_k}{2}\right)^l \alpha_{pp(q-l)}, \tag{30}$$

$$g_{pj}(t_k) = b_{pjq} - \frac{1}{\Omega_k}\sum_{l=1}^{q}\left(\frac{h_k}{2}\right)^l \alpha_{pj(q-l)}, \tag{31}$$

where

$$\begin{aligned} \alpha_{pij} &= b_{piq}a_j - b_{pij}. \\ I_{p(\mathrm{eq})}(t_k) &= \left[G_{p(\mathrm{eq})}(t_k) - b_{ppq}\right]v_p(t_k) \\ &\quad + \sum_{j=1,j\neq p}^{N}\left[g_{pj}(t_k) - b_{pjq}\right]v_j(t_k) \\ &\quad + \frac{1}{\Omega_k}\sum_{i=1}^{N}\sum_{j=1}^{q}\beta_{pij}(t_k)x_{ij}(t_k), \end{aligned} \tag{32}$$

where

$$\begin{aligned} \beta_{pij}(t_k) = h_k &\sum_{m=0}^{j-2}\left\{\alpha_{pi(q-m-1)}\left(\frac{h_k}{2}\right)^m \sum_{l=0}^{q-j}\left(\frac{h_k}{2}\right)^l a_{q-j-l}\right\} \\ &- \alpha_{pi(q-j)}\left\{\sum_{l=0}^{j-1}\left(\frac{h_k}{2}\right)^l a_{q-l} - \sum_{l=j}^{q}\left(\frac{h_k}{2}\right)^l a_{q-l}\right\} \\ &- h_k\sum_{m=0}^{q-j-1}\left\{\alpha_{pi(q-m-j-1)}\left(\frac{h_k}{2}\right)^m \right. \\ &\qquad \left. \times \textstyle\sum_{l=0}^{j-1}\left(\frac{h_k}{2}\right)^l a_{q-l}\right\}. \end{aligned} \tag{33}$$

These elements correspond to a conductance, a set of voltage-controlled current sources, and a current source in the multi-port macromodel, as shown in the 2-port macromodel in Fig. 6. The transfer conductance term, g_{pj}, in (29) represents the influence of the jth-port on the pth-port of the network.

Since the transient analysis of a circuit begins with finding a dc solution at t_0 for the circuit, the corresponding macromodel stencils need also to be defined. This is done by setting $t_k = t_0$

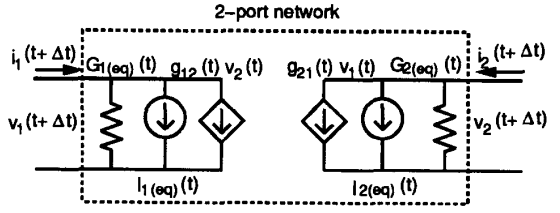


Fig. 6. 2-port macromodel stencil of an interconnect for circuit simulation.

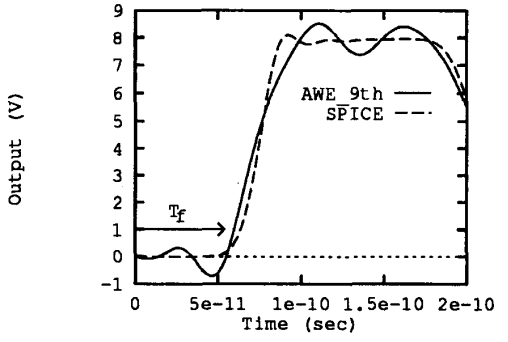


Fig. 7. Macromodel output response of a low-loss line ($R_t = 10.53\ \Omega$, $L_t = 2.9$ nH, $G_t = 0\ \Omega$, $C_t = 1.17$ pF, length = 1 cm) using 9th-order AWE y-parameter approximation. The line was driven by a saturated ramp with $t_r = 20$ ps, through $R_{\rm dr} = 5.0\ \Omega$, and terminated with a capacitance of 0.1 pF.

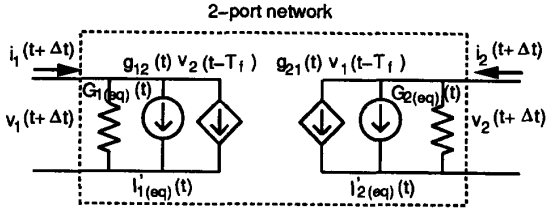


Fig. 8. Two-port, modified macromodel stencils incorporating propagation delay T_f.

and taking the limit as $h_k \to \infty$ in (30)–(33), and where $x_{ij}(t_0^-)$ is obtained by setting $\dot{x}_{ij}(t_0^-) = 0$ in (25). This yields:

$$\begin{aligned} x_{iq}(t_0^-) &= \frac{v_i(t_0^-)}{a_0};\ \ x_{ik}(t_0^-) = 0,\ \ 1 \le k \le q-1, \\ G_{i(\mathrm{eq})}(t_0) &= \frac{b_{iiq}}{a_0}, \\ g_{ij}(t_0) &= \frac{b_{ijq}}{a_0},\ \ 1 \le j \le N,\ \ j \ne i, \\ I_{i(\mathrm{eq})}(t_0) &= 0, \end{aligned} \tag{34}$$

where $1 \le i \le N$.

C. LTE Analysis

Conventional circuit simulators, such as SPICE, employ measures of the local truncation error to control the time-steps in simulation. Since estimating the LTE for the TR integration method requires the 3rd-derivatives of the node variables, information about the energy-storing-device nodes at four time-points (the current and three previous time-points) is stored [18]. A similar technique can be employed to estimate the LTE for the port currents in macromodels. Assuming the previously calculated values are exact, as done in SPICE, the LTE for $x_{ij}(t_k)$, denoted as $\epsilon_{ij}(t_k)$, is given by

$$\epsilon_{ij}(t_k) \approx \frac{h_{k-1}^3}{12} \cdot \frac{d^3 x_{ij}(\xi)}{dt^3}, \qquad 1 \le i \le N,\quad 1 \le j \le q, \tag{35}$$

where $t_{k-1} < \xi < t_k$. The 3rd-derivative in (35) is approximated by fitting a 3rd-order polynomial to the values of $\vec{x}_i$ at t_k, t_{k-1}, t_{k-2}, and t_{k-3}. This yields the following equation [18]:

$$\frac{d^3 \vec{x}_i(\xi)}{dt^3} \approx 6 \cdot D_3[\vec{x}_i(t_k)], \qquad 1 \le i \le N, \tag{36}$$

where D_3 stands for 3rd divided-difference equation and is represented by:

$$\begin{aligned} D_n[\vec{x}_i(t_k)] &= \frac{D_{n-1}[\vec{x}_i(t_k)] - D_{n-1}[\vec{x}_i(t_{k-1})]}{\sum_{i=1}^{n} h_{k-i}}, \\ D_1[\vec{x}_i(t_k)] &= \frac{\vec{x}_i(t_k) - \vec{x}_i(t_{k-1})}{h_{k-1}}, \qquad 1 \le i \le N. \end{aligned} \tag{37}$$

To evaluate (36) more efficiently, the values of the divided-difference vectors of $\vec{x}_i$ can be stored in place of $\vec{x}_i$.

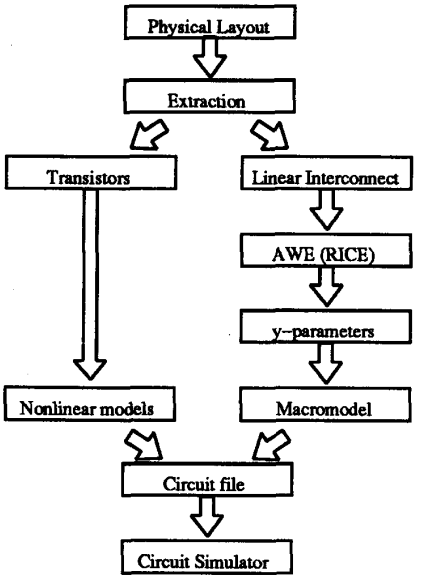
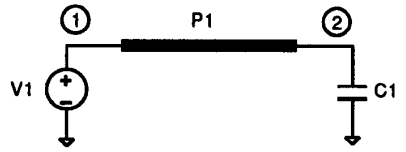


Fig. 9. Program organization of enhanced simulator incorporating interconnect macromodels.

D. Numerical Tuning of Macromodels

For the practical values of the parasitic elements found in interconnect circuits and transmission line models, the




```
*Lossy interconnect macromodel
*Ramp voltage driver
V1 1 0 PULSE(0 1 0 1e-9)
*Transmission-line macromodel
P1 2 1 0 2 0 TL1
*Load capacitor
C1 2 0 1e-12 0.0
*Model specification of multiport macromodel
.MODEL TL1 ORDER=4 TF=5.82e-11 SF=1.67e+11
+        DENOM=(1.0 1.0 4.83e-01 1.15e-01 1.31e-02)
+        Y11=(2.0e-02 8.71e-04 8.84e-03 1.92e-04 2.16e-04)
+        Y12=(0 0 0 0 -2.16e-04)
+        Y21=(0 0 0 0 -2.16e-04)
+        Y22=(2.0e-02 8.71e-04 8.84e-03 1.92e-04 2.16e-04)
.END
```

Fig. 10. Example specification of a lossy interconnect using the macromodeling approach.

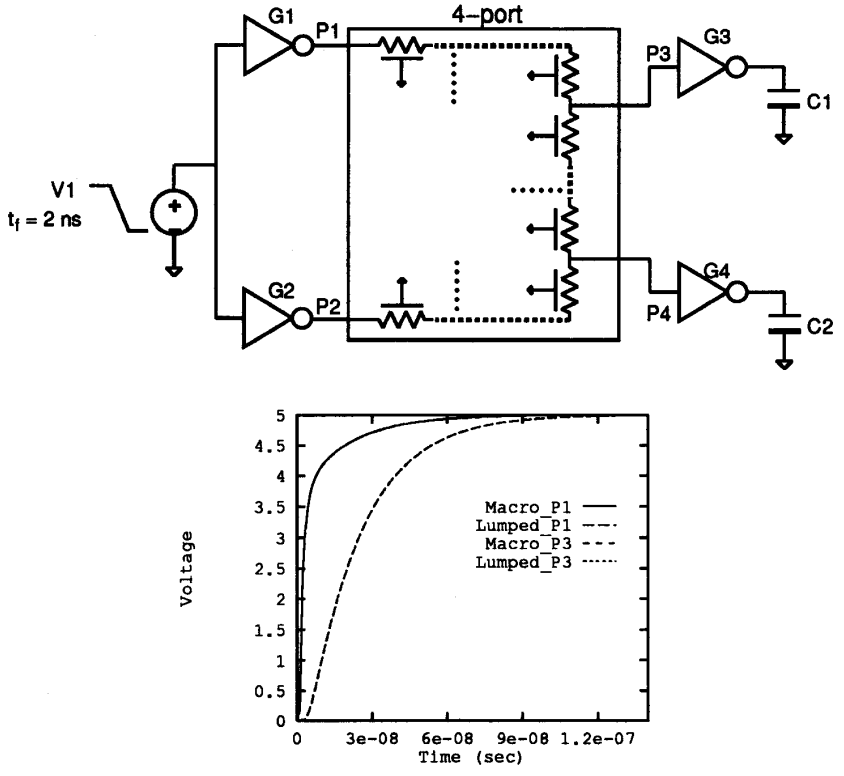


Fig. 11. A clock distribution network with nonlinear MOS drivers and terminations.

TABLE I
COMPARISON OF THE NUMBER OF NODES AND CPU TIMES

Circuit	# of nodes		# of transistors	Run-time (sec)		Ratio of run-time
	Lumped ckt	Macromodel		Lumped ckt	Macromodel	
Fig. 11	8007	8	8	4570.20	11.90	384.05
Fig. 13	342	7	4	79.86	7.88	10.13
Fig. 14	96	13	12	65.98	41.77	1.58

magnitudes of y-parameter coefficients, a_i and b_{ijk} in (36), are monotonically increasing, as shown below.

$$\begin{aligned}\texttt{Denom} &= 1.0s^4 + 1.67\texttt{e}11s^3 + 1.35\texttt{e}22s^2 + 5.36\texttt{e}32s \\ &\quad + 1.02\texttt{e}43 \\ \texttt{Numer} &= 2.00\texttt{e}{-}02s^4 + 1.47\texttt{e}08s^3 + 2.47\texttt{e}20s^2 \\ &\quad + 8.98\texttt{e}29s + 1.69\texttt{e}41\end{aligned}$$

As the orders of approximation of y-parameters required to adequately model (R)LC-class interconnection networks are typically higher than those required for RC-interconnects, the coefficients of the y-parameters approximations for the former network may have a wide dynamic range. This phenomenon results in the so-called *dynamic range problems* [34] and is more evident in transmission lines and similar low-loss, closely matched, strongly coupled systems. Hence, to minimize numerical limitations on the macromodels, a method of numerical tuning of these y-parameter coefficients, is necessary.

In order to effect this, a frequency scaling factor, γ, is defined as:

$$\gamma = \frac{a_{q-1}}{a_q}. \tag{38}$$

Then the new set of scaled denominator and numerator coefficients (denoted as a'_i and b'_{ijk}) is defined as:

$$\begin{aligned} a'_i &= \frac{a_i}{\gamma^{q-i}}, \\ b'_{ijk} &= \frac{b_{ijk}}{\gamma^{q-k}}, \\ \alpha'_{ijk} &= b'_{ijq}a'_k - b'_{ijk} = \frac{\alpha_{ijk}}{\gamma^{q-k}}, \end{aligned} \tag{39}$$

where $1 \le i,\ j \le N$, and $1 \le k \le q$. This change in coefficients causes simple modifications in equations (28) and (30)–(33): all the terms involving the multiplication of a-, b- or α-coefficients and time-step, h_k, are changed as in the example shown below:

$$\left(\frac{h_k}{2}\right)^l \alpha_{pj(q-l)} \Rightarrow \left(\frac{h_k}{2}\gamma\right)^l \alpha'_{pj(q-l)}. \tag{40}$$

As seen in (40), this change of coefficients prevents the exponents of the floating-point numbers from growing at each evaluation stage, thereby preserving numerical precision. The above example is shown again now with the frequency scaling factor incorporated:

$$\begin{aligned}\texttt{Denom} &= 1.0s^4 + 1.0s^3 + 4.83\texttt{e}{-}01s^2 \\ &\quad + 1.15\texttt{e}{-}01s + 1.31\texttt{e}{-}02 \\ \texttt{Numer} &= 2.00\texttt{e}{-}02s^4 + 8.71\texttt{e}{-}04s^3 \\ &\quad + 8.84\texttt{e}{-}03s^2 + 1.92\texttt{e}{-}04s \\ &\quad + 2.16\texttt{e}{-}04 \\ \texttt{Scale Factor} &= 1.67\texttt{e}11\end{aligned}$$

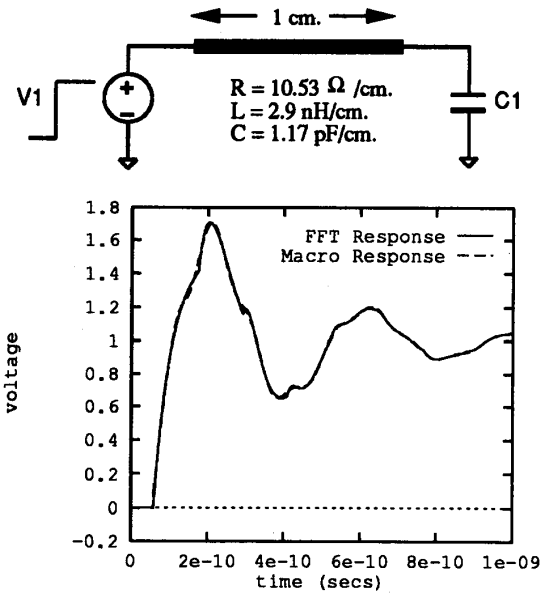


Fig. 12. Comparison of the result of the macromodeling method against the FFT response.

E. Incorporating Transmission-Line Delays

As discussed in Section III.B, the physical realization of the AWE y-parameters can represent active networks, which can result in spurious ringing or unstable behavior for some passive source impedances. For transmission line models, this is evidenced as nonphysical ringing during the *time-of-flight* [3], denoted as T_f, which is also known as *phase delay* and represents a *pure* delay factor. For instance, using AWE approximations for the y-parameters results in the nonphysical ringing during $0 \le t \le T_f$, as shown in Fig. 7.

This ringing is especially significant in the case of fast-rising signals and can be attributed to the truncation and numerical errors associated with the reduced-order models for the y-parameters obtained using AWE, which may have triggered the transformation from a passive network to an active network representation.

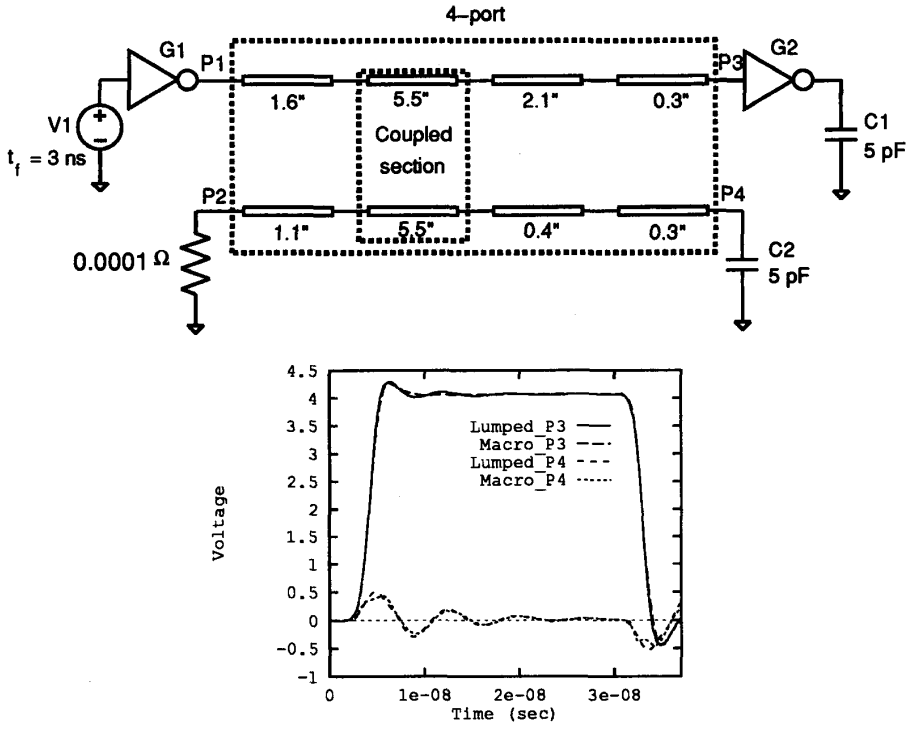


Fig. 13. An interconnect configuration with lossy, coupled transmission lines, extracted in lumped parameters.

One possible approach to minimizing the oscillations for $t < T_f$, is to first extract the time-of-flight for the given transmission-line configuration and artificially incorporate it into the macromodel [3], [13]. For a single transmission line, a lower bound for the time-of-flight across the line is given by $\sqrt{L_t C_t} \leq T_f$, where L_t and C_t are the total inductance and capacitance of the line. This delay can be incorporated in the equivalent macromodel by the introduction of delay elements (implemented using simple circular queues [3]), as shown in Fig. 8. The time-domain equation characterizing the pth-port in this modified N-port macromodel is:

$$i_p(t_{k+1}) = G_{p(\mathrm{eq})}(t_k)v_p(t_{k+1}) + I'_{p(\mathrm{eq})}(t_k) + \sum_{j=1, j\neq p}^{N} g_{pj}(t_k)v_j(t_{k+1} - T_f), \quad 1 \leq p \leq N, \tag{41}$$

where $I'_{p(\mathrm{eq})}(t_k)$ is given by:

$$\begin{aligned} I'_{p(\mathrm{eq})}(t_k) = {} & \left[G_{p(\mathrm{eq})}(t_k) - b_{ppq}\right]v_p(t_k) \\ & + \frac{1}{\Omega_k}\sum_{j=1}^{q}\beta_{ppj}(t_k)x_{pj}(t_k) \\ & + \sum_{j=1, j\neq p}^{N}\left[g_{pj}(t_k) - b_{pjq}\right]v_j(t_k - T_f) \\ & + \frac{1}{\Omega_k}\sum_{i=1, i\neq p}^{N}\sum_{j=1}^{q}\beta_{pij}(t_k)x_{ij}(t_k - T_f). \end{aligned} \tag{42}$$

V. Simulator Interface and Results

A. Simulator Interface

The macromodels proposed in this paper provide a unified, efficient simulation framework for any circuit containing passive LLF networks. The overall simulation strategy using these macromodels is depicted in Fig. 9. As seen, the multiport parameter descriptors need be computed only once for a section of interconnect, immediately following the circuit extraction stage of design verification.

The proposed macromodeling algorithm was also embedded into a SPICE-like simulator. The model card for a multi-port element in a net-list that is input to a circuit simulator, is as follows:

P⟨name⟩⟨#ports⟩⟨node 1⟩⟨node 2⟩...⟨model name⟩.

The form of the model is:

MODEL ⟨model name⟩ ORDER = (order of y-param.)
Tf = (T_f) SF = (scale factor)
+ DENOM = ($a_q a_{q-1} \ldots a_0$) Y11 = (⟨num. coeff.⟩)
Y12 = (⟨num. coeff.⟩)....

The example shown in Fig. 10 illustrates the ease of notation and compact nature of this specification. The macromodel element routines are then called at each time-step, using a routine that requires only the model information and the step size h_k. From this model, generalized MNA stencils are used to fill in the port parameters in the system matrix.

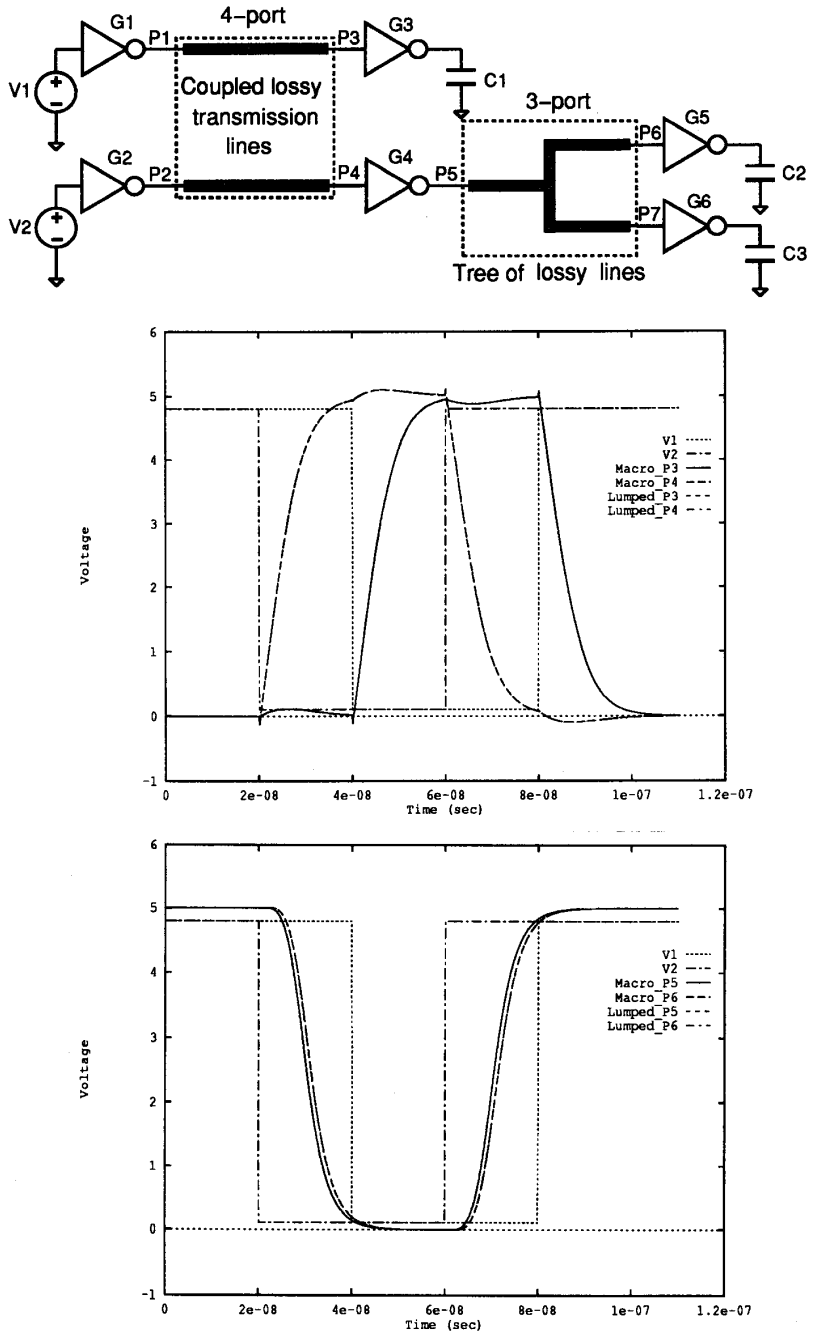


Fig. 14. Two lossy interconnect structures with multiple MOS drivers and nonlinear MOS terminations.

VI. Results

The utility of the macromodeling approach is most evident when evaluating large, stiff interconnection networks such as clock lines, power buses, etc. Fig. 11 illustrates a clock net containing nonuniform 8000 RC-segments and nonlinear drivers/terminations. The response is measured at the gate-node of one receiver represented by $P3$ in Fig. 11, when multiple excitations are present. The response waveform of a macromodel derived from 3rd-order AWE y-parameter approximations is seen to be indistinguishable from that obtained by using the original circuit.

With respect to the efficiency, evaluating the original circuit in a circuit simulator consumed inordinately long run-times, whereas using the macromodel of 3rd-order AWE approx-

imations yielded a decrease in run-time by two orders of magnitude (384 times in this example). This gain in run-time is due to the size-optimality of the macromodel since the run-time grows faster than the size of the system matrix does.

The accuracy in macromodeling RLC circuit models is demonstrated through the analysis of a length of low-loss transmission wire, driven with a perfect step voltage, and terminated by an arbitrary capacitor (see Fig. 12). Comparing the response of a macromodel with 6th-order AWE approximations of the y-parameters to that of the transmission line obtained using conventional FFT techniques shows insignificant compromise in accuracy.

Fig. 13 illustrates an interconnect configuration obtained from industry,[4] which has been extracted in a lumped circuit containing both capacitive and inductive coupling. This example shows the capability of the macromodeling approach in cases that the interconnects are extracted in the form of lumped circuits, which often occurs for simplicity. 5th-order AWE y-parameter approximation was used for the simulation of 4-port macromodel.

Macromodels of interconnection networks can be regarded as standard devices in a circuit file, so that any number of macromodels and nonlinear devices may be put together, as shown in the data path example of Fig. 14. In this case, 8th- and 6th-order AWE y-parameter approximations were considered for the 4- and 3-port, respectively. The results again show excellent accuracy in the response waveforms. The comparison results of run-times for these examples are summarized in Table I (CPU times are measured on SUN-SPARC1 station).

VII. Conclusion

Complex interconnect networks have been characterized as linear multi-ports using a reduced-order modeling approach. Based on these multi-port descriptions, a simple macromodeling method has been derived. This enables the reduction of large, stiff, RC/RLC interconnect configurations into compact representations that pose minimal problems to conventional circuit simulation techniques. The macromodel can be incorporated directly into a conventional circuit simulation with no modification of the original simulation algorithm. The techniques proposed herein are suitable for development as a software library that can be used to enhance existing simulators to handle large VLSI interconnect configurations very efficiently. In addition, the ability to handle elements at the port level makes the proposed approach extremely attractive for any linear(ized) macromodels or for applications such as mixed-mode and behavioral simulation.

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