Stability Considerations

When embarking on any amplifier design it is very important to spend time checking on the stability of the device chosen, otherwise the amplifier may well turn into an oscillator.

The main way of determining the stability of a device is to calculate the Rollett's stability factor (K), which is calculated using a set of S-parameters for the device at the frequency of operation. The calculations are long winded and it is much quicker to simulate under ADS.

The conditions of stability at a given frequency are $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$,and must hold for all possible values Γ_L & Γ_S obtained using passive matching circuits. We can calculate two Stability parameters K & $|\Delta|$ to give us an indication to whether a device is likely to oscillate or not or whether it is conditionally/unconditionally stable.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}.S_{21}|} > 1 \quad , \quad \text{where } |\Delta| = |S_{11}.S_{22} - S_{12}.S_{21}| < 1$$

The parameters must satisfy K > 1 and $|\Delta| < 1$ for a transistor to be unconditionally stable. Once we have calculated the K factor and find the device to be unconditionally stable we can calculate the Maximum available gain (MAG):-

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right)$$

Where K is on the limit of unity the above equation reduces down to:-

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|}$$

In this case the MAG is known as the maximum stable gain MSG.
In the case of the design we need to calculate the stability factor at 4 & 6GHz, however it is important to check the stability factor from low frequencies up to the f_T of the device as instabilities may occur at other frequencies even though the device is stable within the pass-band.

Evaluation of K at 4GHz

$\Delta = S_{11}.S_{22} - S_{12}.S_{21} =$ (0.862∠ - 92x0.607∠ - 61) - (0.066∠33x2.986∠97)

$= 0.5232\angle -153 - 0.19707\angle 130$ convert to cartesian for subtraction

$= (-0.23751 - j0.46617) - (0.15094 - j0.1266) = -0.38845 - j0.33957$ convert to polar

$$= \sqrt{(-0.38845)^2 + (-0.33957)^2}\angle \tan^{-1}\left(\frac{-0.38845}{-0.33957}\right) = 0.5159\angle -131.2$$

$\therefore \quad |\Delta| = 0.5159$ and $|\Delta|^2 = 0.26615$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}.S_{21}|} = \frac{1 - (0.862)^2 - (0.607)^2 + 0.26617}{2(0.066\angle 33 x 2.986\angle 97)}$$

$$= \frac{1 - 0.743 - 0.368 + 0.26617}{2(0.197\angle 130)} = \frac{0.1551}{0.394} = 0.39$$

Therefore, at 4GHz the transistor is conditionally stable as K < 1 and therefore, we will have to be careful in the way the transistor is matched.

Similarly the K factor at 6GHz was calculated to be 0.585 and $|\Delta| = 0.42$.

Now that it is known that the transistor is conditionally stable it is now necessary to calculate and plot the corresponding stability circles on a Smith chart so that the no-go areas for matches can be highlighted.

The equations for calculation of the stability circles are:-

$$r_{s1} = \frac{C_1^*}{|S_{11}|^2 - |\Delta|^2}$$ This gives the location of the centre of the input stability circle

Where $C_1 = S_{11} - \Delta.S_{22}^*$ Note * denotes complex conjugate

$$p_{s1} = \left| \frac{S_{12}.S_{21}}{|S_{11}|^2 - |\Delta|^2} \right|$$ This gives the radius of the input stability circle.

Similarily for the ouput

$$r_{s2} = \frac{C_2^*}{|S_{22}|^2 - |\Delta|^2}$$ This gives the location of the centre of the output stability circle

Where $C_2 = S_{22} - \Delta.S_{11}^*$ Note * denotes complex conjugate

$$p_{s2} = \left| \frac{S_{12}.S_{21}}{|S_{22}|^2 - |\Delta|^2} \right|$$ This gives the radius of the output stability circle.

The Figure below (figure 1) below shows the form of stability circles in relation to a Smith chart.

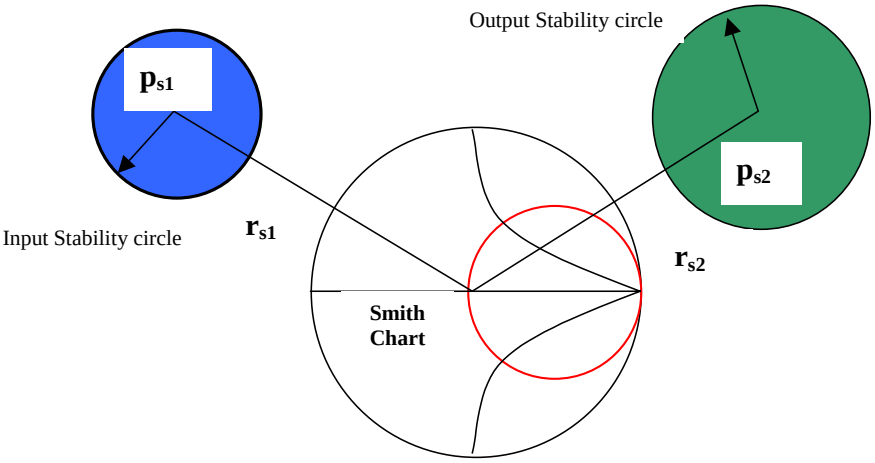


Figure 1 Stability Circles

In the above example the active device would be showing unconditional stability, as there is no intersection of the stability circles on the Smith Chart. All devices with S11 and S22 < 1 must be stable with a load impedance of 50 ohms therefore, the centre of the Smith chart must always be a stable region. In the above example the device will be stable for all possible matches on the input or output of the active device.

However, in the case where S11 or S22 > 1 and the stability circle covers the centre of the Smith chart then this region is unstable the following diagram shows the regions of instability.

The Figure below (Figure 2) shows the areas of instability with S11 <> 1 & S22<1.

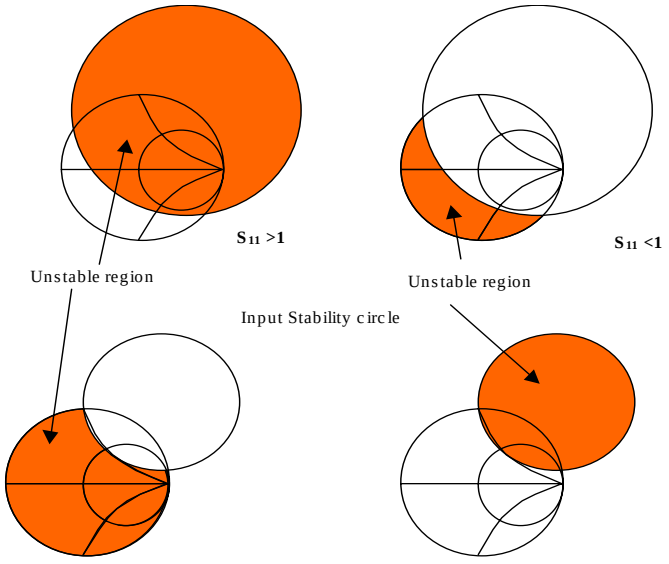


Figure 2 Areas of instabilty

Calculation of stability circles are tedious, prone to error and in addition they should be plotted across a range of frequencies – low frequency to at least the f_t of the active device. This because a match may be clear of a region of instability at the pass-band frequencies but may be in a region of instability at another out of band frequency. A common problem of FET devices is that they are conditionally stable and have the stability circles clipping the outer edge of the Smith chart. This means that if an open or short circuit is applied to the input then the device may well oscillate. This may not be a problem where a broadband load is applied but in case of antennas for example they often are open/short circuit at very low frequencies and together with the very high gain of the active device at low frequencies often leads to oscillation.

The following plots show the stability circles for a range of frequencies between 1 & 15 GHz, together with the ADS S-parameter test bench for analysing the circuit.

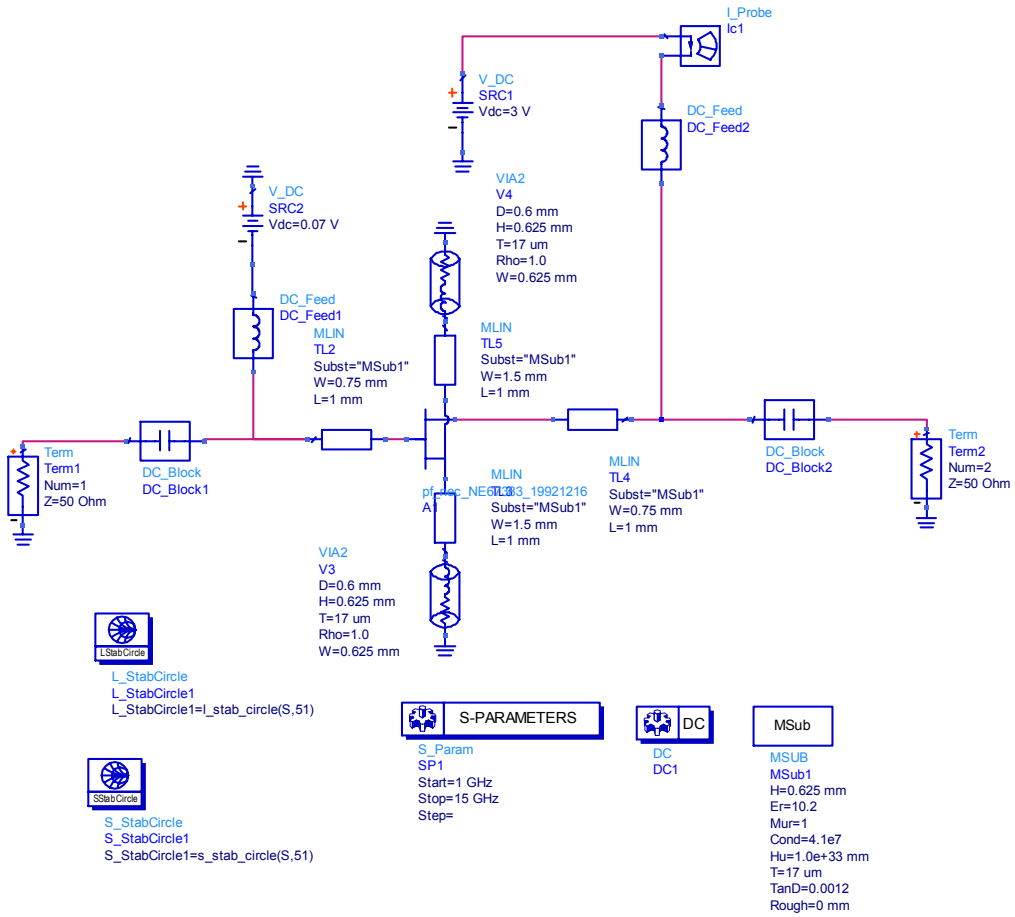


Figure 3 ADS Circuit Schematic for analysing the Stability circles.

The above figure shows the simplified ADS circuit test-bench for calculating, DC bias, S-parameters and stability circles. The FET is biased with Vd = 3V and a negative bias on the gate of –0.09V to give a drain current of ~20mA. The S-parameter block is set to sweep between 1 to 15GHz in 20 steps. The MSUB defines the microwave substrate material in this case RT Duroid 6010 25 thou thick. S_StabCircle and L_StabCircle are the input (Source) and output (Load) stability circle measurement blocks respectively.

To complete the circuit solder pads and grounding via holes have been added as will be needed to mount the device to the RT Duroid and will highlight any stability problems due to lead, solder pad, and via hole inductance

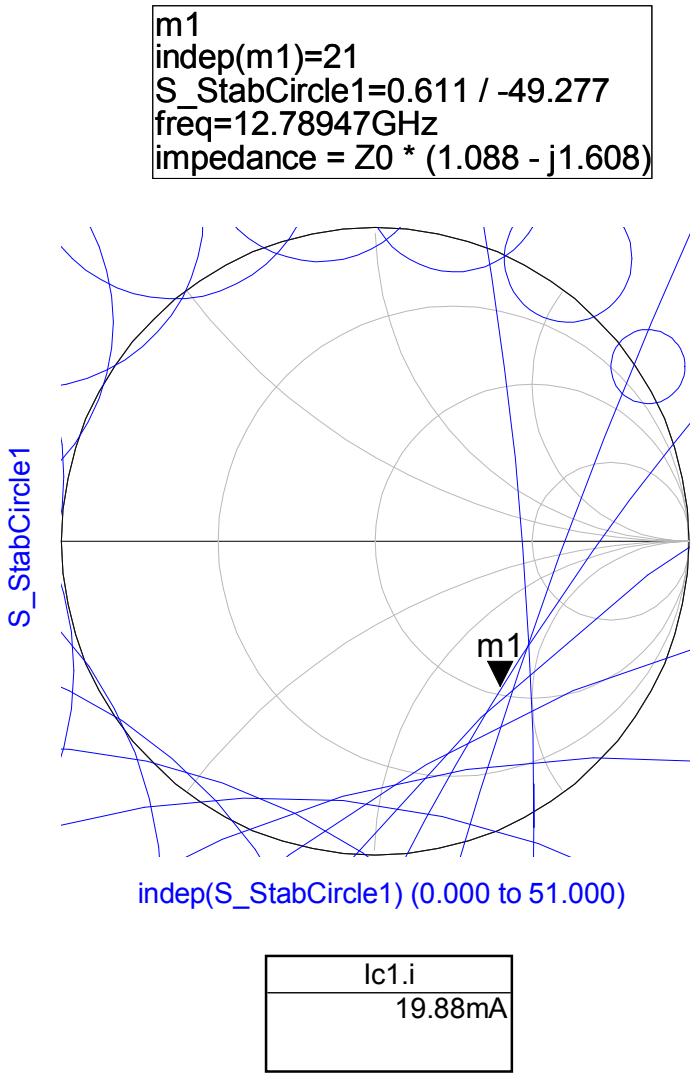


Figure 3 Input Stability Circles. From the Smith chart of input stability circles we can see that there are large areas of potential instability at high frequencies. Marker 1 is at the 12GHz stability circle and thus the smith chart to the right of the line is an area of potential instability.

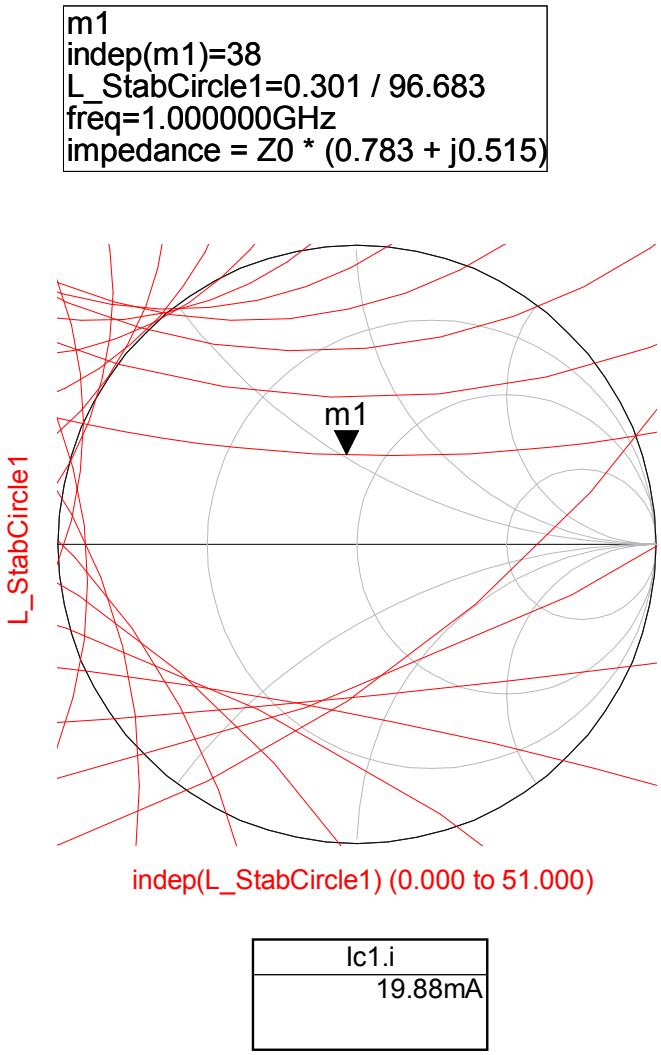
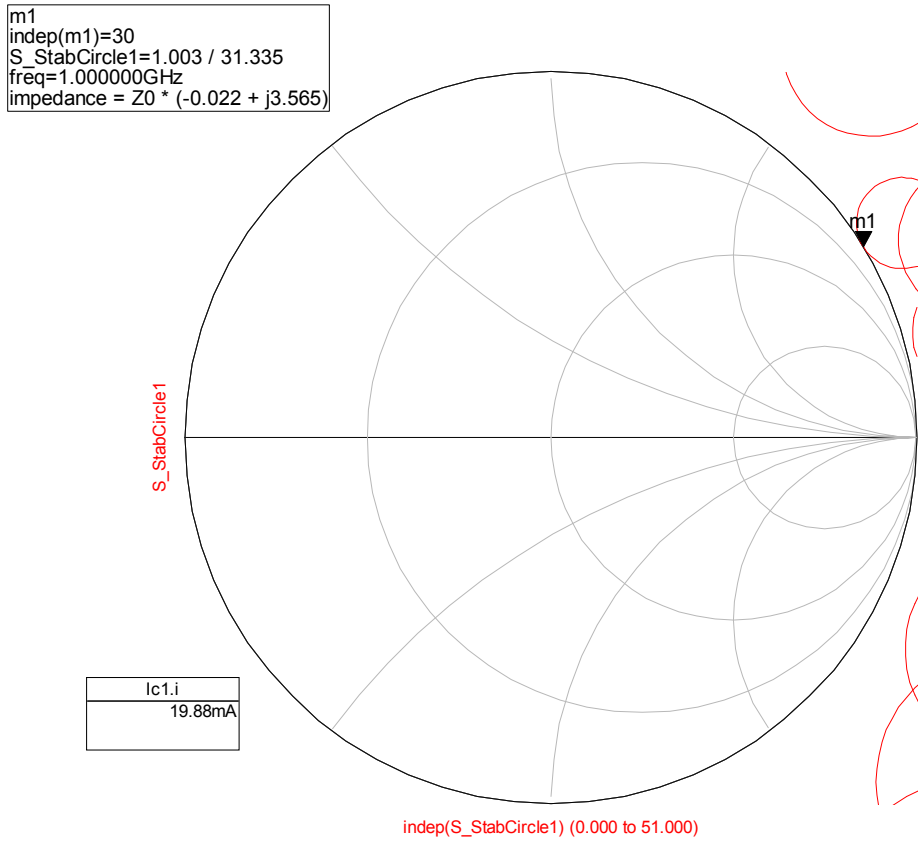


Figure 4 Output Stability Circles. From the Smith chart of output stability circles we can see that there are large areas of potential instability at low frequencies. (This is why it is difficult to design low frequency LNA's with high frequency MESFets). Marker 1 is at the 1GHz stability circle and thus the smith chart above the line is an area of potential instability

To improve the stability of the FET circuit we can add a small series resistor. A value of 35ohms ensures that the stability circles lie outside of the smith chart, ensuring that the circuit will be stable with any applied load between 1 and 15GHz.

Figure 5 Input Stability Circles with a 35Ω series resistor



The effect of the series 35-ohm resistor is to 'banish' the stability circles to the outside region of the Smith chart. This will allow us to attach any passive matching circuit with any complex load to the input of the FET without causing the device to oscillate.

However! The circuit schematic assumes that the FET source leads go straight to ground. Of course there are source leads, solder pads and via holes to provide the RF/DC ground. These have to be added to the circuit as is shown on the next ADS circuit schematic (Figure 6) and corresponding simulation result (Figure 7) showing the input stability circles.

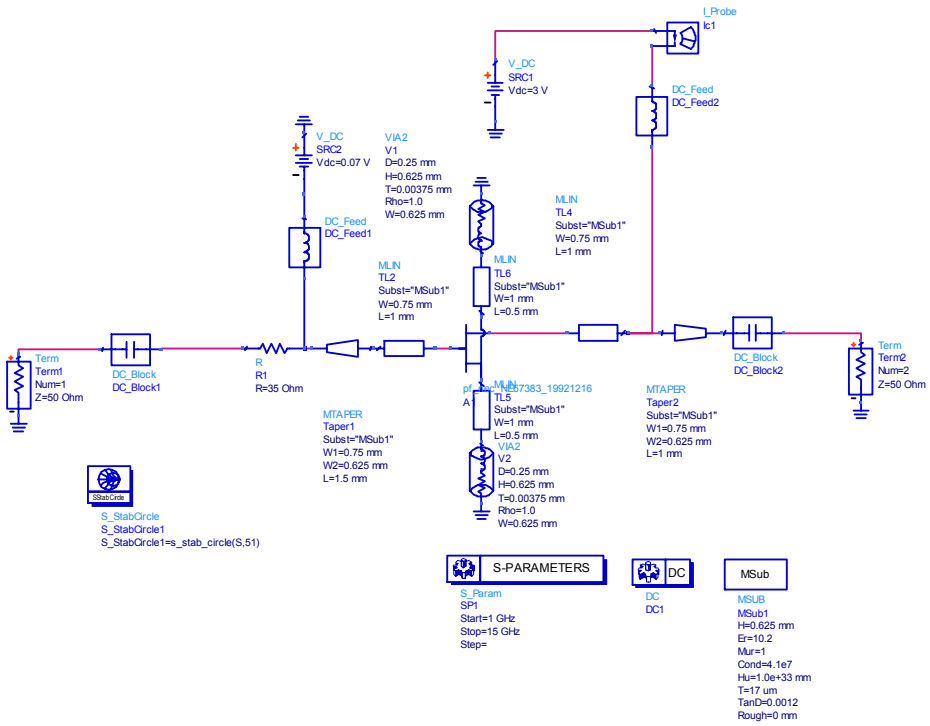


Figure 6 Showing the ADS circuit schematic with solder pads and via holes added to the FET. Also added are tapers from the gate/drain 0.75mm wide track to the 50-ohm 0.625mm track.

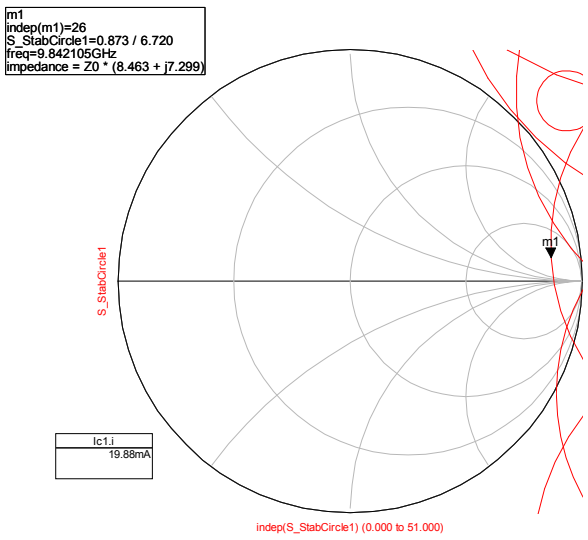


Figure 7 Showing the resulting input stability circles. The plot shows some potentially unstable regions at ~ 10GHz. However, a very high impedance would have to be applied in order to cause the possibility of oscillation.

As shown in figure 7 there is still some potential instability with an applied high impedance at around 10GHz. However the resulting matching circuit will have some loss at this frequency so the impedance at this frequency will always be lower. If when the circuit is re-simulated with RF bias networks and matching applied, there are some additional stabilising techniques that can be used.

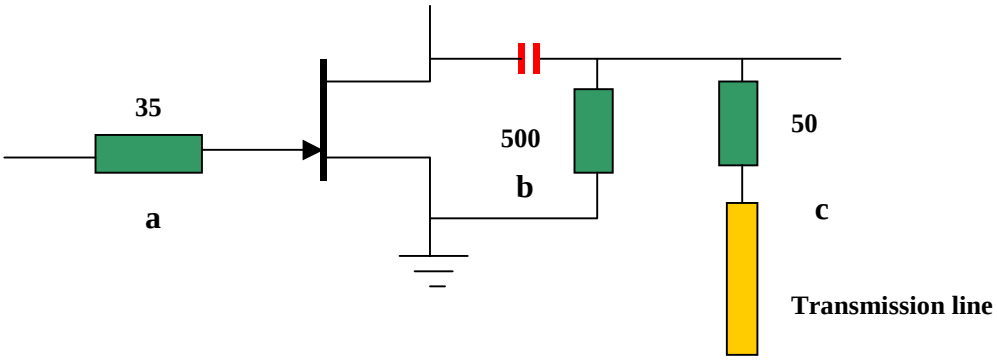


Figure 7 Stabilization techniques

Figure 7 shows several methods of stabilization (a) is the addition of a series resistor to ensure that no match is capable of intersecting an input stability circle to tend to clip the outer edge of the Smith chart. That is why some devices especially FET's readily oscillate when an open or short circuit is applied to the input of the device.
A note of caution however is that the addition of a resistor will greatly increase the noise figure of the device as the resistor acts as a noise generator.

The second method (b) involves adding a fairly high value shunt resistor across the output of the device. The DC block ensures that the DC bias to the drain/collector is not upset.

The third method (c) involves the use of a quarter wavelength piece of transmission line connected to a resistor usually 50 ohms. At the resonant frequency the quarter wavelength transmission line being an open circuit at one end will be transformed to a short circuit at the resistor end. Therefore, at the resonant frequency the resistor will be effectively shorted to ground ensuring a 50ohm load to the device. This method is generally required for high frequency problems with devices having very high Ft's.

Additionally 50-ohm resistors can be added to the bias networks to ensure that a 50-ohm resistor is connected at low frequencies where the gain of the device is at it's highest.