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Fast Time-Domain Simulation of 200+ Port S-Parameter Package Models

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Abstract

S-Parameters are quickly becoming the standard method in PCB SI analysis to describe packages, channels, and connectors. This paper will describe techniques for significantly improving the generation and transient simulation of typical s-parameter models and large (200+ port) s-parameter package models used for power distribution and simultaneous switching noise analysis. We show that direct representation of s-parameters by poles/residues is more efficient than creating equivalent circuits or performing direct convolution.

This paper will also describe why it is important to simulate channels in transient analysis, the caveats of alternate frequency-domain channel analysis techniques, and how AMS models and these new transient s-parameter simulation techniques makes it feasible to perform transient simulation of hundreds of thousands of data cycles.

Author(s) Biography

Vadim Heyfitch is an MTS engineer with the Altera High-Speed IO Applications Group in San Jose, CA. Lately he has been working on modeling SSN in FPGA packages. Vadim has worked in the field of signal integrity - both as an employee and as a consultant - at system, board and package level at Intel, Cadence, MEMS, and telecom startups. He has a M.S. in Physics from MIPT (Moscow Institute of Physics and Technology), Russia, and has done some post-graduate work at Michigan State University and the University of Washington.

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Gary Pratt is the manager of high speed partnerships for Mentor Graphics Corp.'s System Design division. He is a graduate of the University of Wisconsin at Madison, a member of IEEE, and a licensed professional engineer with 23 years experience in power electronics; control systems; digital image and signal processing; analog, digital and software design; and engineering management. Gary has been an evangelist for emerging EDA technologies throughout his career.

Sherri Azgomi is a Senior Applications Engineer at Altera Corporation, and has been with the company for the last nine years. She has specialized in signal integrity and has written numerous white papers, application notes, and other literature on design features of FPGAs. She has a BSEE from San Jose State University.

Introduction

At operational frequencies now reaching several GHz, the conventional lumped circuit component models become inadequate. By developing new high-speed models such as W-element (coupled transmission line) we can solve a number of relatively simple problems with special geometry, such as a set of parallel traces along ideal ground plane. However, any realistic design would contain a variety of more complicated geometrical constructions whose detailed description is available only with electrodynamics' methods (ED). Still, pure ED models are quite expensive and so developers have to combine them with traditional circuit components.

A natural bridge between ED and the circuit world is a frequency-domain description (Y, Z and S-parameters) of multi-port blocks. Normally, frequency-domain data has a form of touchstone files or other formats generated from ED simulation or measurement. Recently, S-parameters became a new type of library primitive which modern simulators need to support for PCB SI applications. Due to its distributed-parameter nature, size and complexity, S-parameters present many challenges. These include simulation accuracy, stability, causality and performance, as well as the ability to simulate IC packages and connectors with hundreds of ports.

A number of techniques were developed over time dealing with convolution, rational approximation, enforcing model passivity & causality and generating equivalent circuits. Interested reader can find hundreds of related publications. However, none of the existing implementations seems perfect; each one has its own bias and makes compromises between accuracy and performance. Let us briefly consider them in more details.

Direct Convolution and Pole-Residue Approximation Methods

As the original model description exists in frequency domain, we need to use some form of a convolution integral

$$y(t) = \int_0^{t_n} a(t-\tau)\frac{dx}{d\tau}d\tau = \int_0^{t_n} \beta(t-\tau)x(\tau)d\tau \qquad (1)$$

to compute time-domain (transient) solution. Here, *x(t)* and *y(t)* are respectively the input and response of the linear block, while *a(t)* and *β(t)* are unit step and unit pulse test response of the block. Mathematically, the existing methods can be grouped by the way they compute convolution in (1).

In the first group, they find system step or pulse response numerically by inverse fast Fourier transform and then use *direct convolution* to compute (1) as a discrete sum. This method is implemented in a number of simulators, including HSPICE, ELDO (with DSP method), Apache Spice and others. This approach is straightforward however it suffers from the following:

Increasingly slow computations - Model evaluation time grows as the simulation progress. Each time we estimate (1), we integrate from time zero to the current moment. Since the step/pulse response is a sampled dependence, there is no way to reuse the

portion of the integral/sum computed at the previous step. Because of above, they truncate the step/pulse response in order to limit the number of summations. However, such truncation changes the property of the model that results in loss of accuracy or even instability if passivity is violated.

Limited dynamic range - Since the inverse Fourier transform can only accept equally distant points and the number of sampling points cannot exceed a few thousands, the effective frequency range of the model cannot be made wider than approximately 3 decades. Normally, the model has poorer accuracy at low frequencies, where the number of samples per decade is the smallest; therefore much of inaccuracy appears near the steady state.

Sampled step/pulse response has its own time granularity independent on step selection mechanism used by the simulator. In presence of nonlinear devices, such as transistors, simulators may greatly reduce the step. The lumped models can naturally adjust to the smaller step and produce the correct behavior. However, S-parameter models have a fixed granularity of the step/pulse response determined at the model initialization step (see Fig. 3 below). This may result in discontinuity and cause the step selection mechanism to fail.

Possible non-causality of the solution - If for some reason the sampled frequency data does not satisfy causality conditions (e.g., Kramers-Kronig relations), its Dirac pulse or unit step response, computed by the inverse Fourier transform, may start at negative time, that is, prior to the input causing this response. Practically, they always remove this forgoing portion of the test response so it does not appear in the convolution integral. However, such simple elimination of unwanted portion creates imbalance between the responses in frequency and time domain. In simpler words, the model we finally get in time domain is not the same as the original dependence. Sometimes this appears as mismatch between AC and transient analysis.

Excessive memory is needed to store all the step/pulse responses of the large size model. With N ports, we need to store NxN (or $Nx(N+1)/2$ if symmetric) sampled dependences, each one consisting of thousands of points. But this is not all: during simulation, we also need to store the past history $x(t)$ that has to be integrated over and over.

The methods from the second group are approximate because of the sampled dependence by rational polynomials, which can also be represented as a sum of simple components defined by their respective pole and residue. Such approximation helps leverage efficient simulation in a number of ways. First, rational polynomial approximation is strictly causal therefore we obtain an exact match between time- and frequency domain models. Next, since pulse and step response of each pole/residue pair is an exponential function - possibly with complex argument - the resulting pulse/step responses in (1) can now be expressed as sums of exponential functions, too. Hence, it becomes possible to re-evaluate the current value of the integral sum based on the value it had at the previous point (so-called recursive convolution). Time-consuming integration of past history can be replaced by fast and compact update of state variables that makes the overall algorithm

linear in complexity. The other advantages include time-continuous model with no time granulation, unlimited dynamic range (6-8 and more decades of frequency range), and no need in response truncation.

Although mathematically equivalent, there exists conceptually different and more popular way of exploiting the same type of rational polynomial approximation, where each pole-residue pair is represented by the element of the lumped circuit. The advantage of this approach is evident: the sampled frequency dependence is replaced by the portable Spice-compatible sub-circuit that can be used directly without adding any special primitive or making any modifications to the simulator code. Due to that reason, there were almost no efforts made to adopt the pole/residue approximation directly in circuit simulators, in contrast to simply using the equivalent circuits. However, with increasing size and complexity of the distributed models, several limitations of equivalent circuit models become evident. The performance of the simulator is greatly affected by the following.

With thousands of additional elements and hundreds of internal nodes, the equivalent circuits inflate the list of elements and the size of the Jacobian matrix thus increase the time spent on model evaluation and solution stage. Parsing of subcircuits takes up to several hours. It makes repeated simulation of the design impractical. Less known but quite important is the effect of losing the accuracy if instead of 'analytically accurate' recursive convolution we perform numerical integration of differential equations (which describing the circuit elements). The recursive convolution is known to be 'error free' provided that the input applied to the model is a piecewise linear function and we do not miss the corner points during computations. Whereas with differential equations, we always have nonzero LTE (local truncation error), even if the input is piecewise linear. In case of long simulation run (e.g., when building eye-diagrams) LTE may accumulate and produce considerable simulation error.

It would be improper to say that no tools were developed so far which use pole/residue pairs during transient simulation. For example, rational approximation of line admittance and propagation function is a part of the lossy transmission line modeling algorithm [1, 2]. This approach is also implemented in electromagnetic solvers and some other technical applications. However, among widely known circuit simulators, we had no examples of using poles/residues as a substitute for the Touchstone files or synthesized equivalent circuits when dealing with S (Y or Z) parameters.

S-Parameter Simulation Technology Based on Direct Use of Poles/Residues

To avoid limitations associated with direct computation of the convolution sum or using large equivalent circuits, in ELDO/ADMS we developed a new type of the S-parameter model primitive that may work with tables of poles/residues directly. The program includes rational polynomial fitting and passivity enforcement capability, supplied with number of parameters allowing sufficient flexibility. The original data is provided in Touchstone format. When the model is instantiated for the first time, the program generates the table of poles/residues and saves it into the PLS file. In the next, the simulator works with this table only; the Touchstone file is no longer needed. The one-

time fitting step penalty is the same or even smaller than that needed to generate the equivalent circuit. Reading the table from the PLS file is very fast as it does not require parsing. The size of this file is many times smaller than the Touchstone it was built from, and considerably smaller than the equivalent circuit built from the same poles/residues. Hereafter, we'll call this method CPF (complex-pole fitting) for convenience and brevity.

Model Stamp

To incorporate a new circuit primitive, we need to develop a stamp that would be used in different types of analyses. Although S-parameters can be transformed into more frequently used *Y* or *Z* types, we prefer to work in the original basis to avoid model singularity.

For simplicity, let us consider linear time-invariant *N*-port object (network) with its reference node grounded, as in Fig.1a (only two ports are shown). We assume that the S-parameters of the original network (ON) are described by the sampled – Touchstone – data.

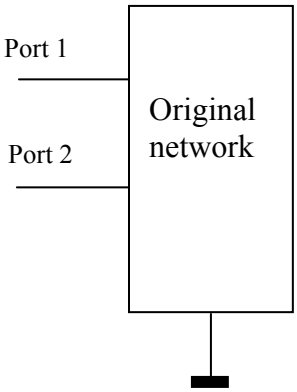


Fig. 1a

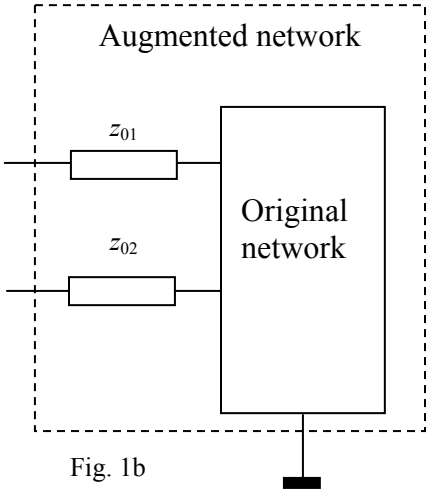


Fig. 1b

For characteristic impedance of ports, defined in the Touchstone file, and the original network, we can construct the so-called augmented network (AN), as shown in Fig.1b. Note that the characteristic impedance may be different. Inversely, the original network can be defined from AN by means of the structure shown in Fig.1c.

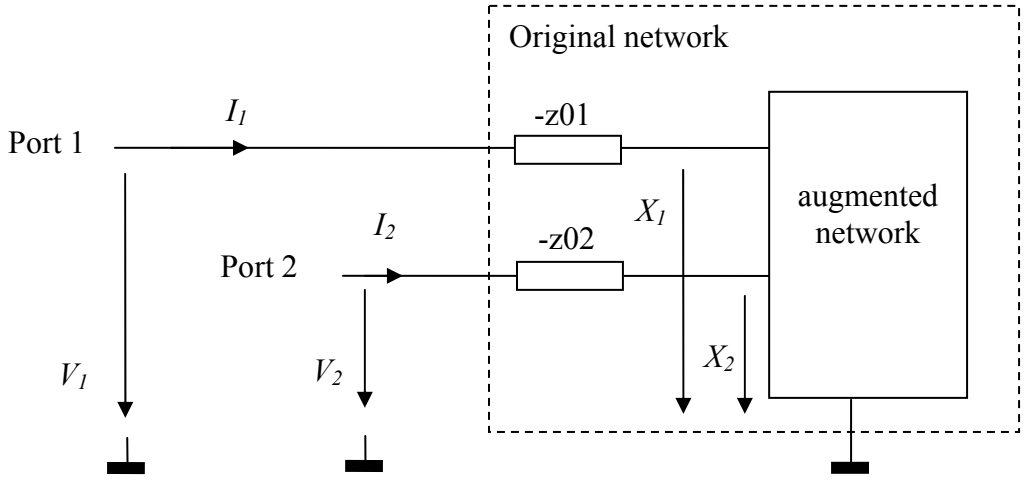


Fig. 1c. Original and augmented network

Note that in Fig. 1c we place negative resistances to compensate for extra resistance contained in the AN.

From Fig. 1c, we can directly form the matrix equation:

$$\begin{bmatrix} I \\ 0 \end{bmatrix} = \begin{bmatrix} -Z_0^{-1} & Z_0^{-1} \\ Z_0^{-1} & -Z_0^{-1} + Y_{AN} \end{bmatrix} \begin{bmatrix} V \\ X \end{bmatrix} \tag{2}$$

Here, vectors $\boldsymbol{I}$, $\boldsymbol{V}$, $\boldsymbol{X}$ combine the scalar values of port currents, external voltages, and internal voltages measured at AN ports, respectively. Same way, the diagonal matrix $\boldsymbol{Z}_0$ combines port impedance values defined for our S-parameters.

Now, we express the conductance of the augmented multi-port, $\boldsymbol{Y}_{AN}$, via S-parameters. In [3, (9.88) and (9.89)] we find the relation between properly normalized scattering matrix and the normalized (dimensionless) admittance of the augmented network:

$$S = U - 2Y_{NAN}, \tag{3}$$

where U is a unit matrix and

$$Y_{NAN} = Z_0^{1/2} Y_{AN} Z_0^{1/2}. \tag{4}$$

Combining relations (3), (4), we get

$$Y_{AN} = \frac{1}{2} Z_0^{-1/2} (U - S) Z_0^{-1/2}. \tag{5}$$

Equation (5) can be modified as

$$Y_{AN} = \frac{1}{2} Z_0^{-1} + H(s), \text{ where } H(s) = -\frac{1}{2} Z_0^{-1/2} S Z_0^{-1/2}. \quad (6)$$

The first summand in (6) is a diagonal matrix that can be thought as a conductance between nodes *X* and the ground. The square matrix *H(s)* is the conductance of a dynamic *N*-port, connected to same nodes. Let I_H be a vector describing the current flowing into this dynamic *N*-port. The matrix equation (2) together with (6) serves as a model stamp. However, in time domain, the current of the dynamic *N*-port cannot be expressed simply as a product of *H* and *X*. We assume that the dependence *H(s)* has been fitted [4-6] and thus represented as the sum

$$H(s) = H_\infty + \sum_{m=1}^{M} \frac{1}{2} \left[\frac{A_{1m} - jA_{2m}}{1 + s/(\alpha_m + jw_m)} + \frac{A_{1m} + jA_{2m}}{1 + s/(\alpha_m - jw_m)} \right]. \quad (7)$$

Here, for every pair of complex-conjugate poles we use frequency-sized parameters α_m, w_m ($\alpha_m > 0$) and coefficients A_{1m}, A_{2m}, all real. The above expression also works for real poles. If the *m*-th root is real ($w_m = 0$) then the denominators equal and the second coefficient A_{2m} negates.

With (7), the current of the dynamic *N*-port may be computed via recursive convolution formulated in the matrix form:

$$I_H(t_n) = [H_0 - \sum_{m=1}^{M} \mathrm{Re}\, \dot{D}_m(h)] X(t_n) - \sum_{m=1}^{M} \mathrm{Re}\, \dot{z}_m(t_n) \quad (8)$$

$$\dot{z}_m(t_n) = e^{-\dot{\Omega}_m h} \dot{z}_m(t_{n-1}) + (e^{-\dot{\Omega}_m h} - 1) \dot{D}_m(h) X_{n-1}, \quad (9)$$

where $$\dot{D}_m(h) = \frac{\dot{A}_m}{\dot{\Omega}_m h} (1 - e^{-\dot{\Omega}_m h}). \quad (10)$$

For simplicity, we reduced (8)-(10) to the case of fixed time step. Expression (8) contains the entries needed to complete the stamp (2), both the matrix and the right hand vector that is the sum of the vector state variables.

Additional features we support include delay extraction so that the *H(s)* is represented as a sum (7) multiplied by the delay operator. This operation may considerably reduce the number of pole/residue pairs needed for some matrix components. Another considerable advantage of using pole-residue form over equivalent circuit is the ability to perform asymptotic pole reduction to further accelerate time domain analysis. The idea behind the method is that in any actual transient computation the ratio of simulation window to simulation resolution is typically 10^3-10^4, while the poles' radii may differ in 5-6 orders. Hence, for a given simulation window & resolution we can detect poles responsible for "too fast" or "too slow" movements and asymptotically remove them. Note that reduction should be performed only on pre-analysis stage. It cannot be done while originally generating poles & residues, or equivalent circuit, for we do not know the actual simulation conditions yet.

Four Port Example Model

Let's first take relatively simple model: coupled 2-conductors on FR4. It is described by the 5000 data points equally sampled from zero to 50GHz. The built-in ELDO component-based fitting of this model and passivity enforcement takes 4.5 min. This time mainly depends on the complexity of given data. The number of complex poles required to approximate different matrix components varies from 23 to 68. The least square error does not exceed 0.3%. The results of fitting are stored in the fr4data.pls file that is only of 77KB size (compare to 2.33MB of the original touchstone). Actually, we do not need the touchstone file anymore since ELDO CPF can perform simulation by taking all necessary data from the fr4data.pls. Together with the fitted table, we output the Spice-compatible equivalent circuit, built from same poles/residues.

In Fig. 2 below we can see the sampled and fitted dependence describing matrix component S11. The legends are: solid red – original dependence, real part; solid blue - original, imaginary part; dashed green – fitted, real part; dashed cyan – fitted, imaginary part.

Then, we performed a series of simulations with the touchstone, fitted poles/residues and with the equivalent circuit. In all cases, we load our 4-port model with 100Ohm resistors and apply 1V step voltage to the port 1. The simulation interval was set to 50ns; the step size was not allowed to exceed 1ps, both in ELDO and in the Base Simulator (BASESIM). Transient analysis times are: ELDO CPF – 2.3 sec, ELDO w/convolution 122 sec, BASESIM w/convolution 183 sec, BASESIM w/equivalent circuit – 151 sec.

The waveforms (voltage at port 3) are shown in Fig. 3. Since we do not filter out high frequency components, the waveform we observe is what actually comes out of the S-parameter model. Both convolution-based methods exhibit internal time granularity that corresponds to the upper frequency of 50GHz. We immediately notice the stepwise waveform generated by ELDO pulse-response-based convolution approach. The BASESIM (green) probably exploits the step-response version of the convolution integral, therefore it looks very much piecewise linear. If we connect the middle points of the edges on the red curve, the sections will form something very close to the green (BASESIM) solution. However, because of the finite time granularity, both convolution waveforms do not look realistic.

In Fig. 4, we add extra solutions computed with the S-model replaced by the synthesized equivalent circuit (EC). First, note that the CPF and EC curves almost coincide if the solution step is 1ps or below (blue and magenta). However, with increasing step tolerance (delmax=5ps), the EC curve (magenta) acquires considerable amplitude/phase distortions, due to its inherent LTE stemming from approximation of derivatives by finite differences, whereas the CPF (fixed 5ps step, black) keeps the computed points mostly at previous positions.

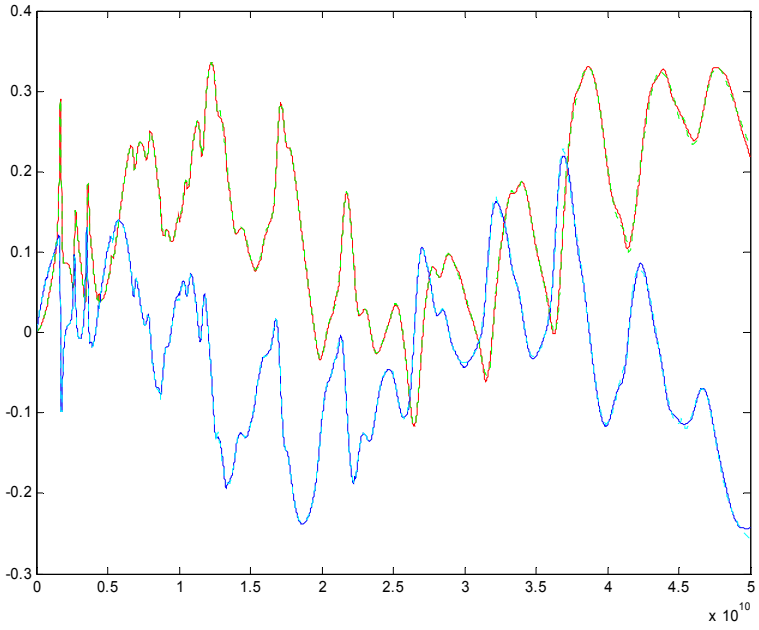


Fig. 2. Fitted and original dependence for S11.

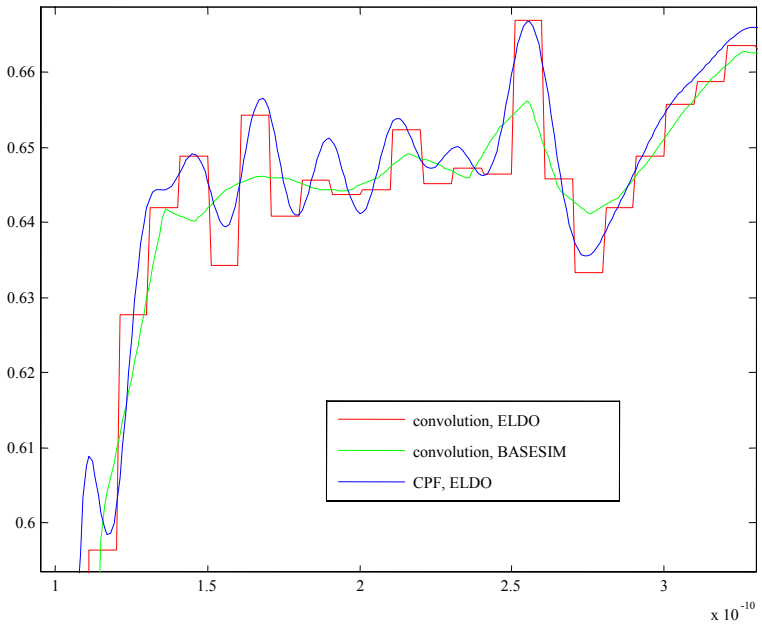


Fig. 3. Waveforms computed with CPF and direct convolution methods (zoomed to demonstrate the effect of time granularity).

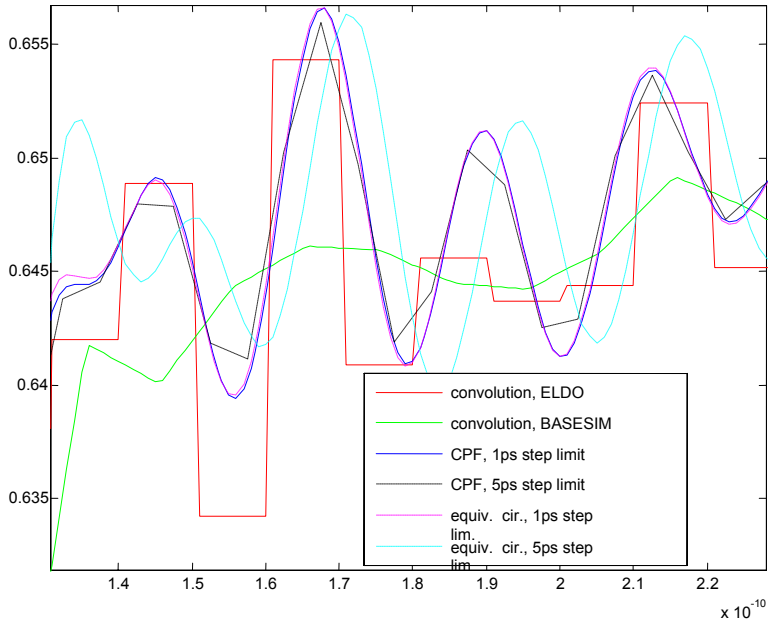


Fig. 4. Waveforms computed with CPF, direct convolution and equivalent circuit

S-Model as a Substitute for the Lumped RLC Model

So far, we considered the S-parameter simulation issues. We found that direct simulation with poles/residues outperforms the equivalent circuits. It is faster because the large number of internal nodes and circuit elements are excluded from consideration. It is more accurate because poles/residues empower analytical LTE-free evaluation. Logically, the next question is this. Suppose we have to simulate a design that includes large linear circuit described by RLC components and transmission lines. Can we benefit from replacing this linear portion of the design by the S-model described with poles/residues? Surprisingly, the answer is yes, provided that the fitting can be made sufficiently accurate and the number of external ports is much smaller than the size of the linear circuitry.

Let us take a customer design with the differential channel containing packages or/and connectors. The linear model contains several nested sub-circuits that total to 208 internal nodes and 611 linear components. By the AC analysis, we extract the 4-port S-parameters of the channel. To maintain accuracy, ELDO may select frequency step size adaptively, to follow the curvature of the dependence. Although irregular stepping is useless for convolution-based methods, it is valuable for the complex-pole fitting. The touchstone file is of 2.5MB size; it is then fitted into PLS file of only 130KB.

To estimate how much the model contributes into the total evaluation and solution time we loaded it with constant resistors and applied a pulse voltage. With approximately 40,000 transient steps, the fitted S-parameter model is solved in 2.1 second. The original non-compressed RLC model takes 92 second for the same number of steps.

Then, we estimated the error produced by different models relative to the fitted model solved with 1ps step, taken as a reference. As we see from Fig.5 below, the solutions with RLC models computed with 10, 5, 2 and 1ps step converge to the CPF solution (cyan, green, red, black respectively). We also plotted the error for the CPF solutions computed with 10ps step (blue). It is about the same as of the 5ps RLC solution.

As we mentioned earlier, CPF method does not produce LTE error, as RLC model does. It would give us no error if the voltages at the model ports were piecewise linear. However, this is not the case due to exponential nature of solution. Therefore, the accuracy of CPF solution also depends on the step size although the error is much smaller than if LTE were present.

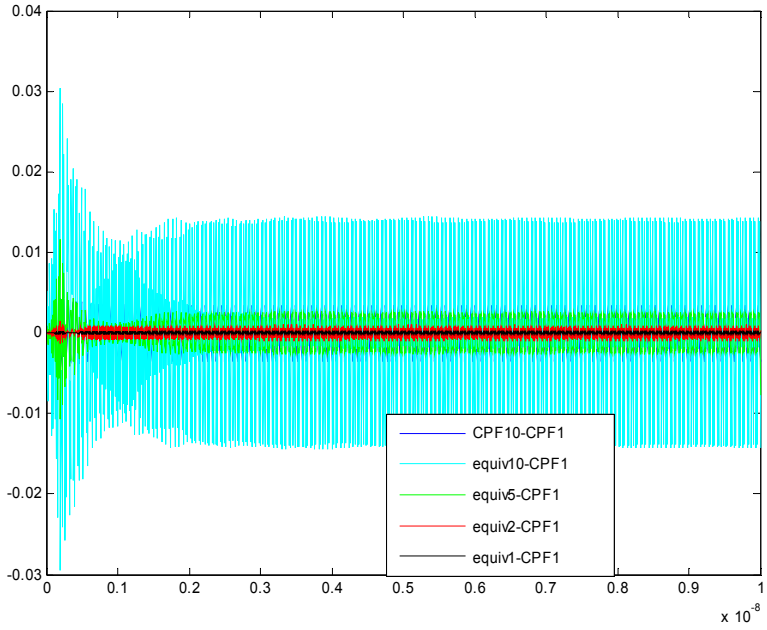


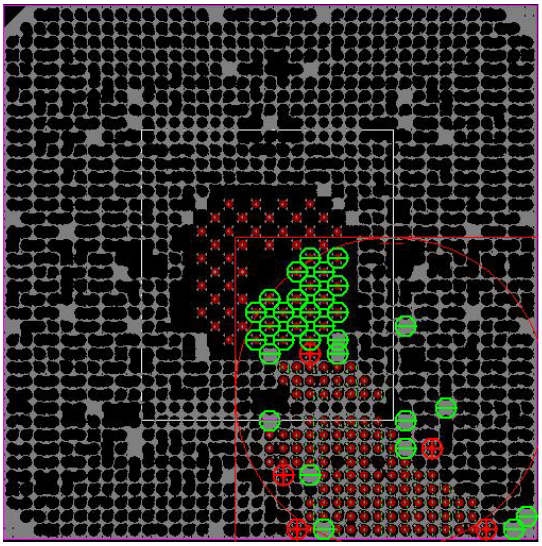
Fig. 5. Convergence of RLC solutions to CPF.

226-port S-Parameter Model Example

The compactness and efficacy of the pole/residue representation extend the size of amenable S-parameter model. An example of using the large S-parameter model is a single bank of 2S130F1508 Altera® FPGA.

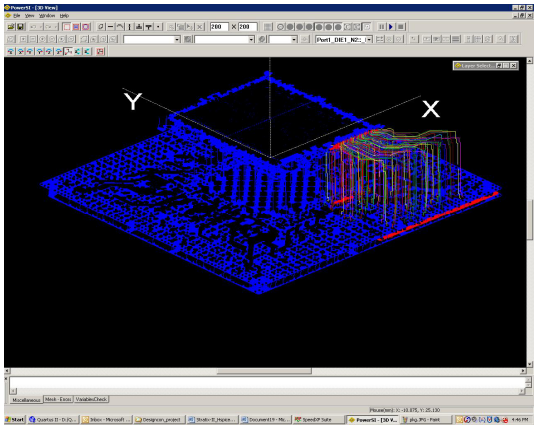
Generally, creating an adequate package model for SSN (Simultaneously Switching Noise) simulations is much simpler for ASIC chips than for FPGA devices. In ASICs designers usually use a periodic pattern of ground and power pins that is repeated in both x- and y- directions. The common practice for SSN modeling of ASIC package is to extract such 'elementary' cell, or cluster, of IO pins all the way from the bump side to the ball side of the BGA package. A typical case would be a group of 12 BGA balls – a rectangular cluster 3 by 4 pins – where every other ball is either a ground or a power. Most typically, one would break these 12 copper nets into segments and extract each segment using quasi-static 2D or 3D solvers. Such approach, of course, neglects couplings between the adjacent pin clusters. It has other shortcomings as well, critiquing

which falls outside the scope of this paper. Apart from known and, possibly, unknown flaws of this approach, it simply cannot be easily used for FPGA packages. The latter have rather few ground and power pins (or, balls) unevenly distributed throughout each bank. The picture below shows distribution of ground pins in Bank 8.



Ground and Power pin distribution.

Therefore, one has to somehow extract the entire FPGA package bank to have an accurate SSN model. In F1508 package there are more than 100 signals per bank. Each signal opens up as a bump to the die and a ball to the board. The resulting S-parameter package model has more than 200 ports. It is a fully coupled model that apriori does not neglect any couplings. The complexity of the problem can be better appreciated from looking at the 3D picture of the 'open' package.



3D view of the F1508 package.

The data was extracted using Sigrity's PowerSI from 100 Hz to 100MHz with logarithmic and then constant 10MHz steps up to 4GHz. The touchstone file contains total 425 points, and sizes to 772MB. We performed fitting and passivity enforcement with a stand-alone tool, thus produced the PLS and equivalent circuit files. Just reading the touchstone file takes 12 min of ELDO time. Fitting takes 4.1 min and passivity

enforcement 14 minutes. The size of the pole/residue and equivalent circuit files are 44MB and 54MB respectively.

To compare different S-parameter simulation techniques, we isolated the model, loaded it with resistors to ground and performed transient analysis up to 1ns with 1001 computed points. All attempts with direct convolution methods, both in ELDO and BASESIM, were unsuccessful. The only completed are CPF and equivalent circuit solutions, which give an excellent agreement (see Fig.6). Table 1 contains the statistics that speaks for itself. Here, For CPF method, we did not include fitting and passivity enforcement time mentioned earlier, as it is a one-time penalty. However, the huge equivalent circuit parsing/error check time is an each time penalty therefore it is included.

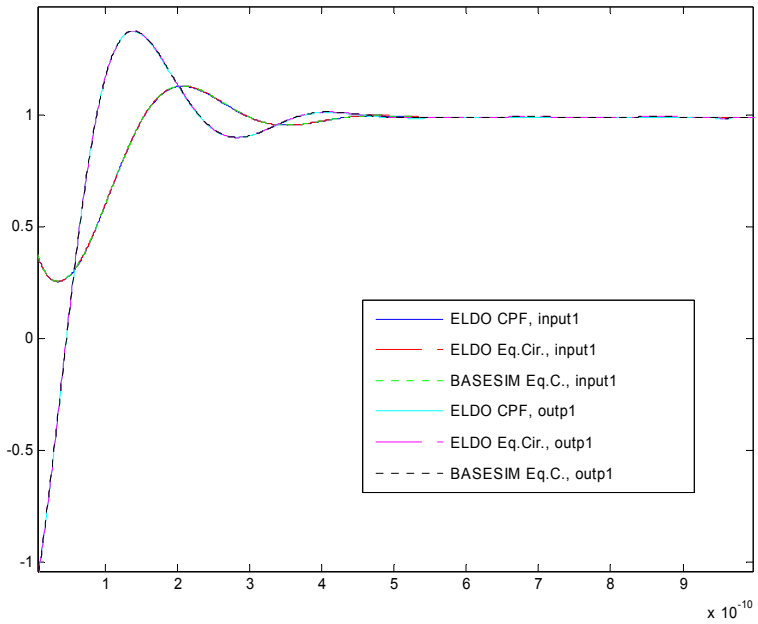


Fig. 6. Solutions by ELDO CPF, ELDO + equivalent circuit, and BASESIM + equivalent circuit.

Table 1. Statistics indicating the advantage of the CPF approach.

	ELDO CPF (with PLS file)	ELDO, equivalent circuit	BASESIM, equivalent circuit
Read/parse/err check	14 sec	38 min 05 sec	11 h 48 min
DC solve	6.8 sec	3 min 55 sec	4 sec
Transient	7 min 22 sec	46 min 09 sec	20 min 11 sec
Total	7 min 43 sec	1 h 28 min 10 sec	12 h 08 min 36 sec

IC Model Compression Technique

IC Model Compression Technique

We proposed the use of the pole/residue based S-model as a substitute of the lumped RLC model that can be thought as linear model compression. However, to make simulation of a real design feasible, we need to consider the device model compression as well.

Traditional IBIS

Perhaps the best known form of IC device model compression is the IBIS table model. While reasonably popular, this modeling approach has one major drawback. Being a template type model, the template parameters need to be continually enhanced to accommodate new aspects of each new technology. Unfortunately, the length of time required to propose, ratify, and adopt these new enhancements is usually not compatible with the market demand for SI models of the new technology.

Transistor-level SPICE

For this reason, often the only alternative IC vendors and PCB designers had for new technologies was to resort to encrypted SPICE models. But SPICE has its own well-known set of drawbacks. Encrypted transistor-level SPICE is non-portable (each Spice vendor has its own encryption technique), slow (since the transistor-level design contains much more detail than is necessary for SI analysis), complex (requires PCB designers to understand difficult Spice syntax), and non-public (as there is no single Spice standard).

IBIS 4.1 IEEE 1076.1 and Accellera AMS

Fortunately, the IBIS committee (http://www.eigroup.org/IBIS/Default.htm) recognized the time delay drawback to traditional IBIS, and that it was becoming difficult to accommodate the complexities of newer technologies in a template model. As a result, in 2003 the IBIS committee ratified a new approach which will accommodate current technologies, as well as the technologies of the future. Rather than fixed templates, this new technique is based on the IEEE 1076.1 and Accellera standard analog and mixed-signal (AMS) behavioral modeling languages. With the power of an actual modeling language, modeling engineers can easily add any new feature that is required to accommodate the complexities of new technologies. It is no longer necessary to propose and champion a change to the IBIS standard, wait for ratification, and then wait again for EDA vendors to incorporate the change and model builders to utilize the change. The AMS language capability is somewhat like having a simulator programmer (with the simulator source-code) on staff. If your technology requires a new feature, just write the new feature into the model.

With its unparalleled flexibility, perhaps the greatest uses of AMS are those we have yet to imagine. History continually shows when creative engineers are given the freedom to innovate, novel solutions to difficult problems are the result. In fact, we are seeing clear signs of this with creative AMS applications including automated eye jitter and amplitude

measurement, fast DFE implementation, fast CDR modeling, slew-dependant timing modeling, and complete interface functional SI testing. And, this is just the beginning.

Of course, flexibility is not the only benefit to AMS. With the ability to abstract away transistor-level complexity and partition sections of the design to the digital domain, simulations run hundreds of time faster, sensitive IP is protected, and convergence problems become nearly non-existent. Likewise, since IEEE 1076.1 AMS is a public standard, a model written in AMS will be compatible with any IBIS 4.1 IEEE AMS compliant simulator. The industry will no longer be locked into one convergence-error-prone proprietary transistor-level simulator. Figure 7 shows the typical results of an encrypted transistor-level simulation versus an equivalent AMS model simulation. As shown, the simulation is over 200 times faster, and produces virtually identical results.

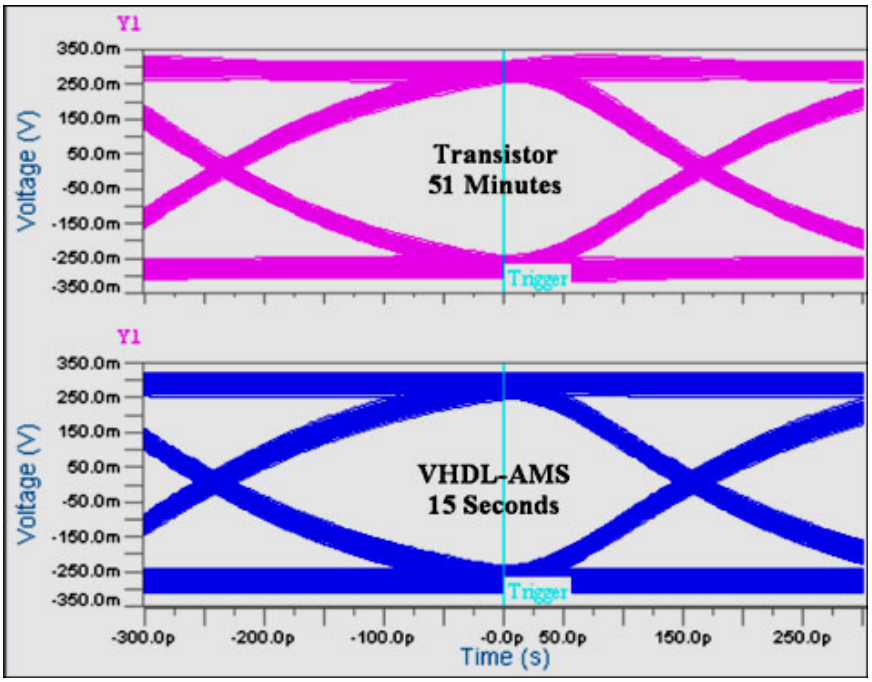


Fig. 7. Eye diagrams built with transistor-level and AMS models.

Other SI Modeling Alternatives

There are other alternatives to encrypted-spice simulation as well, but none with all the positive attributes of AMS. Statistical methods suffer from loss of non-linear information and have trouble accurately analyzing crosstalk and CDR effects. Macro modeling uses a fixed set of building-blocks so it suffers the same inflexibility as the IBIS template model approach (and its use often requires a great deal of cleverness resulting in models that are slower, cryptic and difficult to maintain). And, other lesser-known alternatives require proprietary models or are proprietary to a single silicon vendor. AMS is the clear choice for the future of SI modeling.

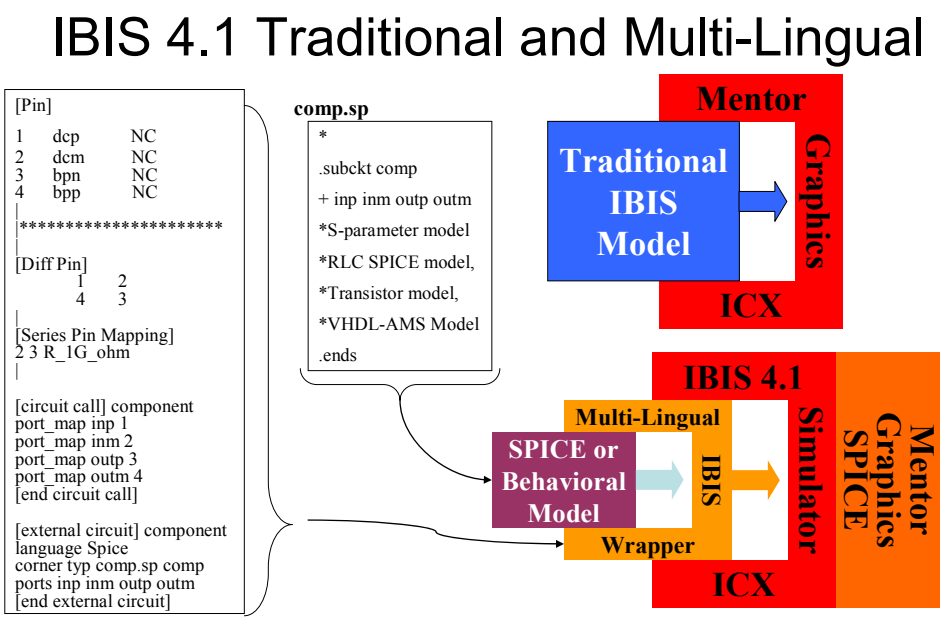


Fig. 8. Traditional IBIS versus IBIS 4.1.

Integration of AMS Using IBIS 4.1

In addition to formally supporting AMS models, IBIS has provided a mechanism for AMS and other external models to be easily used in specialized SI tools. The IBIS model provides the physical connectivity (pin numbers, differential pair mapping, etc) where the AMS model provides the detailed behavioral information (switching times, voltage levels, pre-emphasis behavior, etc). Figure 2 shows how an external model is incorporated into an IBIS simulator. In Mentor Graphic's ICX, the process is:

1) Import the IBIS 4.1 model
2) Import the layout (or place blocks for a pre-layout analysis)
3) Assign the IBIS 4.1 model to a part
4) Select the net to simulate
5) Select "probe net"
6) View the results

Combining AMS and S-Parameter Models and Integration of S-parameter Models Using IBIS 4.1

Although AMS models are very much faster than their spice counterparts, AMS models are not the whole solution. As the Figure 3 shows, an SI simulation with a complex channel can only provide simulation speed up to the point where the channel analysis begins to dominate. To see further increases in speed, it is critical that traditional channel models and channel analysis techniques be replaced with fast s-parameter models and CPF analysis as described earlier in this paper.

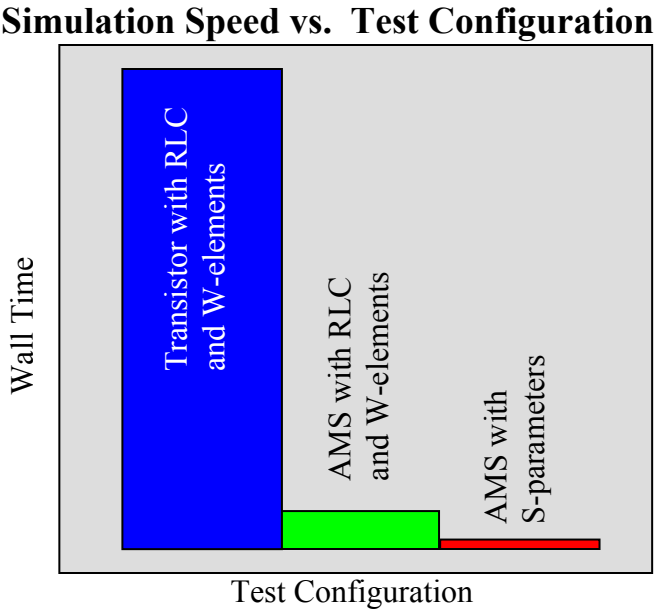


Fig. 9. Simulation Speed Improvement with AMS and S-parameter models.

S-parameter models can also accommodated with IBIS 4.1 allowing quick and easy use of s-parameters for connectors, packages, vias, or fixed channels.

Table of Poles/Residues as a New Standard for S-parameter Description

For more than two years, in some Mentor products they use a new type of files (PLS) to describe frequency-dependent matrices. This format is a convenient and condensed replacement to the Touchstone data with the difference that the touchstone format describes sampled dependence while PLS describes the dependence fitted. Many advantages of using this type of model description were shown earlier in this paper. For large models, there is simply no reasonable alternative.

Of course, to follow this standard, one has to be able to create these PLS models and use the simulator that is able to understand them. As we show, both problems can be solved in a very efficient way.

Conclusion

In this paper we considered the S-parameter simulation approach implemented in Mentor Graphics simulator ELDO/ADMS. We compared direct convolution and rational approximation based methods. Within the second group, we demonstrated the pros and contras for using equivalent circuits or the tables of poles/residues. Although equivalent circuits present the most portable solution, for large models they become very inefficient due to enormous overhead costs. As many experiments with widely different model parameters demonstrate the approach that directly makes use of poles/residues is the most advantageous. The efforts needed to create the PLS-type data file definitely pay off.

The combination of AMS, S-parameters, and IBIS 4.1 provides a fast and easy-to-use solution for PCB SI analysis now and well into the future.

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