Optimal Placement of Decoupling Capacitors on PCB Using Poynting Vectors Obtained by FDTD Method

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ABSTRACT

This paper describes the searching method for positions of decoupling capacitors on the printed circuit board (PCB). In this method, first, the distributions of electromagnetic field between power and ground planes in the time domain are simulated, using FDTD method. Next, the distribution of poynting vectors in the frequency domain is investigated, using Fast Fourier Transform (FFT). Furthermore, this method finds the optimal location of decoupling capacitor so that the poynting vector is the highest. Finally, we analize the distribution of magnetic field emission above the signal plane in the x and y axes in the specified range of frequency and verify the validity of our method.

1. INTRODUCTION

With the increasing levels of integration and the associated increase in the current demand, power delivery is becoming an important design concern. The recent technology advance into the deep submicron regime has brought the noise and signal integrity issues into the spotlight. The signal degradation comes from various sources, such as the coupled noise from adjacent signals, the reflection noise from impedance discontinuities, and the power supply noise due to switching currents. To simulate accurately these noises and the radiated emission, a three-dimensional structure of PCB model is required [1] and some numerical methods such as Partial Element Equivalent Circuit (PEEC) method and Finite Difference Time Domain (FDTD) method have been used [2], [3].

FDTD method is arguably the most popular numerical method for the solution of problems in electromagnetic field effects because this algorithm is simple and provides superior accuracy. This method is based on the direct difference method of Maxwell's equations. This method is able to analyze the electromagnetic field effects of two or three-dimensional structures [4], [7], [8].

On the other hand, in order to reduce the emission, the methods for placing decoupling capacitors between power and ground planes have been developed. However, the designer must empirically determine the positions of the decoupling capacitors to reduce radiated emission [5], [6].

This report proposes the searching method for positions of decoupling capacitors on PCB. This method finds the location of decoupling capacitors, where the value of poynting vector is the highest in the frequency domain. In the proposed method, first, the electromagnetic field effects of three dimensional PCB are calculated by using FDTD method and the distributions of electromagnetic field between power and ground planes in the time domain are obtained. Next, the distribution of poynting vectors is extracted in the frequency domain by using Fast Fourier Transform (FFT). Finally, we find the optimal positions of decoupling capacitors to reduce the radiated emission. Furthermore, we verify the validity of this method by the simulation of placement of decoupling capacitors on an example printed circuit board.

2. A METHOD FOR OPTIMAL PLACEMENT OF DECOUPLING CAPACITORS

This section describes a method for optimal location of the decoupling capacitors. We use FDTD method, which is simple and provides superior accuracy, to analyze the electromagnetic field effects of three-dimensional PCB. Decoupling capacitors are located on the lattice composed of 2-dimensional meshes of the PCB. In general, it can be said that the poynting vector represents energy flow in electromagnetic field and a decoupling capacitor has to supply the current with all the frequencies in the

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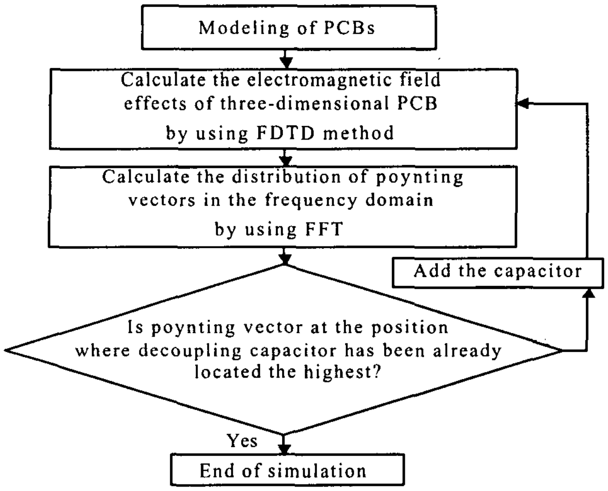

Fig. 1 An algorithm to search the positions of decoupling capacitors.

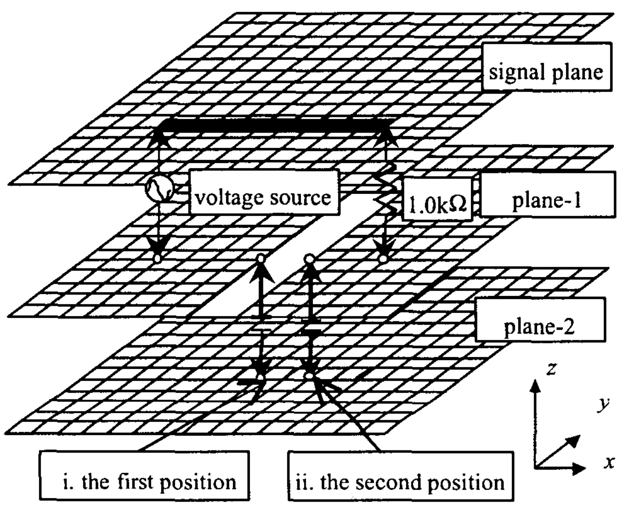

Fig. 2 The printed circuit board of Example 1.

specified range during the state transition (switching) of the logic element. Then, in this method, decoupling capacitor is located at the position where the poynting vector is the highest. Poynting vector $\boldsymbol{P} = (P_x, P_y, P_z)$ is defined by

$$\begin{aligned} \boldsymbol{P} &= \boldsymbol{E} \times \boldsymbol{H} \\ &= (E_x \boldsymbol{i} + E_y \boldsymbol{j} + E_z \boldsymbol{k}) \times (H_x \boldsymbol{i} + H_y \boldsymbol{j} + H_z \boldsymbol{k}) \\ &= (E_y H_z - E_z H_y)\, \boldsymbol{i} + (E_z H_x - E_x H_z)\, \boldsymbol{j} \\ &\quad + (E_x H_y - E_y H_x)\, \boldsymbol{k}, \end{aligned} \tag{1}$$

where $\boldsymbol{E}$ and $\boldsymbol{H}$ represent the vectors of electric and magnetic fields in the time domain between power and ground planes, which can be obtained by FDTD method, and $\boldsymbol{i}, \boldsymbol{j}$ and $\boldsymbol{k}$ represent unit vectors in the directions of x, y and z respectively. In this simulation, decoupling capacitors are located in the z axis. Then, we calculate the value of poynting vector. $P_z = (E_x H_y - E_y H_x)\, \boldsymbol{k}$ and determine the positions of decoupling capacitors. In the algorithm, first, the distribution of poynting vectors is calculated

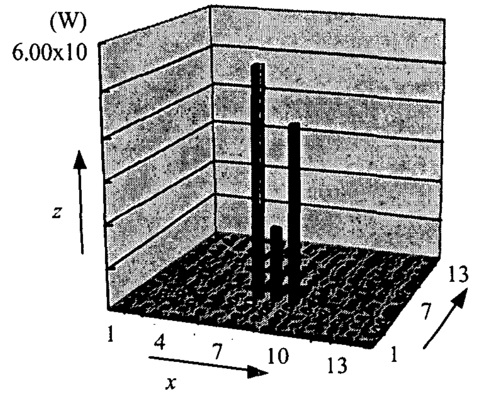

Fig. 3 The distribution of poynting vectors in the z axis (Example 1, 500MHz).

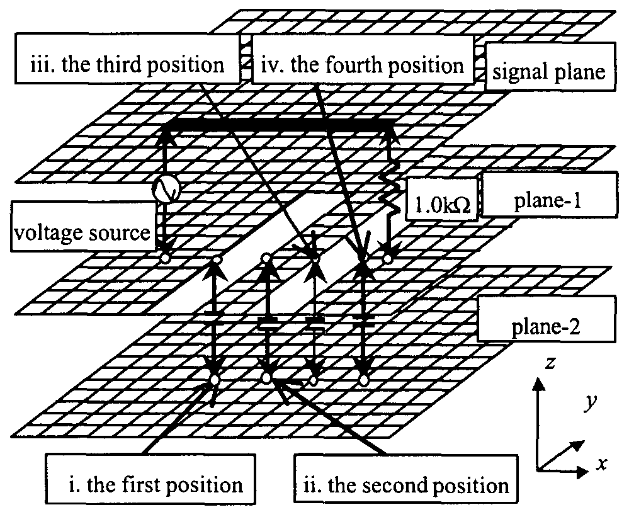

Fig. 4 The printed circuit board of Example 2.

without capacitors on the plane. Next, the decoupling capacitor is located at the position in which the value of poynting vector is the highest. This procedure is repeated until poynting vector at the position where decoupling capacitor has been already located is the highest. Poynting vectors in the specified range of the frequency are obtained by applying FFT to E_x, E_y, H_x, and H_y derived by FDTD method. The algorithm to search the optimal positions of decoupling capacitors is summaried as shown in Fig. 1.

3. NUMERICAL RESULTS

We simulated an example PCB with the FDTD method. We analyzed with the three-dimensional FDTD simulator "*After*" developed at our laboratory [6], [7]. The spatial steps used in analysis by FDTD method are $\Delta x = \Delta y = 1$mm and $\Delta z = 0.1$mm, and the total mesh dimensions are 15x15x14 in the x, y, and z axes. We have assumed that both of under and upper spaces of PCB are air whose relative permittivity is 1.0005. The material of the line is copper and electrical conductivity is 5.8×10^7 [Ω^{-1}/m]. In this

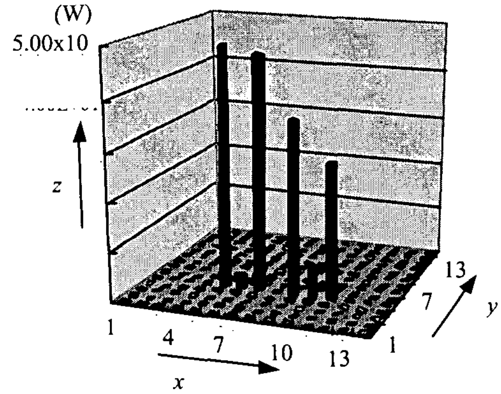

Fig. 5 The distribution of poynting vectors in the *z* axis (Example 2, 500MHz).

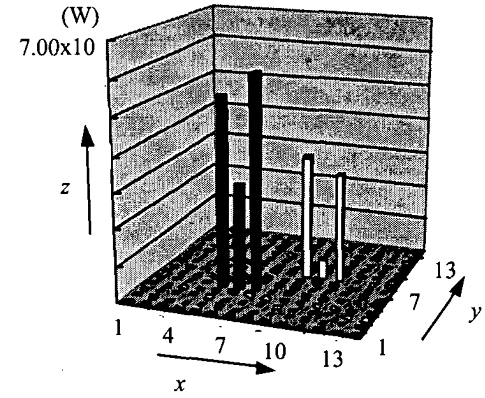

Fig. 7 The distribution of poynting vectors in the *z* axis (Example 3, 500MHz).

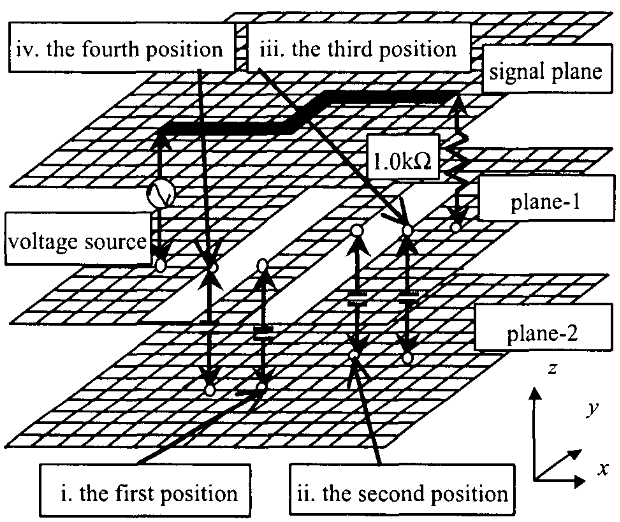

Fig. 6 The printed circuit board of Example 3.

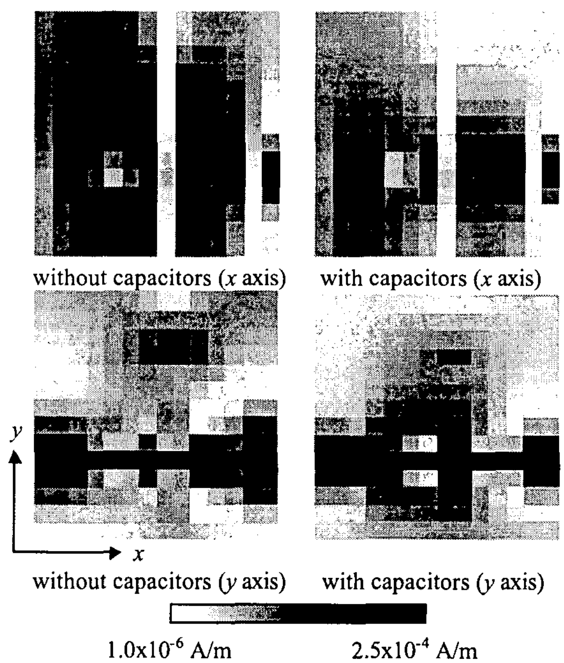

Fig. 8 The distributions of magnetic field emission (Example 1, 500MHz).

simulation, Gaussian Pulse is used as the input signal. The value of decoupling capacitors is 0.01μF.

Example 1: An example PCB is shown in Fig. 2, which is composed of three planes with a slit. Fig. 3 shows the distribution of poynting vectors on the plane-2 in the case of PCB without the decoupling capacitors, which was obtained by FDTD method and (1). The decoupling capacitors are placed at the positions where the poynting vectors are the highest and the second. The positions i and ii in Fig. 2 are the first and second positions respectively. In this simulation, we have obtained the result that optimal positions of decoupling capacitors are the ones neighboring to the slit and just below the line.

Example 2: Next, we attempted to simulate an example PCB which has two slits on the plane-1 as shown in Fig. 4. Fig. 5 shows the distribution of poynting vectors on the plane-2 in the case of PCB without the decoupling capacitors. From Fig. 5, we could obtain that the optimal positions i, ii, iii, and iv are neighboring to the slits and just below the line as similar to Example 1.

Example 3: As the third example, we simulated PCB which has two slits on the plane-1 and the different path on the signal plane as shown in Fig. 6. Fig. 7 shows the distribution of poynting vectors on the plane-2 in the case of PCB without the decoupling capacitors. From Fig. 7, we could obtain that the optimal positions i, ii, iii and iv are neighboring to the slits, just below the line and current loop is shorter than that in the case of without capacitors.

In general, if there exists the slit on the ground plane, this slit causes undesired effects to the transmission characteristics of the line and bring the noise and radiated emission. After optimal

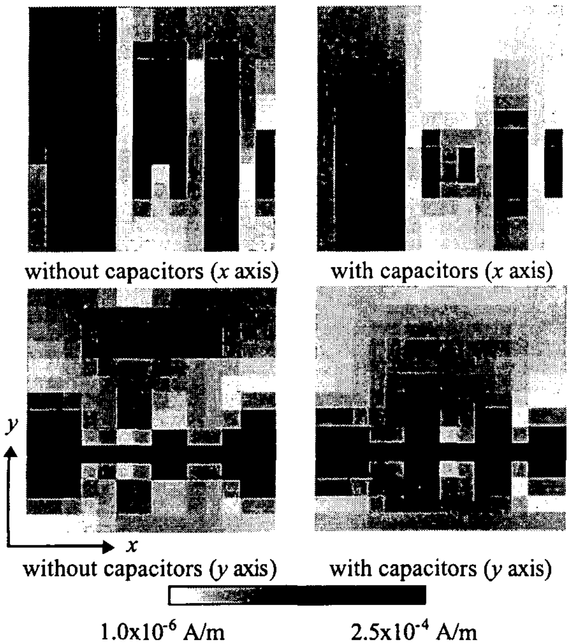

Fig. 9 The distributions of magnetic field emission (Example 2, 500MHz).

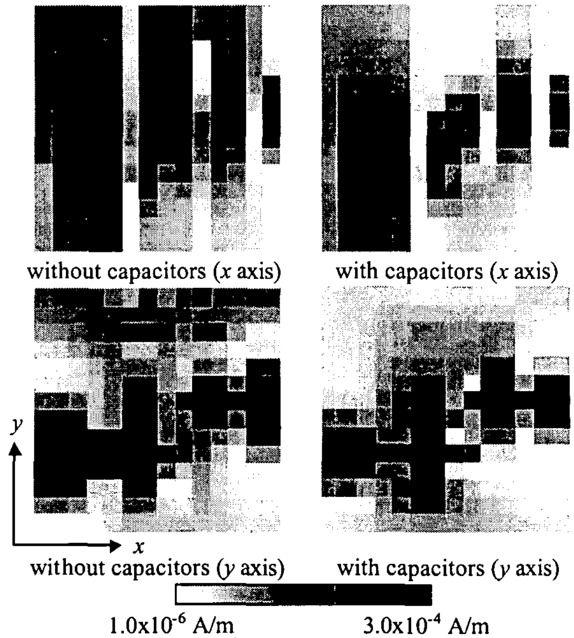

Fig. 10 The distributions of magnetic field emission (Example 3, 500MHz).

location, we have simulated the distributions of magnetic field in the cases of PCBs without and with the decoupling capacitors. Figs. 8, 9 and 10 show the distributions of magnetic field emission above the signal plane in the x and y axes at the frequency of 500MHz in the cases of examples 1, 2 and 3, respectively. From these figures, we can see that the radiated emission is inhibited in the case with the decoupling capacitors. As a result, we have confirmed that the proposed method is useful.

4. CONCLUSION

We have introduced a method which optimizes the positions of the decoupling capacitors on the PCB. This optimization method is based on the distribution of poynting vectors which is obtained by FDTD method. We could confirm the effects of the decoupling capacitors and the validity of this method. In conclusion, it is expected that our method is useful for search of the optimal positions of decoupling capacitors.

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