The Optimal Value Selection of Decoupling Capacitors Based on FDFD Combined with Optimization

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Abstract: This paper described a novel attaching decoupling method, which can promptly guide engineers to select the optimal value of decoupling capacitors to suppress low, middle and high frequency noise for board/package/system design. Analysis of 6 layers PCB indicated the methodology could efficiently and automatically guide engineers to attach how much value of decoupling capacitor on board/package/chip.

1. Introduction

Simultaneous switching noise, also called Delta-I noise or power/ground bounce, is one of the biggest concerns in designing the power supply of a high-performance system. To ensure system performance and reliability, typically, on-chip, on-module and on-board decoupling capacitors are used to suppress high, mid and low frequency noise respectively. Several authors[1] have discussed accurate modeling methods for on-chip and on-module power distribution to quantify Delta-I noise and to determine use of decoupling capacitors to control its sources. The need to control these high and mid-frequency noises is well understood and has become a major design effort for both the chip and package designers. However, in most real package/board design environment, evaluation of decoupling capacitors is still engineering estimation or use of well-established guidelines from experience. The usual reasons for this are limitation of modeling tools and mainly schedule impact caused by a detailed expensive modeling effort in a short design cycle.

With higher frequency, more power consumed by next generation chips and the constraint in space on board due to growing but conflicting effort of adding more features and minimizing size of a system, optimization of board decoupling capacitances is a major issue. This paper will propose a methodology for attaching the optimal decoupling capacitors based on FDFD combined with optimization.

2. Methodology

2.1 FDFD Method

Modeling and simulation based on EM field formulations are important for accurate analysis and design of today's high-speed circuits and systems. Much research in efficient numerical techniques for EM problems has already been conducted and several types of solution algorithms have become widely recognized, such as finite difference time domain (FDTD)[2], finite-difference frequency domain (FDFD)[3], finite element, transmission line methods and others. In the following, the formulation of FDFD will be introduced.

Following Yee's notion[4], the spatial nodal points is arranged in the way that placement of **E** and **H** nodes are off in space by a space step. Therefore, every component of **H** can be obtained by the loop integral of E using the four surrounding **E** nodal values according to Maxwell's curl equation, and a similar approach holds for the calculations of **E**. Taking the Laplace transform, all the variables in the resulting ordinary differential equations become functions of complex frequency and space position.

$$\mu hsH_x(i,j,k,s)+[E_z(i,j+1,k,s)-E_z(i,j,k,s) - E_y(i,j,k+1,s)+E_y(i,j,k,s)]=\mu hH_x(i,j,k,t)\big|_{t=0} \quad (1)$$

$$\mu hsH_y(i,j,k,s)+[E_x(i,j,k+1,s)-E_x(i,j,k,s) - E_z(i+1,j,k,s)+E_z(i,j,k,s)]=\mu hH_y(i,j,k,t)\big|_{t=0} \quad (2)$$

$$\mu hsH_z(i,j,k,s)+[E_y(i+1,j,k,s)-E_y(i,j,k,s) - E_x(i,j+1,k,s)+E_x(i,j,k,s)]=\mu hH_z(i,j,k,t)\big|_{t=0} \quad (3)$$

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$$(\varepsilon hs+\sigma)E_x(i,j,k,s)+[H_y(i,j,k+1,s)-H_y(i,j,k,s)$$
$$-H_z(i,j+1,k,s)+H_z(i,j,k,s)]=\varepsilon hE_x(i,j,k,t)\big|_{t=0} \quad (4)$$
$$(\varepsilon hs+\sigma)E_y(i,j,k,s)+[H_z(i+1,j,k,s)-H_z(i,j,k,s)$$
$$-H_x(i,j,k+1,s)+H_x(i,j,k,s)]=\varepsilon hE_y(i,j,k,t)\big|_{t=0} \quad (5)$$
$$(\varepsilon hs+\sigma)E_z(i,j,k,s)+[H_x(i,j+1,k,s)-H_x(i,j,k,s)$$
$$-H_y(i+1,j,k,s)+H_y(i,j,k,s)]=\varepsilon hE_z(i,j,k,t)\big|_{t=0} \quad (6)$$

In general, the right vector is a function of the initial conditions and external sources.

2.2 Analysis flow & methodology

The method is to firstly extract S parameter of structure using FDFD. Secondly, input model into a simulator to get the time domain results and try to find out the impedance goal when the excited sources are specified. At last, based on the real capacitor characteristic, which will be discussed in next section, set the suitable initial values of decoupling capacitors and start the optimization, and output the results on time and frequency domain. The optimization flow is shown in Fig. 1.

Fig.1 Optimization flow

2.3 Frequency Domain Analysis of Real Decoupling Capacitors

In order to suppress the noise in system, especially for SSN, we generally attach multiple decoupling capacitors. But in real world, the capacitor is non-ideal with ESR (equivalent series resistance) and ESL (equivalent series inductance) values, as shown in Table 1, so they have own responding resonant frequency points.

Table 1

Type	ESR(ohm)	ESL(H)	C (F)
Decap1	0.3133	0.52e-9	100e-12
Decap2	0.2084	0.52e-9	390e-12
Decap3	0.1579	0.52e-9	1000e-12

The impedance equation of real decoupling capacitors,

$$Z=\frac{1}{j\omega C}+j\omega L+R \quad (7)$$

For the above 3 kinds of decoupling capacitor, their frequency characteristics with resonant frequencies of 6.979E8Hz, 3.534E08Hz and 2.207E08Hz are shown in Fig.2, respectively. Capacitor 1 has the highest resonant frequency and hence acts are a capacitor over the widest frequency band.

Fig. 2 Frequency response of the decoupling capacitor

This enables the suppression of high frequency resonant peaks in the power delivery system. So, we can attach the different decoupling capacitors to suppress the low, mid and high impedance noise using the characteristics of real decoupling capacitor.

3. Analysis of example

In this section, the method will be used to analyze a 6 layers PCB board in time and frequency domain through hierachical optimization. Fig.3 (a) and (b) are separately shown top view and 3D view of the structure. 6 capacitors have been distributed in two sides of board in length direction. Their values are

C 2 0 0.47e-6
L 2 3 1.0e-9
R 3 1 0.01

At the bottom side of board, multiple small value resistors have been connected with power and ground. Their values are 0.01.

Extract the responding impedances of 9 ports, which is located in center and shown in Fig.3(b). Results are shown in Fig.4(b). The computation time of whole process is about 40s in PIII 700Mhz.

Fig.3 (a). 3D view of Board
(b). Top view of Board

Suppose that the buffers are specified and the power/ground impedance noise should be below 3Ohm, in the following, discuss how much values of the decoupling capacitors should be attached.

Firstly, set the initial capacitors value to suppress the impedance noise from DC to mid frequency milestone (400Mhz). The results after opt are shown in Fig. 4(a) The decoupling caps values for each port are in **Table2**, their ESR and ESL are all 70mΩ and 0.9nH.

Secondly, calculate the pulse period of excited source and it's responding frequency if the excited source amplitude is 1.0A and slew rate is 5A/ns.The period is 2ns so the speed is 500Mhz. Using Equ.(7), estimate the capacitor value at this frequency point and attach it with

each port. The capacitor is C=0.304nF, ESL=0.333nH and ESR=21mΩ. The self-impedances of 9 ports after attached this caps and 1st optimization are shown in Fig.4 (a). If we observe the time wave at this time, we will find the noise is not evidently improved, shown in Fig.5. It is because 500M caps inserted pushed the impedance noise to low frequency end and high frequency end, respectively. So the next step is to further suppress the low frequency noise and mid frequency noise.

Thirdly, set the initial capacitors values to suppress the noise within from low frequency to high frequency. The results are shown in Fig.4 (a). The optimal caps are in **Table3**, and their ESR and ESL are all 21mΩ and 0.333nH. The original impedances compared with results after optimization at all ports are shown in Fig.4 (b).Voltages at 9 ports are shown in Fig.5 for after/before optimization.

Fig.4(a) Results comparison for the above three steps. (b) Results comparison for after opt and the original.

Fig.5 Noise voltages at port1 for four cases

4. Conclusion

In this paper, an effective method on the optimal value selection of decoupling capacitors is introduced. The method can promptly and automatically search the optimal value compared with existing methods through optimization. Besides, it has high accuracy because it is applied FDFD method to extract the model of structure. Application of two examples has further demonstrated that not only it has provided a full solution for suppressing the low, mid and high frequency noise but also it can simultaneously analyze the system in time and frequency domain.

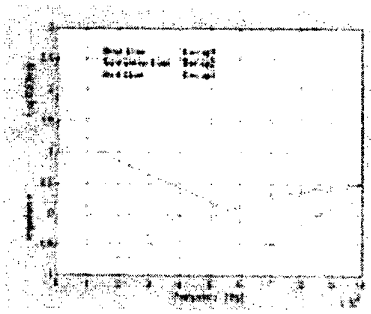

Fig. 2 Frequency response of the decoupling capacitor

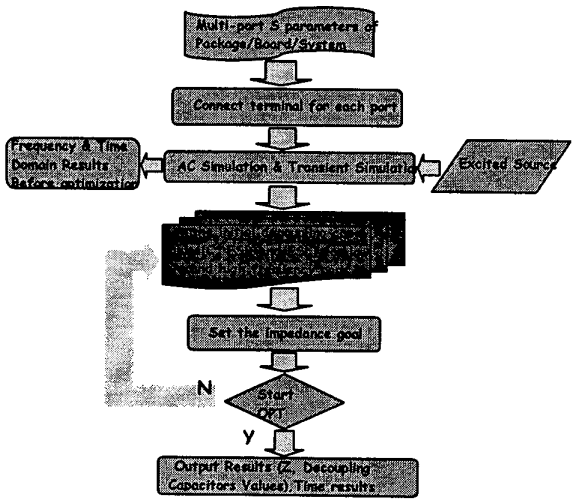

Fig.1 Optimization flow

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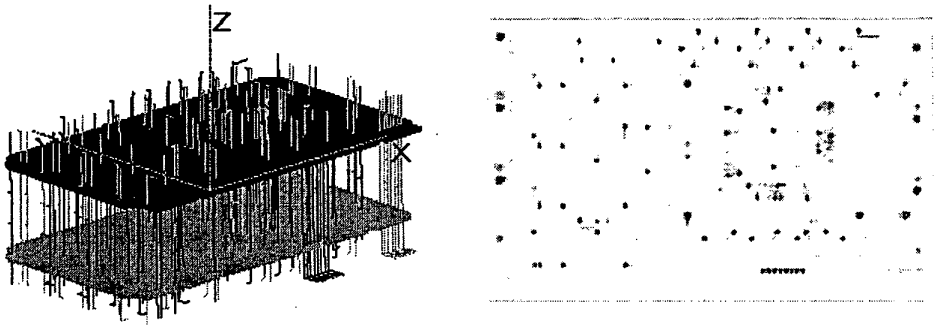
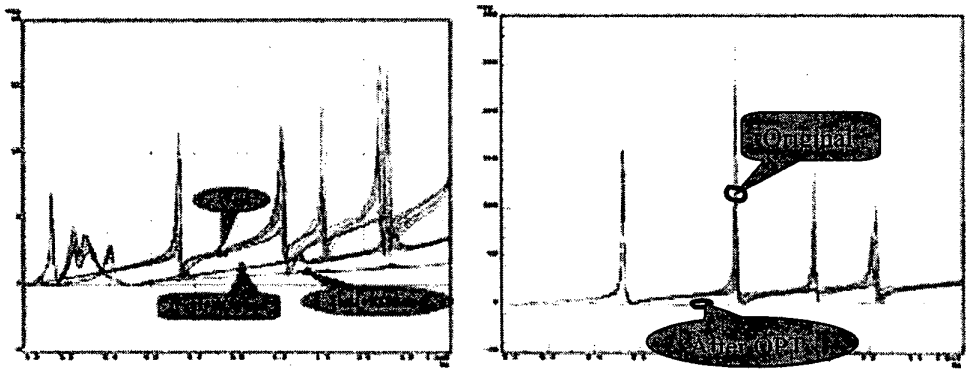


(a) (b)

Fig.3 (a). 3D view of Board . (b). Top view of Board



(a) (b)

Fig.4 (a) Results comparison for the above three steps. (b) Results comparison for after opt and the original.

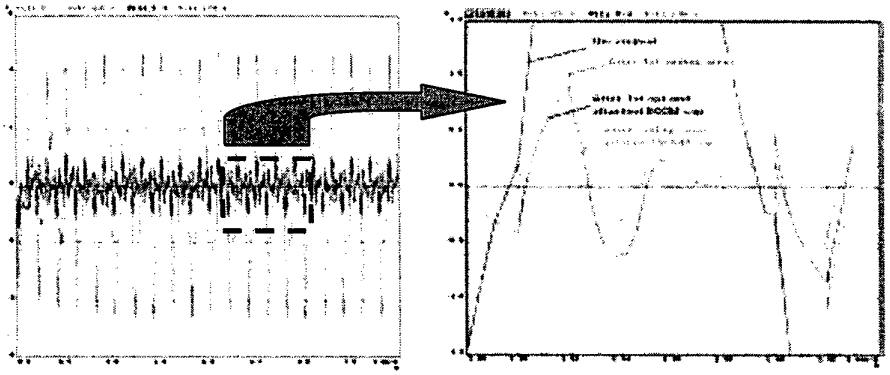


Fig.5 Noise voltages at port1 for four cases

Table2

	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9
C(nF)	32.8	33.6	35.8	44.8	60	43.9	45.2	42.6	35

Table3

	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9
C(nF)	5.8	9.9	4.1	4.1	6.8	7.2	5.2	9.0	8.5