# Power Supply Noise Aware Floorplanning and Decoupling Capacitance Placement [*]

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## ABSTRACT

*Power supply noise is a strong function of the switching activities of the circuit modules. Peak power supply noise can be significantly reduced by judiciously arranging the modules based on their spatial correlations in the floorplan. In this paper, power supply noise is, for the first time, incorporated into the cost function to determine the optimal floorplan in terms of area, wire length, and power supply noise. Compared to the conventional floorplanning which only considers area and wire length, power supply noise aware floorplanning can generate better floorplan both in terms of area and peak noise. The decoupling capacitance required by each module is also calculated and placed in the vicinity of the target module during the floorplanning process. Experimental results on MCNC benchmark circuits show that the peak power supply noise can be reduced as much as 40% and both the total area and wire length are improved due to the reduced total decoupling capacitance budget gained from reduced power supply noise.*

## 1. INTRODUCTION

Signal integrity is emerging as an important issue as VLSI technology advances to the nanoscale regime. Of particular importance among the signal integrity issues is the power supply noise. As CMOS technology scales, devices are of smaller feature size, faster switching speed, and higher integration density. Large current spikes due to a large number of "simultaneous" switching events in the circuit within a short period of time can cause considerable *IR* drop and $Ldi/dt$ noise over the power supply network [1]. Power supply noise degrades the drive capability of transistors due to the reduced effective supply voltage seen by the devices. Power supply noise may also introduce logic failures and jeopardize the reliability of high performance VLSI circuits. Recently, many research efforts [2][3][4][5][6][7] have been directed toward power supply noise analysis and power supply network optimization. Topology optimization [8], wire sizing [9], on-chip voltage regulation [10], and decoupling capacitance deployment [2][11] are the most widely used techniques to relieve power supply noise.

Decoupling capacitance (decap) placement is usually treated as an afterthought in the post-floorplanning process [12][2]. The disadvantage of this approach is that many candidate foorplans which may result in better power supply noise and smaller decap budgets are inadvertently thrown away in the traditional floorplanning.

In this paper, we propose a power supply noise aware floorplanning methodology which incorporates the power supply noise as

a factor into the cost function. The rationale behind this methodology is that power supply noise depends strongly on the switching activities in the circuit modules. The power supply noise, and therefore the total decoupling capacitance, can be significantly reduced by judiciously arranging the circuit modules in the floorplan based on their spatial correlations. For example, a cluster of high switching activity modules can overload specific power pins and generate a noisy spot in the floorplan while a scattered distribution of high switching activity modules can lead to reduced peak power supply noise and decap budget. Similar ideas have been applied to thermal placement [13][14] to smooth out the hot spots and to substrate aware mixed-signal macrocell placement [15] to reduce the substrate coupling.

Given the worst case switching activity profiles of the circuit modules, we generate the floorplan candidates using a simulated annealing method. The merit of each candidate floorplan is evaluated based on the cost function which comprises of the total area and wire length as well as the power supply noise. Decap required by each circuit module is determined and deployed in the close neighborhood along the floorplanning process. Experimental results on MCNC benchmark circuits show that peak power supply noise can be reduced as much as 40% compared to traditional floorplanning. Both area and wire length are improved due to the reduced decap budget gained from reduced power supply noise.

The rest of the paper is organized as follows. Problem formulation is given in Section 2. Floorplan generation and simulated annealing are discussed in Section 3. Power supply noise estimation is addressed in Section 4. Cost function evaluation is discussed in Section 5. Experimental results are presented in Section 6. Finally, conclusions are drawn in Section 7.

## 2. PROBLEM FORMULATION

Given a circuit with the worst case switching profiles of the modules known, we want to determine the optimal floorplan for the circuit such that the total chip area, wire length, and power supply noise can be minimized. In conventional floorplanning, area and wire length are the main objectives, and the optimality of a floorplan is measured based on the following cost function, which is a weighted sum of the chip area and total wire length.

$$\Psi = A + \lambda W,$$

where $A$ is the total area, $W$ is the total wire length, and $\lambda$ is the weight parameter. The decap deployment required for power supply noise suppression is considered as an afterthought and addressed in a post-floorplanning process.

As VLSI technology scales to the nanoscale regime, power supply noise is becoming more of a concern than ever before. Total

decap budget required for a high performance microprocessor contributes to a significant portion of the chip area. Hence, it is necessary to address power supply noise in the floor planning process so that the peak power supply noise, and therefore the decap budget, is minimized. To address the power supply noise during floor planning process, we redefine the cost function by incorporating the power supply noise into it as follows:

$$\Psi = A + \lambda_1 W + \lambda_2 V_N, \qquad (1)$$

where is $V_N$ is the cost associated with the power supply noise, and $\lambda_1$ and $\lambda_2$ are the weight parameters used in the cost function for balancing the three factors.

Fig. 1 illustrates the rationale for noise-aware floorplanning methodology. Floorplan (a) in the figure is unbalanced and the power pin 1 is overloaded compared to other power pins. As a result, the spot around power pin 1 is very noisy, and therefore requires a large decap to relieve the noise. On the other hand, floorplan (b) in the figure is more balanced as the highly active modules are scattered across the floorplan. Consequently, the peak power supply noise is reduced, and so is the decap. While the two floorplans have the same area and may look equally good in the conventional floorplanning, it does make a difference in the noise-aware floorplanning, and floorplan (b) will be chosen over floorplan (a). In typical high performance VLSI circuits, the switching activities are quite different for different circuit modules. Clock module and ALU module, for example, have much higher switching activities than other modules. It is very important to take the variations of switching activities into consideration during the floorplanning process.

Compared to conventional floorplanning, power supply noise aware floorplanning can monitor the placement of circuit modules based on the switching activities and the spatial correlation between the modules. The noise-driven floorplanning favors the balanced floorplan that has the least overall cost as determined by Eqn. (1).

The power supply noise must be suppressed below a given specified limit by placing decap in the vicinity of each module. The decap budget for a module is determined based on the power supply noise and the switching profile. Once the decap budgets for the circuit modules are determined, white space in the close neighborhood is allocated to each module for MOS capacitor fabrication. If the existing white space in the floorplan can meet the total demand, there is no area and wire length penalty. If, on the other hand, additional white space needs to be inserted into the floorplan to meet the decap demand, there will be an area penalty as well as a wire length penalty since the inserted white space will push modules apart, and therefore, increase the wire length. The cost associated with power supply noise can be converted to the area penalty $\delta A$ and the wire length penalty $\delta W$. The cost function $\Psi$ can be rewritten accordingly as follows:

$$\Psi = (A + \delta A) + \lambda_1 (W + \delta W). \qquad (2)$$

Hence, the problem is really equivalent to the generation of a floorplan with minimal overall cost as dictated by Eqn. (2) for a given circuit.

## 3. FLOORPLAN GENERATION AND SIMULATED ANNEALING

Floorplanning is an NP-hard problem. Among many heuristics proposed for floorplanning, simulated annealing [16] is one of the more effective techniques. The efficiency of a simulated annealing based algorithm hinges on the representation of the floorplan and the computation complexity involved in the representation evalua-



(a) Unbalanced      (b) Balanced
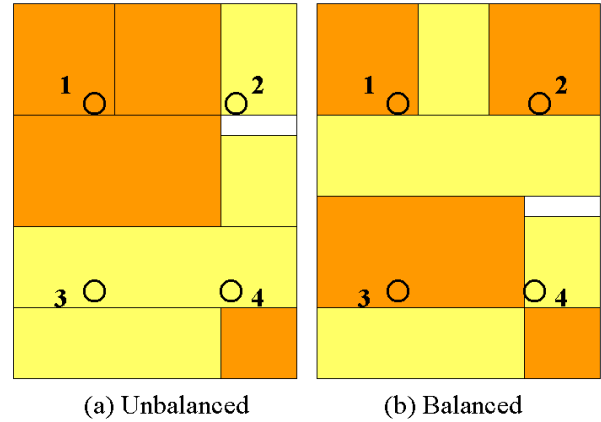
**Figure 1: Correlation between power supply noise and floorplanning – A rationale for noise-aware floor planning.**

tion. Recently, there are several significant advancements in floorplan representation– sequence pair [17], BSG[18], O-tree[19] and $B^*$-tree [20]. In the proposed noise-aware floor planning methodology, we use sequence pair to represent the floorplan. The sequence pairs are evaluated by *Longest Common Subsequence (LCS) Computation* –an efficient algorithm of complexity $O(n \log \log n)$ proposed in [21] for fast sequence pair evaluation.

Our proposed power supply noise aware floorplanning methodology is implemented based on a simulated annealing technique. An initial floorplan is generated by aligning the circuit modules in one row. Initial temperature is determined based on a statistical technique proposed in [16]. Current floorplan is perturbed by performing one of the legal movement operations defined in [17], such as switching the order of two modules in the sequence pair or rotating a module by 90°. The merit of the perturbed floorplan is evaluated according to the cost function given in Eqn. (2).

$$\Psi = (A + \delta A) + \lambda_1 (W + \delta W).$$

If the perturbed floorplan has a smaller cost, the movement is accepted. Otherwise, the perturbed floorplan is accepted with a probability of $e^{-\Delta\Psi/T}$. The simulated annealing procedure is detailed in Fig. 2.

The area $A$ of the floorplan is easy to calculate since the total width and height of the floorplan are known after the sequence pair evaluation using the LCS algorithm. The wire length for a net is calculated as half the perimeter of the bounding box. The total wire length $W$ can be easily calculated once we know the position of each module in the floorplan. The LCS algorithm calculates the module positions as the sequence pair is evaluated.

The difficult part of the cost function evaluation is to determine the cost associated with power supply noise. Details about power supply noise estimation are given in Section 4. As discussed in Section 2, the cost associated with the power supply noise is determined by the area penalty $\delta A$ and the wire penalty $\delta W$. The exact $\delta A$ and $\delta W$ can be determined only when the existing white space in the floorplan is allocated with a linear programming (LP) technique. The LP problem is computationally expensive and we can not afford to solve it for every run in the simulated annealing process. To resolve this, LP programming is solved only at low temperature to determined the exact $\delta A$ and $\delta W$, while estimated $\delta A$ and $\delta W$ are used for cost function evaluation at high temperature. Details about cost function evaluation at both high temperature and

```
Algorithm Simulated Annealing
    Initial floorplan; T_0 = INIT_T
    while T_k > T_Frozen
        Perturb_Current_Floorplan()
        Estimate_Power_Supply_Noise()

        if  T_k > T_LOW
            Evaluate_Cost_Function_T_HIGH()
        else
            Evaluate_Cost_Function_T_LOW()

        ΔΨ = Ψ_new − Ψ_old

        if  ΔΨ < 0
            Accept the perturbed floorplan
            Ψ_old = Ψ_new
        else
            Accept the floorplan with probability e^{−ΔΨ/T_k}

        k = k + 1; T_k = rT_{k−1}

END  Simulated Annealing
```

**Figure 2: Simulated annealing algorithm for power supply noise aware floorplanning.**

low temperature in the simulated annealing algorithm are presented in Section 5.

# 4. POWER SUPPLY NOISE ESTIMATION

The power supply noise estimation is key to the cost function evaluation in the simulated annealing process. The estimation has to be fast and with reasonable accuracy. We use an efficient technique proposed in [12] to calculate power supply noise. For completeness of presentation, the essence of the technique is summarized here.

Power supply network is modeled as an RLC mesh with the circuit modules modeled as current sinks that are sourcing currents from the power mesh. The current sourcing by a module is assumed to come only from the neighboring VDD pins and the contribution from remote VDD pins is small, and therefore ignored as illustrated in Fig. 3 [12]. The contribution from each of the neighboring VDD pins is determined as follows. Suppose that there are $N$ ($N = 4$ in most cases) neighboring $VDD$ pins surrounding a sink. Let $Z_1, Z_2, \ldots, Z_N$ be the impedances between the current sink to the $N$ neighboring $VDD$ pins, respectively. Let $I$ be the current a sink is sourcing from the power network. Let $I_1, \ldots, I_N$ be the currents contributed by the $N$ neighboring $VDD$ pins, respectively. $I_1, \ldots, I_N$ are given by the following equations:

$$
\begin{aligned}
I_1 + I_2 + \ldots + I_N &= I & (a)\\
Z_1 I_1 = Z_2 I_2 = \ldots &= Z_N I_N & (b)\\
Y_j = \frac{1}{Z_j} \quad j &= 1, 2, \ldots, N & (c)\\
\Rightarrow \quad I_j = \frac{Y_j}{\sum_{i=1}^{N} Y_i} I, \quad j &= 1, 2, \ldots, N, & (d)
\end{aligned}
\tag{3}
$$

where $Y_j$ is the admittance from the sink to $VDD$ pin $j$.

Once the current contributions $I_j$ ($j = 1, 2, \ldots, N$) from the neighboring $VDD$ pins are determined, we distribute $I_j$ among the dominant paths (paths of least, second least impedances) from $VDD$ pin

$j$ to the sink [12]. Let $\{P_1, P_2, \ldots, P_w\}$ denote the ordered set of the shortest paths and the second shortest paths under consideration. Let $Y_{P_1}, Y_{P_2}, \ldots, Y_{P_w}$ be the admittance of these paths. The current $I_j$ can be distributed among these paths, denoted by $i_{P_1}, i_{P_2}, \ldots, i_{P_w}$, as follows:

$$
\begin{aligned}
i_{P_1} + i_{P_2} + \ldots + i_{P_w} &= I_j,\\
i_{P_k} = \frac{Y_{P_k}}{\sum_{i=1}^{w} Y_{P_i}} I_j, \quad k &= 1, 2, \ldots, w.
\end{aligned}
\tag{4}
$$

Given the mesh topology and the switching current waveforms of the circuit modules, we can approximately determine the distribution of those switching currents among the power supply network as illustrated above.
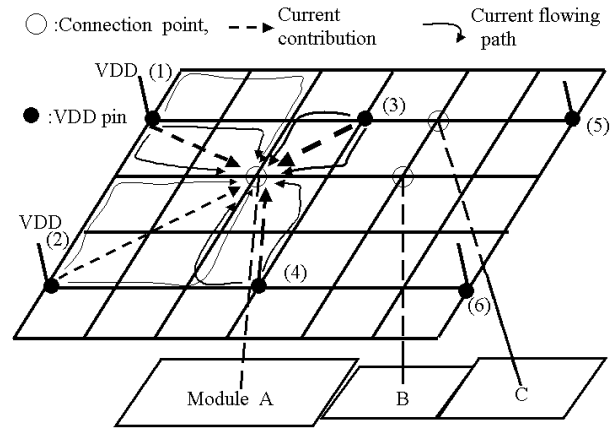


**Figure 3: Power Supply Network–Mesh Structure**

The power supply noise that a circuit block experiences can be estimated by calculating the voltage difference between the connection point and its neighboring power supply pins [12]. Suppose $P_k$ is a dominant current path between the connection point of circuit module $k$ and the $VDD$ pin closest to it. Let $T^{(k)} = \{P_j : P_j \cap P_k \neq \emptyset\}$ be a collection of the current paths in the power supply mesh that overlap with path $P_k$ (including $P_k$ itself). Let $P_{jk} = P_j \cap P_k$ denote the overlapping part between path $P_j$ and path $P_k$, $r_{P_{jk}}$ denote the resistance of $P_{jk}$, and $l_{P_{jk}}$ denote the inductance of $P_{jk}$. Let $V_{noise}^{(k)}$ denote the power supply noise at module $k$. $V_{noise}^{(k)}$ can be calculated using Kirchhoff's Voltage Law (KVL):

$$
V_{noise}^{(k)} = \sum_{P_j \in T^{(k)}} \left( i_j r_{P_{jk}} + l_{P_{jk}} \frac{di_j}{dt} \right),
\tag{5}
$$

where $i_j$ is the current flowing along path $P_j$. We should point out that not only the switching current of module $k$ contributes to $V_{noise}^{(k)}$, other modules that draw current from the same $VDD$ pins as module $k$ contribute as well, as long as their current distribution paths overlap with $P_k$. This explains why power supply noise is sensitive to the spatial correlations between modules.

# 5. COST FUNCTION EVALUATION

In this section, we will evaluate the cost associated with power supply noise, namely the area penalty $\delta A$ and the wire length penalty $\delta W$ in Eqn. (2). First, decoupling capacitance budgets are estimated, and then the cost function evaluation at high simulated temperature and low simulated temperature is addressed in the following subsections.

## 5.1 Decoupling Capacitance Estimation

Suppose there are $M$ modules in the floorplan, and the switching current of module $k$ is $i^{(k)}$, $k = 1, 2, \ldots, M$. Let $C^{(k)}$ be the decoupling capacitance required for circuit module $k$. Let $Q^{(k)}$ be the total charge that module $k$ will draw from the power supply network during the worst case switching process. $Q^{(k)}$ is given by the following equation:

$$Q^{(k)} = \int_0^\tau i^{(k)}(t)dt,$$

where $\tau$ is the duration that the switching process lasts. The decoupling capacitance required for each circuit module can be estimated as follows:

$$\theta = max(1, \frac{V_{noise}^{(k)}}{V_{noise}^{(lim)}}),$$
$$C^{(k)} = (1 - 1/\theta)Q^{(k)}/V_{noise}^{(lim)}, \quad k = 1, 2, \ldots, M. \quad (6)$$

Suppose the estimated power supply noise (before considering decap) of module $k$ is $\theta$ times the tolerable noise limit $V_{noise}^{(lim)}$. In order to reduce the power supply at module $k$ to $V_{noise}^{(lim)}$, we need to scale the noise at module $k$ by a factor of $\theta$, which is achievable if we scale down all the currents that contribute to $V_{noise}^{(k)}$ by a factor of $\theta$ according to Eqn. (5). The current flowing through the network can be reduced to $1/\theta$ of its value by adding enough decap to buffer $(1 - 1/\theta)$ portion of the current load. Since the decap at module $k$ is only responsible for providing the switching current of module $k$, the decap $C^{(k)}$ should be such that when its voltage is lowered from $Vdd$ to $(Vdd - V_{noise}^{(lim)})$, it will release $(1 - 1/\theta)Q^{(k)}$ amount of charge to supply the demand of module $k$ during the switching process, which leads to $C^{(k)}V_{noise}^{(lim)} = (1 - 1/\theta)Q^{(k)}$. When $V_{noise}^{(k)} \le V_{noise}^{(lim)}$, no decap is required.

## 5.2 Cost Function Evaluation at High Simulated Temperature

On-chip decaps are usually fabricated as MOS capacitors. The unit area capacitance of a MOS capacitor is given by $C_{ox} = \varepsilon_{ox}/t_{ox}$, where $t_{ox}$ is the oxide thickness, and $\varepsilon_{ox}$ is the permittivity of $SiO_2$. The decoupling capacitance budget for each circuit module is converted to the area of silicon required to fabricate the decap as follows:

$$S^{(k)} = C^{(k)}/C_{ox}, \quad k = 1, 2, \ldots, M, \quad (7)$$

where $S^{(k)}$ is the white space required to fabricate $C^{(k)}$.

Decaps need to be placed in the close neighborhood of switching activities to effectively relieve the power supply noise. Decaps located far from the noisy spot are not effective due to the longer $RC$ delay time and the $IR$ drop [2]. The total area required for decap fabrication, denote as $S_{decap}$, is given as follows:

$$S_{decap} = \sum_{k=1}^{M} S^{(k)}.$$

The existing white (empty) space (WS) in the floorplan, denoted by $S_{exist}$ can be easily calculated. Part or all of the existing WS can be used for decap fabrication depending where the existing WS locates in the floorplan. We do not know exactly how much of the existing WS can be used for decap until a linear programming (LP) technique is used to allocate the existing WS to the neighboring circuit modules based on their decap demand. Unfortunately, LP is

expensive to solve, and we cannot afford to do that at high simulated temperature. We can, however, assume that $\gamma$ portion of the existing WS is accessible for decap fabrication, and the additional WS that needs to be added to the floorplan is given by:

$$\delta A = max(0, S_{decap} - \gamma S_{exist}).$$

$\delta A$ is the area penalty due to power supply noise (or decap) in the cost function. If $\delta A$ is 0, there is no penalty to wire length; Otherwise, the additional $\delta A$ WS is inserted into the floorplan as WS bands between the levels of circuit modules as illustrated in Fig. 4. Since we do not know exactly how the existing WS is allocated to the modules, we assume the additional WS $\delta A$ is distributed evenly between levels of modules in the floorplan. Then the width of the WS band, denoted by $B_{WS}$, can be easily calculated based the totoal module levels, denoted by $d$, the dimensions of the floorplan, and $\delta A$.

$$B_{WS} = \delta A/d * LayoutX,$$

where $LayoutX$ is the width of the floorplan. Module positions are updated after WS insertion. Wire length is recalculated. The change of the wire length is the wire length penalty.

$$\delta W = W_{updated} - W_{old}.$$

The $Evaluate\_Cost\_Function\_T_{HIGH}()$ function performs the cost function evaluation at high temperature as illustrated above.

## 5.3 Cost Function Evaluation at Low Simulated Temperature

At low simulated temperature, the isolated WS's in the floorplan can be allocated to the neighboring circuit modules based on their decap demands using a linear programming (LP) technique to maximize the utilization of existing WS. Suppose there are $H$ isolated WS modules with area $A_k$, $k = 1, 2, \ldots, H$, in the existing floorplan. Let $N_k = \{j : module\ j\ is\ adjacent\ to\ WS\ module\ k\}\ k = 1, 2, ..., H$, denote a set of circuit modules neighboring WS module $k$. Let $x_k^{(j)}$ be the amount of WS allocated to circuit module $j$ from WS module $k$. The WS allocation problem can be formulated as follows:

$$
\begin{aligned}
maximize \quad S \ &= \ \sum_{k=1}^{H} \sum_{j \in N_k} x_k^{(j)}, \\
subject\ to \quad \sum_{j \in N_k} x_k^{(j)} \ &\le \ A_k, \ k = 1, 2, \ldots, H, \\
\sum_{k=1}^{k=H} x_k^{(j)} \ &\le \ S^{(j)}, \ j = 1, 2, \ldots, M, \\
x_k^{(j)} \ &\ge \ 0, \quad \forall k, \forall j, \quad (8)
\end{aligned}
$$

where $S$ is the total WS allocated. The first set of constraints guarantee that the total WS allocated from a WS module $k$ is less than or equal to its area $A_k$. The second set of constraints guarantee that the WS allocated to a circuit module $j$ is less than or equal to its WS demand $S^{(j)}$, because there is no need to over-supply its WS demand. The third set of constraints guarantee that all the allocations are positive.

After we solve the LP problem, we know exactly how the existing WS modules are allocated to the circuit modules and how much WS is inaccessible. We compute the updated white space demand $\tilde{S}^{(j)}$, $j = 1, 2, ..., M$, for all circuit modules after the WS allocation as follows:

$$\tilde{S}^{(j)} = S^{(j)} - \sum_{k=1}^{H} x_k^{(j)}, \quad j = 1, 2, \ldots, M.$$

The additional amount of WS $\delta A$ that needs to be inserted into the floorplan is determined as:

$$\delta A = \sum_{j=1}^{M} \tilde{S}^{(j)} = \sum_{j=1}^{M} S^{(j)} - S.$$

If $\delta A = 0$, allocation process is complete; Otherwise, we need to insert $\delta A$ into the floorplan such that the WS can be used for decoupling capacitance allocation. The $\delta A$ is the area penalty in the cost function associated with power supply noise.

We use a heuristic to insert $\delta A$ into the floorplan. The WS is inserted by extending the floorplan dimensions in both x-direction and y-direction. Suppose $\alpha$ portion of the additional WS $\delta A$ is obtained by extending the floorplan in y-direction, and $(1 - \alpha)$ portion of $\delta A$ is obtained by extending the floorplan in x-direction. Let *LayoutX* and *LayoutY* be the width and height of the original floorplan. The extensions of the floorplan in x-direction and y-direction, denoted by *ExtX* and *ExtY*, are given as follows:

$$ExtY = \frac{\alpha \delta A}{LayoutX}; \quad ExtX = \frac{(1-\alpha)\delta A}{(LayoutY + ExtY)}.$$

The heuristic works as follows: The modules in the floorplan are
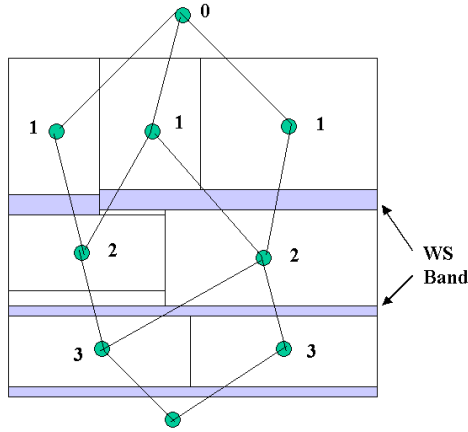


**Figure 4: Inserting additional white space between levels of modules.**

levelized according to their depth in the constraint graph [22] with the source node in the graph at depth 0. First we move the circuit modules in y-direction level by level. We move the modules in the top level by *ExtY*, then the levels below it are moved subsequently as illustrated in Fig. 4. We insert WS bands between the levels by shifting the adjacent rows by different amounts in y-direction. The width of the WS band is determined by the WS demand of the circuit modules in the previous row. The width of the WS band inserted between level $j - 1$ and level $j$, denoted by $B_{WS}^{(j-1)}$ is given as follows:

$$B_{WS}^{(j-1)} = \frac{\sum_{i \in level \ (j-1)} \alpha \tilde{S}^{(i)}}{LayoutX}.$$

The inserted WS band provides $\alpha$ portion of the WS demanded by the circuit modules in row $j - 1$.

Similarly, WS bands are inserted between columns by moving the modules in x-direction.

$$B_{WS}^{(k-1)} = \frac{\sum_{i \in column \ (k-1)} (1-\alpha) \tilde{S}^{(i)}}{LayoutY + ExtY}.$$

**Table 1: Technology parameters**

| Parameters | Description | Value |
|---|---|---|
| $r$ | wire resistance per unit length ($\Omega/\mu m$) | 0.0125 |
| $l$ | wire inductance per unit length ($pH/\mu m$) | 0.8 |
| $c$ | wire capacitance per unit length ($fF/\mu m$) | 20 |
| $L_P$ | package inductance per VDD pin ($nH$) | 0.2 |
| $R_P$ | package resistance per VDD pin ($\Omega$) | 0.5 |

Since the modules are pushed further apart after the additional $\delta A$ WS is inserted into the floorplan, the total wirelength should be recalculated to determine the wire length penalty $\delta W$. Since we know exactly how the modules are moved around, we update the positions of the modules. New wire length can be calculated based on the updated positions. The wire length penalty is :

$$\delta W = W_{updated} - W_{old}.$$

Function $Evaluate\_Cost\_Function\_T_{LOW}()$ evaluates the cost function of each intermediate floorplan at low simulated temperature following exactly the procedures outlined above.

The proposed heuristic for additional WS insertion does not incur extra WS other than required, which is the advantage of the approach. Other heuristics may also work.

*Remark: The decap budgets may be slightly changed when inserting additional white space into the floorplan since module positions are changed. However, the additional white space inserted is no larger than 8.1% of the chip area from the experimental results, and the additional white space is inserted between the rows and columns of modules by extending the original floorplan both horizontally and vertically. The dimensions of the floorplan increase by less than 4% in both directions. The relative change of the module positions is about 4% since the increase is distributed between the rows and columns of the modules. The current distribution, and consequently the noise and decap budgets, change slightly. In the worst case, the modification can be taken care of by iteration, and the extension is straightforward.*

## 6.   EXPERIMENTAL RESULTS

The proposed power supply noise-aware floor planning methodology is implemented in C. The linear programming part of the algorithm is solved using Matlab by invoking a system call to Matlab in our C program. Experiments are performed on five MCNC [23] benchmark circuits implemented in $0.25\mu m$ technology. The pitch for the metal lines in the power supply mesh is $333.3\mu m$, and the pitch for *VDD* pins is $1000\mu m$. The power supply voltage is $2.5V$. The parameters such as unit length parasitics of the metal grids in the power supply network are provided by a leading semiconductor company. The technology parameters are listed in Table 1. The worst case switching current profiles for the circuit modules are generated as follows. The worst case current density $j_s$ is estimated for $0.25\mu m$ technology based on the technology parameters, such as integration density, transistor channel length, obtained from ITRS'97 Roadmap [24]. The peak switching current for a circuit module $k$ is $I^{(k)} = factor[k] * j_s A_k$, where $A_k$ is the area of module $k$, and $factor[k]$ is either 1 or 2 depending on the random number generated. If the $factor[k]$ is 2, we regard the module $k$ as a highly active module, otherwise, module $k$ is a low activity module. The overall switching current waveform of module $k$ is approximated

with a triangular waveform with peak value $I^{(k)}$, and the duration of the switching current waveform ($\tau$) is assumed to be half the clock cycle. Our method is, however, not limited to the triangular waveform assumption, and more sophisticated piece-wise linear waveforms can be used to represent the switching current waveforms of the circuit modules. In our experiments, $j_s$ is set to $0.2\mu A/\mu m^2$, and $\tau$ is set to $1ns$. The power supply noise limit $V_{noise}^{(lim)}$ is set to be $0.25V$.

The typical value of $\gamma$ ranges from 0.3 to 0.8. The solution quality is sensitive to the value of $\gamma$, but there is no general trend for all the circuits. In the experiments, the $\gamma$ value is adjusted around 0.5. We assume that the area and the wire length are equally important, so we set $\lambda$ to 1.

The $T_{LOW}$ is a parameter that can be adjusted based on the run-time allocated and the split of run-time between the high-temperature evaluation and the low-temperature evaluation. In our experiments, the run-time is split evenly, and the $T_{LOW}$ is set to $e^{-20}$.

The experimental results from noise-aware floorplanning are presented in Table 2 and Table 3 in comparison with the results from post-floorplanning approach. Compared to conventional floorplanning, the peak power supply noise and the total decap are reduced for all the five circuits as shown in Table 2. For *apte* and *xerox*, the peak power supply noise is reduced by 40% and 27.7%, and the decap is reduced by 21.0% and 13.2% respectively. On average, the peak power supply noise is reduced by 20.4%, and the decap budget is reduced by 11.5%. The reason that the decap is not reduced as much as the peak power supply noise is that while the noise-aware floorplanning approach can reduce the peak power supply noise by scattering highly active modules across the floorplan, it does, in the meantime, increase the power supply noise at other quiet spots. The overall decoupling capacitance is reduced, and the distribution of power supply noise becomes more even across the floorplan. For circuit *ami33*, the floorplan generated with conventional floorplanning is very close to the floorplan generated with power supply noise aware floorplanning. There is not much room for improvement for both peak supply noise and the decap. The CPU time is also presented in Table 2. The noise-aware planning method is more than an order of magnitude slower than the post-floorplanning approach.

The area of the final floorplans (after decap placement) of the five benchmark circuits are shown in Table 3. The floorplans produced by power supply noise aware floorplanning algorithm have smaller area than the corresponding floorplans from post-floorplanning. The area reduction for circuit *hp* is about 2.9% of its floorplan area. The area savings for circuits *apte* and *xerox* are 0.93% and 1.3% of its floorplan area, respectively. The average area reduction of the benchmark circuits is 1.2%.

As for the wire length, most of the benchmark circuits have improved total wire length due to the reduced decap gained from noise-aware floor planning. The total wire length for *hp*, however, increases. This is due to the fact that the gain from decap outweighs the loss to wire length and the overall cost of the floorplan is improved. For comparison purposes, the sums of the area and wire length obtained with the two floorplanning approaches are also listed in Table 3.

## 7. CONCLUSIONS

In this paper, we propose a power supply noise aware floorplanning methodology. Power supply noise is incorporated into the cost function of a simulated annealing based floorplanning algorithm. Compared to the conventional floorplanning which only considers area and wire length, power supply noise aware floorplanning can

generate better floorplan both in terms of area and peak noise. Experimental results on MCNC benchmark circuits show that the peak power supply noise can be reduced as much as 40%, and both the total area and wire length are improved due to the reduced total decoupling capacitance budget gained from reduced power supply noise. Decoupling capacitance required by each module is also determined and deployed in its vicinity so that the power supply noise is suppressed below a specified limit.

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**Table 2: Comparison of experimental results: "Noise-aware" vs "Post-floorplan"** ($\lambda = 1$)

| Circuit | peak noise (post) (V) | peak noise (noise-aware) (V) | percentage improved (%) | decap (post) (nF) | decap (noise-aware) (nF) | percentage improved (%) | time (post) (s) | time (noise-aware) (s) |
|---|---|---|---|---|---|---|---|---|
| apte | 2.05 | 1.23 | 40.0 | 20.72 | 16.36 | 21.0 | 12 | 119 |
| xerox | 1.63 | 1.18 | 27.7 | 6.74 | 5.85 | 13.2 | 18 | 193 |
| hp | 1.61 | 1.42 | 11.8 | 4.45 | 4.12 | 7.4 | 16 | 215 |
| ami33 | 0.38 | 0.35 | 7.9 | 0.085 | 0.084 | 1.2 | 45 | 956 |
| ami49 | 1.7 | 1.45 | 14.7 | 9.34 | 8.00 | 14.3 | 57 | 1582 |

**Table 3: Experimental results for MCNC benchmark circuits** ($\lambda = 1$)

| Circuit | Modules | area (noise-aware) ($\mu m^2$) | area (post) ($\mu m^2$) | wire length (noise-aware) ($\mu m$) | wire length (post) ($\mu m$) | A+W (noise-aware) | A+W (post) |
|---|---|---|---|---|---|---|---|
| apte | 9 | 50235794 | 50705710 | 595920 | 830445 | 50831714 | 51536155 |
| xerox | 10 | 20581079 | 20850453 | 545615 | 556625 | 21126694 | 21407078 |
| hp | 11 | 10559300 | 10876803 | 186952 | 184126 | 10746252 | 11060929 |
| ami33 | 33 | 1253960 | 1254350 | 85884 | 87359 | 1339844 | 1341709 |
| ami49 | 49 | 37548000 | 37766000 | 1125750 | 1277880 | 38673750 | 39043880 |

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