Macromodeling of Digital Libraries for Substrate Noise Analysis

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ABSTRACT

The demand for low cost, low power, and small area electronic devices calls for system-on-a-chip (SoC) designs. Integration of complex digital blocks and high performance analog functions onto single SoCs induces signal integrity between noisy digital circuits and sensitive analog sections. Such signal integrity degrades the performance of analog circuits and even causes functional failures of victim circuits. In order to account for this interference in circuit design phases, substrate noise analysis becomes particularly important, especially in deep submicron digital and mixed-signal circuits. To this end, it is critical to estimate efficiently and accurately the noise injection from the digital circuit with tens of millions of transistors. In this work, we develop *techniques that automatically extract* low-complexity time-varying macromodels for digital blocks, at the cell library building phase. Tailored for substrate noise analysis, the extracted macromodel includes three major noise injection mechanisms. The efficacy and accuracy of our macromodel are confirmed in the simulation results. Thanks to the linear time-varying (LTV) model reduction based on the Time-Varying Padé (TVP) method, our macromodel extraction features high accuracy with affordable complexity. Equally attractive is the accurate-by-construction substrate noise model generation by merging the macromodel extraction into cell library building phase.

I. INTRODUCTION

The demand for electronic devices with high performance, low cost and low power consumption, together with continuously advancing silicon technology, results in an increasing number of system-on-a-chip (SoC) designs. Such designs give rise to *signal integrity problems* between noisy digital circuits and sensitive analog sections. A major cause for signal integrity problems is *substrate coupling*, defined as any voltage deviation in the bulk node of a device caused by currents propagating through a substrate [8]. When thousands of transistors in the digital circuit switch, they inject considerable current into the common substrate. This injected current travels through the substrate and eventually interferes with analog circuits on the same die. As feature sizes decrease and clock frequencies increase, the substrate noise created by digital switching increases dramatically. Therefore, in nanometer process (0.25μm and below), substrate noise analysis becomes increasingly important.

Substrate noise analysis consists of the following components: i) calculation of the amount of currents injected by the digital circuitry into the substrate; ii) modeling of the path that leads the injected currents to the analog circuitry, i.e., extraction of the substrate model; iii) evaluation of substrate noise impact on the analog circuitry. In this paper, we will concentrate on the first component.

The most accurate means to quantify the substrate interference would be the full SPICE model. However, its feasibility is questionable due to the large digital circuit size. Not to mention the inclusion of package model, substrate model, and power supply model. In the literature, several approaches have been proposed to speed up the computation by replacing the SPICE model of digital blocks with their corresponding macromodels. These approaches include: a macromodel consisting of a current (noise) source that is obtained by running the SPICE model for each gate [12]; a model utilizes capacitors controlled by ideal switches [3]; and a model that stores in a cell library independent time varying current sources for individual cells [4].

Nevertheless, to reduce complexity, these approaches sacrifice accuracy. This is because all of them rely on manually derived models, which yields an accuracy that is heavily dependent on the individual researcher's understanding of the physical nature of the digital circuits. Reminiscent of existing macromodels, we also start from the SPICE-level circuit descriptions. But different from all existing works, in this paper we provide a new perspective by introducing an *automatically* generated macromodel for substrate noise analysis.

The automatic feature of our approach stems from the fact that the low-complexity models are generated using algorithms. More specifically, the digital circuit is first partitioned into digital cells each containing one or more nonlinear devices. We then convert each of these digital cells into a LTV macromodel, and collect all of them in a cell library. Notice that the conversion/extraction and collection can be carried out off-line, and thereby does not hinder the real-time substrate noise computation. The latter can be implemented by "dragging-and-dropping" corresponding macromodels from the library into the chip-level substrate noise analysis representation.

The simulation results confirm that: compared to SPICE model, our macromodel approach is up to *160* times as fast, with only 3.21% peak noise error. Summarizing, by slightly modifying cell characterization methodology, our macromodel extraction is capable of generating bottom-up accurate-by-construction models for full-chip substrate noise analysis.

The rest of the paper is organized as follows. In Section II, we will present three major noise injection mechanisms. In Section III, the development of our macromodel will be presented in conjunction with a brief review of TVP. Macromodel examples, together with simulations and comparisons, will be presented in Section IV. Finally, summarizing remarks will be given in Section V.

II. NOISE INJECTION MECHANISMS

Since all transistors and contacts are connected to the substrate directly or through reverse biased junctions, noise can be injected to the substrate through several mechanisms. Among all noise injection mechanisms, we will briefly review three major ones in this section.

A. Noise Injection through Contacts

When digital circuits operate, transistors switch on and off at the same rhythm. Consequently, current spikes are generated in power supply lines. Flowing through bond wires and package lead frames, the current spikes induce noise in the power lines due to the impedance of the package and wires by $L(dI/dt)$ and IR, as shown in Figure 1. Such noise is known as simultaneous

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switching noise (SSN), or, delta-I noise. As a result, power supply lines in digital circuits are contaminated by SSN. With tens of millions of transistors on a single chip, the SSN can easily reach hundreds of millivolts.

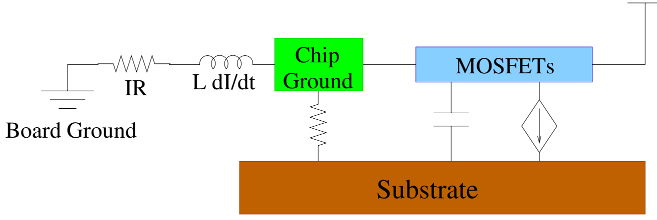

Fig. 1. Current spikes flow through bond wires and package lead frames cause fluctuations in the internal supply voltage. During switches, MOSFETs also inject currents to substrate through capacitive coupling and impact ionizations

Current spikes can also be generated when the load capacitance is charged or discharged. The latter occurs due to the state change at the IC outputs. As the current spikes flow through the pins and bond wires, voltage fluctuations can be observed.

Both SSN and the voltage fluctuations on the I/O pad will induce current injection into the substrate through resistive P^+ contacts.

B. Noise Injection through Capacitive Junctions

In digital circuits, routine MOSFET operations implicate capacitance-alike behavior of the junctions between transistors and the substrate. This is because they are reversely biased. This capacitance plays the role of connecting bridge for current leak from switching MOSFETs. The magnitude of this current leakage is proportional to the transient speed and the junction capacitance. As a result, noise injection becomes increasingly important in high speed digital circuits.

C. Impact Ionization

It is well known that strong electric field exists between drain and source in submicron transistors. The presence of such a strong electric field enables electrons (in NMOS devices) to acquire sufficient energy to become "hot." These hot electrons impact the drain, produce ionization and dislodging holes that are swept to the substrate, which appear as substrate currents [1]. This impact ionization current density is typically in the order of mA/μm, and thereby dominates junction leakage. As technology advances, the channel length keeps shrinking, but the power supply voltage decreases at a slower pace. Consequently, the electric field increases, and can lead to intensive electron-hole pair generation [6]. Different from NMOS transistors, hot carrier induced substrate currents are smaller in PMOS transistors, due to the lower mobility of holes.

III. Macromodel for Noise Injection

Based on these three noise injection mechanisms, we will next develop a macromodel that is extracted from a SPICE-level description. Any circuit connected to a noisy power supply can be represented by modeling the power supply noise as a *small* system input $u(t)$, in addition to the *large* signal vector containing its logic inputs $\boldsymbol{b}_l(t)$[1]. The resultant nonlinear system driven by both inputs are given by:

$$\frac{d\boldsymbol{q}(\boldsymbol{y}(t))}{dt}+\boldsymbol{f}(\boldsymbol{y}(t))=\boldsymbol{b}_l(t)+\boldsymbol{b}u(t),\ \boldsymbol{z}_t(t)=\boldsymbol{d}^T\boldsymbol{y}(t), \qquad (1)$$

[1] For notational simplicity but without loss of generality, we do not consider the effects of ground bounce here, since the latter can be included in the same manner as the power supply noise.

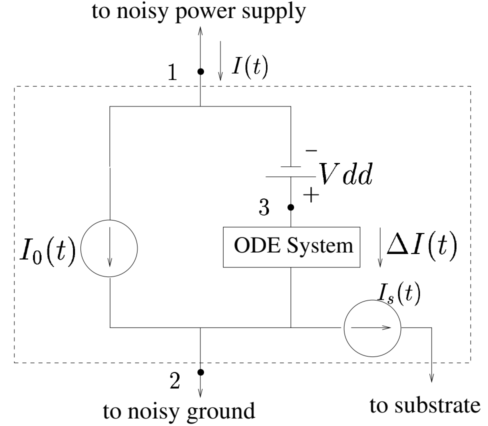

Fig. 2. Proposed macromodel of a digital cell.

where $\boldsymbol{b}$ is the vector that links the small-signal input (that is, the power supply noise) to the rest of the system, $\boldsymbol{y}(t)$ is a $m\times 1$ vector containing a total of m unknown node voltages and branch currents; $\boldsymbol{q}(\cdot)$ and $\boldsymbol{f}(\cdot)$ are nonlinear functions describing the charge/flux and resistive terms in the cell, respectively; the system outputs $\boldsymbol{z}_t(t)$ consist of current flows to ground and current leaks to substrate; and $\boldsymbol{d}$ is the vector that link the output to the rest of the system. Notice that one of the system outputs is current drawn from power network induced not only by the logical input of the digital cell $\boldsymbol{b}_l(t)$, but also by the power supply noise captured by $u(t)$. In contrast, the macromodel in [4] can be interpreted as a solution of 1 with $u(t) = 0$ over a time period (usually a clock cycle). In other words, [4] assumes perfect power supply voltage, which implies that no interaction between the device current and the supply voltage is captured. It has been recently shown that when the power supply voltage drops 10% from (the ideal value) $2V$ in a 0.25μm technology, the peak current through an inverter changes more than 30%. Unfortunately, such an error is inherited to any SSN estimation methods utilizing the model as in [4].

In order to establish a small-sized macromodel that can be generated automatically from SPICE-level circuit descriptions, we adopt a general method called TVP [9]. This method was developed originally for mixed-signal/RF/analog circuits, and was applied to mixers and switched-capacitor filters. However, if appropriately adapted, TVP can be readily applied to substrate noise analysis by reducing large digital logic blocks for *SSN and IR drop prediction purposes*, as we develop and demonstrate here.

Separating the time scales of the small input $u(t)$ and the logic input $\boldsymbol{b}_l(t)$, (1) can be re-expressed in MPDE form as:

$$\frac{\partial \boldsymbol{q}(\hat{\boldsymbol{y}})}{\partial t_1}+\frac{\partial \boldsymbol{q}(\hat{\boldsymbol{y}})}{\partial t_2}+\boldsymbol{f}(\hat{\boldsymbol{y}}(t_1,t_2)=\boldsymbol{b}_l(t_1)+\boldsymbol{b}u(t_2)$$
$$\hat{\boldsymbol{z}}_t(t_1,t_2)=\boldsymbol{d}^T\hat{\boldsymbol{y}}(t_1,t_2) \qquad \boldsymbol{z}_t(t)=\hat{\boldsymbol{z}}_t(t,t), \qquad (2)$$

where the hatted variables are bivariate (i.e., two-time scales) forms of the corresponding variables in (1). In fact, it has been proved in, e.g., [10], that any solution of (1) generates a solution of (2).

Solving (2) when $u(t_2) = 0$, and linearizing around this point, the outputs linear in the input $u(t)$ can be obtained. With the solution denoted by $\hat{\boldsymbol{y}}^*(t_1)$, the outputs are given by $\boldsymbol{z}_t(t) = \hat{\boldsymbol{z}}_t(t,t) = \boldsymbol{d}^T\hat{\boldsymbol{y}}^*(t)$. Recalling that the outputs are two currents, we represent $\boldsymbol{z}_t(t)$ as two current sources $I_0(t)$ and $I_s(t)$, as shown in Fig. 2. Evidently, $I_0(t)$ is identical to

the one resulted by applying the macromodel in [4]. Although $I_0(t)$ and $I_s(t)$ are generally time-varying, they are 'fixed' in the sense that they are uniquely determined by the circuit (digital cell/block) itself, regardless of the power supply variation. Since $I_s(t)$ is only a small part of the total substrate noise, we can ignore the variation of $I_s(t)$ introduced by the fluctuation of power supply voltage without losing much accuracy, but the resulted macromodel will be much simpler. Doing so, the output vector $\boldsymbol{z}$ in (2) becomes a scalar z thereafter. In order to capture the variation of current power supply induced by the fluctuation, one also needs to solve the following *linear* MPDE:

$$\begin{aligned} \frac{\partial(\boldsymbol{C}(t_1)\hat{\boldsymbol{x}})}{\partial t_1} + \frac{\partial(\boldsymbol{C}(t_1)\hat{\boldsymbol{x}})}{\partial t_2} + \boldsymbol{G}(t_1)\hat{\boldsymbol{x}} = \boldsymbol{b}u(t_2) \\ \hat{z}(t_1,t_2) = \boldsymbol{d}^T\hat{\boldsymbol{x}}(t_1,t_2) \quad z(t) = \hat{z}(t,t), \end{aligned} \tag{3}$$

where vectors $\hat{\boldsymbol{x}}$, $\hat{z}$, and z are the small-signal versions of $\hat{\boldsymbol{y}}$, $\hat{z}_t$ and z_t, respectively; $\boldsymbol{C}(t_1) = (\partial\boldsymbol{q}(\hat{\boldsymbol{y}})/\partial\hat{\boldsymbol{y}})|_{\hat{\boldsymbol{y}}^*(t_1)}$ and $\boldsymbol{G}(t_1) = (\partial\boldsymbol{f}(\hat{\boldsymbol{y}})/\partial\hat{\boldsymbol{y}})|_{\hat{\boldsymbol{y}}^*(t_1)}$ are time-varying matrices. Eq. (3) reveals a linear relationship between the bivariate output $\hat{z}(t_1,t_2)$ and the small input signal $u(t_2)$. But this linear relationship is time-varying in the system time scale t_1. To obtain the time-varying transfer function from $u(t_2)$ to $\hat{z}(t_1,t_2)$, let us carry out the Laplace transform of (3) with respect to t_2, and collect observations at a total of $N+1$ instances $\{t_{1,n}\}_{n=0}^N$ with $t_{1,0}=0$, and $t_{1,N}=T_1$. In the following, we will consider the case where the system is periodic in t_1, and take T_1 to be one period of the system[2]. With s denoting the Laplace variable along the t_2 time axis, and capital symbols denoting transformed variables, it can be readily verified that the time-varying transfer function is given by:

$$\begin{aligned} \boldsymbol{H}(s) &= [H(t_{1,1},s),\ldots,H(t_{1,N},s)]^T \\ &= \boldsymbol{\mathcal{D}}^T[s\boldsymbol{\mathcal{C}} + \boldsymbol{\mathcal{G}} + \boldsymbol{\Delta}\boldsymbol{\mathcal{C}}]^{-1}\bar{\boldsymbol{B}}, \end{aligned} \tag{4}$$

such that $\boldsymbol{H}(s)U(s) = \hat{\boldsymbol{Z}}(s)$ with definition $\hat{\boldsymbol{Z}}(s) = [\hat{Z}^T(t_{1,1},s),\ldots,\hat{Z}^T(t_{1,N},s)]^T$. In establishing (4), we also used the following notation: $\bar{\boldsymbol{B}} = \mathbf{1}_{N,1}\otimes\boldsymbol{b}$, where $\mathbf{1_{N,1}}$ is a N by 1 all-one vector, and $\otimes$ denotes Kronecker product; $\boldsymbol{\mathcal{D}} = \boldsymbol{I}_N\otimes\boldsymbol{d}$, and $\boldsymbol{\Delta} = (\mathrm{dial}\{1/\delta_1,\ldots,1/\delta_N\}(\boldsymbol{I}_N - \boldsymbol{J}_N))\otimes\boldsymbol{I}_m$, where $\boldsymbol{I}_N$ stands for a N by N identity matrix, and $\boldsymbol{J}_N$ a N by N circulant matrix with first column $[0,1,0,\ldots,0]^T$, and first row $[0,\ldots,0,1]$; $mN\times mN$ matrices $\boldsymbol{\mathcal{C}}$ and $\boldsymbol{\mathcal{G}}$ consist of $C(t_{1,n})$ and $G(t_{1,n})$, $\forall n\in[1,N]$, respectively. With m and N being the number of system states (i.e., node voltages and branch currents) and the number of samples in t_1, respectively, the product mN could be very large. The latter then poses prohibitive computational complexity. Therefore, we apply model order reduction techniques on Eq. (4). Along the lines of [9], a model of reduced order $q < mN$ can be obtained by casting (4) into the standard form $\boldsymbol{H}(s) = \boldsymbol{\mathcal{D}}^T[\boldsymbol{I}_{mN} - s\boldsymbol{\mathcal{A}}]^{-1}\boldsymbol{\mathcal{R}}$ with definitions $\boldsymbol{\mathcal{A}} = -[\boldsymbol{\mathcal{G}}+\boldsymbol{\Delta}\boldsymbol{\mathcal{C}}]^{-1}\boldsymbol{\mathcal{C}}$ and $\boldsymbol{\mathcal{R}} = [\boldsymbol{\mathcal{G}}+\boldsymbol{\Delta}\boldsymbol{\mathcal{C}}]^{-1}\bar{\boldsymbol{B}}$, and applying Krylov subspace methods [7,11]. With block Arnoldi algorithm, the resultant qth order transfer function that approximates $\boldsymbol{H}(s)$ in (4) is given by [2]:

$$\boldsymbol{H}_q(s) = \boldsymbol{L}_q^T[\boldsymbol{I}_q - s\boldsymbol{T}_q]^{-1}\boldsymbol{R}_q, \tag{5}$$

where $\boldsymbol{L}_q = \boldsymbol{V}_q^T\boldsymbol{\mathcal{D}}$ is a $q\times N$ matrix, $\boldsymbol{T}_q$ is a $q\times q$ block-Hessenberg matrix, $\boldsymbol{R}_q = \boldsymbol{V}_q^T\boldsymbol{\mathcal{R}}$ is a $q\times 1$ vector, and $\boldsymbol{V}_q$ is the $mN\times q$ matrix consisting of the q orthogonal bases generated by applying block Arnoldi algorithm to $\boldsymbol{\mathcal{A}}$ and $\boldsymbol{\mathcal{R}}$.

[2]For more general cases, and frequency domain treatments, the reader is referred to [9].

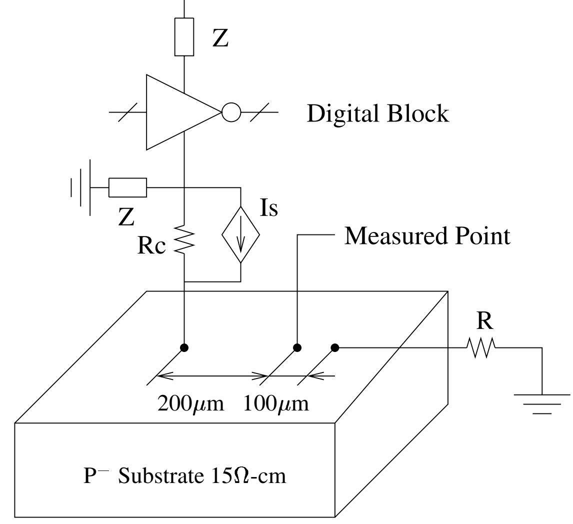

Fig. 3. Schematic diagram for full-chip substrate noise analysis.

Transforming (5) into time domain, we have the following system representation:

$$-\boldsymbol{T}_q\frac{d\boldsymbol{x}}{dt} + \boldsymbol{x} = \boldsymbol{R}_q u(t) \quad z(t) = \boldsymbol{l}_q(t)\boldsymbol{x}(t), \tag{6}$$

where $\boldsymbol{x}$ is a vector of size q, $z(t)$ is the output, and $\boldsymbol{l}_q(t)$ is the $q\times 1$ time-varying vector that relates the system (states) to the output. To link $\boldsymbol{l}_q(t)$ with the $q\times N$ matrix $\boldsymbol{L}_q$ in (5), we notice that the nth column of $\boldsymbol{L}_q$ is nothing but $\boldsymbol{l}_q(t_{1,n})$, $\forall n\in[1,N]$. Eq. (6) corresponds to an ODE system, which translates the noise in power supply grids $u(t)$ to its corresponding current change $z(t)$. As a supplement to the current $I_0(t)$, we denote $z(t)$ as $\Delta I(t)$.

As shown in Fig. 2, the resultant LTV macromodel consists of three major components: a current source $I_0(t)$, a ODE system generating the current $\Delta I(t)$ and a current source I_s injecting current into substrate. The former ($I_0(t)$) is the current that the digital cell consistently draws, assuming perfect power supply and ground. The ODE system in our macromodel turns out to be LTV, which acts as a current source and the current $\Delta I(t)$ is determined by the voltages at node 2 and node 3, i.e., voltage variations at ground and power supply, respectively. Benefited from applying model reduction techniques, the LTV ODE system contains only $1\sim 10$ nodes, which corresponds to a marked reduction in comparison with hundreds of nodes in the original digital cell. Notice that the ODE system parameters captured in $\boldsymbol{T}_q$, $\boldsymbol{R}_q$, and $\boldsymbol{L}_q$ do not depend on the voltage variation, and can thus be computed off-line, and stored together with $I_0(t)$ and $I_s(t)$ in a cell library. The proposed macromodel enjoys high-accuracy and low-complexity, when included in a complete substrate noise analysis circuit that contains the package model, on-chip power networks, and substrate model, and is thus readily applicable to large scale circuits.

IV. Simulation Results

To demonstrate the performance of our macromodel, we apply the extraction method to a full-chip substrate noise analysis example. As depicted in Fig. 3, the system consists of

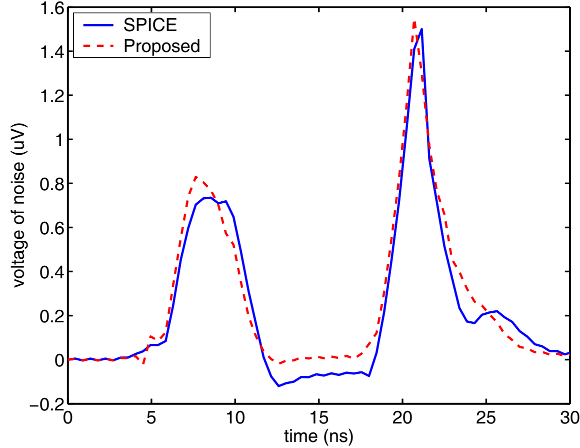

Fig. 4. The time-domain comparison of substrate noise induced by an 100-inverter-block using SPICE MOSFET model and our proposed macromodel.

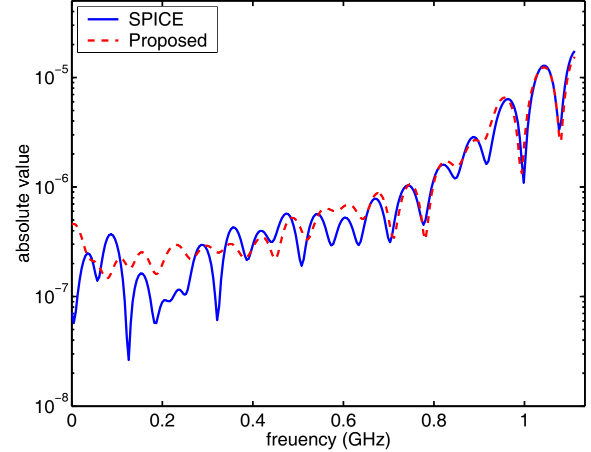

Fig. 5. The frequency-domain omparison of substrate noise induced by an 100-inverter-block using SPICE MOSFET model and our proposed macromodel.

a power supply network, package, a digital block, and a substrate. The digital block is constructed by stacking a total of 50 inverter chains, each containing 2 inverters. The logic input of the digital block has a period 30ns. In our simulations, the package and power supply network are modeled as an impedance $Z = 2 + j2 \times 10^{-9}\Omega$ in Fig. 3; the resistance of ground contact is $R_c = 2\Omega$; and the resistance of ground bias network is $R = 2\Omega$. The substrate is P^- type with dimension $width \times length \times depth = 1000 \times 1000 \times 300\mu m^3$, and a sheet resistance $15\Omega{-}cm$. Discretisizing the substrate into $50 \times 50 \times 50\mu m^3$ cubes, we model it as a resistive mesh. The digital block is located $200\mu m$ from the measuring point, which is $100\mu m$ from the ground bias point.

For the digital block, the MOSFET is simulated using Schichman-Hodges model with $\mu_n C_{ox} \frac{W}{L} = 1.6 \times 10^{-4}$A/V^2 for both NMOS and PMOS, load $C = 0.5$pF (see e.g., [5]). Although not mandatory, the Schichman-Hodges model (instead of more comprehensive models, such as BSIM3) is adopted here for simplicity. In order to verify the capability of our macromodel in reflecting the power supply variation, we use a power supply voltage 10% below the ideal value of 2V.

We choose uniform step size of $t_{1,n} = 450n$ ps, $\forall n \in [0, N]$, and the ODE system order $q = 2$. The latter implies a computational complexity similar to the macromodel in [4]. For comparison purpose, we use both SPICE-level description and our macromodel extraction to represent the digital block, and carry out the substrate noise analysis. With SPICE-level description, it takes 291.3s; whereas with our macromodel, it only takes 1.81s, which is 160 times faster. As evident in Fig. 4, the discrepancy between their peak values is 0.048μV, which corresponds to an error of 3.21%. It is also worth mentioning that the resultant noise using our macromodel closely matches the true not only in peak value, but also in shape, which is corroborated by the comparison in frequency domain by taking Fourier Transform of their corresponding results, as depicted in Fig. 5.

V. Conclusions

Efficient and accurate computation of noise injection from the digital circuits consists of a major challenge in substrate noise analysis. In this paper, using TVP and model reduction techniques, we established a macromodel for noise injection computation with low complexity and high accuracy. A key attraction of this macromodel is the inclusion of three major noise mechanisms. Thanks to its low complexity, the macromodel enables system-level noise analysis, even in large-scale circuits. The accuracy renders our digital cell macromodel interact with power grid voltage variations just as the original cell does, thus provides reliable results even with noisy power supply/ground. As we presented in section IV, our proposed model significantly speeds up the computation (160 times faster) while still offering excellent accuracy (3.21% peak noise error).

VI. Acknowledgment

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