Substrate Noise Analysis and Experimental Verification for the Efficient Noise Prediction of a Digital PLL

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***Abstract*— Substrate noise is a major impediment to mixed-signal integration. This paper describes a CAD tool that can be used at any stage of the design cycle to estimate the substrate noise generated by large digital circuits. The results have been verified with substrate noise measurements on a 480 MHz digital PLL implemented in a 90 nm CMOS process on a high resistivity substrate.** **Keywords: substrate noise, mixed-signal simulation, computer aided design**

I. Introduction

With the increasing levels of integration in ICs today and ever-increasing digital circuit speeds, the problem of substrate noise is becoming more and more pronounced. The performance of sensitive analog circuits can be severely degraded. The effect of substrate noise on the circuits within an IC is typically observed during the testing phase only after the chip has been fabricated. Determination of substrate noise coupling during the design phase would be extremely beneficial to circuit designers who can incorporate the effect of the noise and re-design accordingly before fabrication. This would reduce the turn around time for circuits and increase the yield of working chips.

We have developed a substrate noise analysis tool (SNAT) that provides information on the substrate noise performance of the input design. There has been much work on efficiently modeling noise generation in digital circuits using noise macromodels [1][2]; however, because these approaches require a circuit layout, they are limited to use as a final verification tool. Early in the design cycle, a layout may not be available; thus, a substrate noise estimate cannot be determined. SNAT works with a multitude of input description coarseness that renders it appropriate for use in any stage of the design cycle. A comparison to measured data of a test circuit, a digital phase locked loop (DPLL), is also presented to verify the accuracy of the simulation.

II. Substrate Noise Simulation

To simulate a digital circuit for substrate noise, additional parasitic elements that account for the substrate have to be added. On average, four passive elements are added for each device corresponding to four additional nodes. A for a microprocessor with a hundred million transistors, almost four hundred million additional nodes must be simulated to account for the coupling to the substrate. Even more elements would have to be added to model propagation within the substrate. The large number of nodes results in prohibitively large simulation times. Long simulation times can be tolerated for final verification. If, however, an estimate of the substrate noise is all that is required, a simulation time of several days is excessive.

To speedup simulation times, macromodeling approaches are typically used. The purpose is to extract the noise behavior of a system into equivalent linear macromodels, which are then simulated. SNAT employs macromodels to speed up the simulation.

III. SNAT: Substrate Noise Analysis Tool

SNAT requires two inputs: a circuit description and a technology description. With an event model for each node in the circuit, a noise signature is constructed. This noise signature together with the substrate model and power grid is used to compute the substrate noise. The outputs are a time domain representation and noise spectrum. Figure 1 shows the flow of the tool.

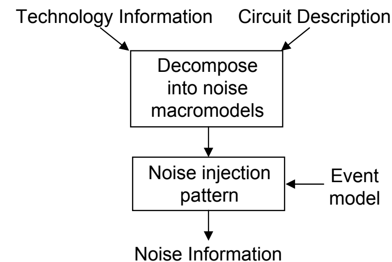
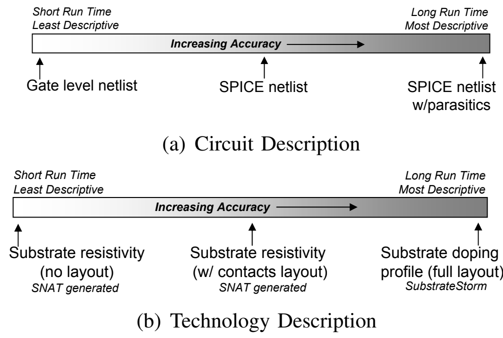


Fig. 1. Flow of Substrate Noise Analysis Tool.

A. Granularity Level

SNAT works with a spectrum of information for both the circuit description and technology description. This is detailed in Figure 2. To generate the noise signature, the tool requires information on the circuit. At a minimum, a gate-level description along with BSIM models can be used to generate the signature. At this level, no layout parasitics are considered in constructing the signature. The effect of parasitics can be significant as will be shown in Section IV-A.2. The effect of resistance in the power supply grid and interconnect capacitance will affect the substrate noise generated [3]; however, this information is not available at the gate-level. A gate-level simulation is performed to extract the event model. As the user provides more information to the tool, accuracy increases at



(a) Circuit Description

(b) Technology Description

Fig. 2. Input Description Granularity Levels.

the expense of simulation efficiency. Providing a more detailed circuit description such as an extracted netlist from layout increases the number of elements that are simulated and thus the run time; however, the accuracy increases. SNAT's ability to work with a variety of input descriptions is referred to as the granularity level.

Multiple granularity levels are also present on the substrate modeling side. To properly model the high resistivity substrate that is typically used in mixed-signal systems, a full extraction of the layout of the circuit with the substrate doping profile has to be generated. Cadence's SubstrateStorm tool was used for the detailed extraction [4].

Depending on the size of the circuit, the generated netlist can be massive since all propagation mechanisms are accounted for. For the DPLL presented in this work, the complete substrate model includes approximately 1.6 million elements to model the substrate. Using such a complete substrate model results in the most accurate result at the expense of a long run time. Simulation times are on the order of several days.

If the technology is not well characterized, substrate doping profiles might not be available. At the next lowest granularity level, SNAT generates a coarser substrate model knowing only the underlying substrate resistivity. It has been observed both for the DPLL and other test circuits that the capacitive effects of wells and other junctions need only be considered at lower frequencies. At higher frequencies, the resistive nature of the substrate dominates. This observation is the basis of the coarser substrate model. Figure 3 shows a comparison of the two models.

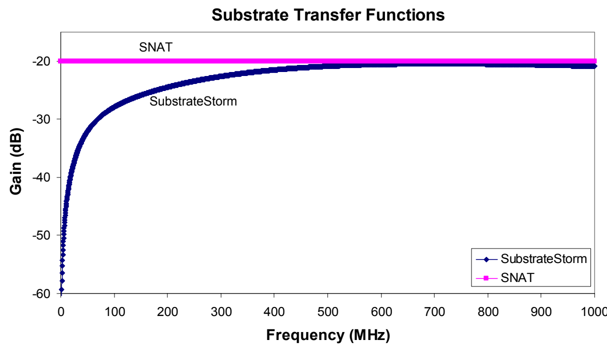


Fig. 3. Substrate model generated by SubstrateStorm and SNAT.

Based on the layout, an equivalent resistive mesh is generated to model the substrate. The number of nodes is greatly reduced speeding up run time. For the DPLL, the coarser substrate netlist consists of 134 resistors. As mentioned earlier, the tool can yield an approximation for the substrate noise levels with no circuit layout. To generate the substrate model for such a case, an estimate of the circuit area must be provided from which a resistive substrate model is generated.

A comparison of simulations done on several granularity levels with that of measured data on a DPLL is provided in Section IV.

B. Macromodel

SNAT generates equivalent macromodels for each gate. The macromodels are then connected as specified by the circuit netlist. A schematic of the macromodel is shown in Figure 4. This macromodel is based on that proposed in [5] with the addition of voltage sources to represent the capacitive sources of noise such as interconnect.

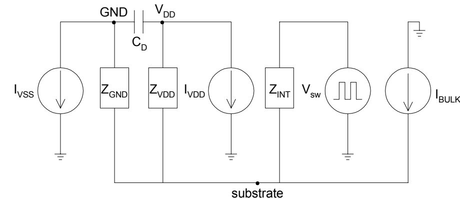


Fig. 4. Noise Macromodel.

The current sources I_{VDD} and I_{VSS} represent the noise in the power and ground lines respectively. I_{bulk} represents current flowing directly into the substrate such as that from impact ionization. The shape of the current signature depends on the input rise time and on the output load if an output switching event occurs. The dependency on these two parameters is specific to each cell and is extracted during a one-time characterization step. This step need only be performed once per technology library and takes approximately 18 hours on a dual processor 1.2 GHz SunFire 280r machine.

The tool requires an event model for each node to generate the noise signature. If a gate-level netlist is available, a gate-level simulation is performed. Such a simulation takes less than a minute. If a gate-level netlist is not available, a Nanosim simulation can be used to generate the event model instead of SPICE which will have considerably longer simulation times [6]. To generate the macromodel current signature, the event model is convolved with the cell current signature. A substrate model is then incorporated between the macromodel nodes labeled substrate in Figure 4. A model for the power grid can also be incorporated.

The macromodel-generated noise is accurate to within 5% of SPICE. Figure 5 shows the noise generated by a noise generator consisting of 1200 gates in a 90 nm technology.

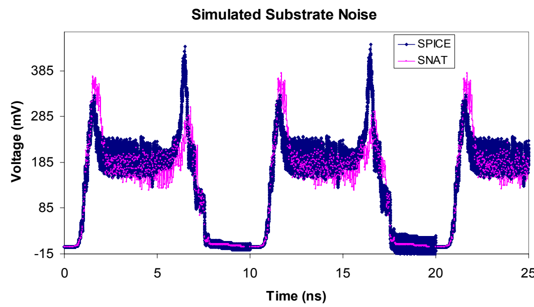


Fig. 5. Comparison of noise from SPICE and SNAT.

IV. Measurement Comparison

To verify the results of the tool, the simulations results were compared to measurements on a test chip. The test chip is a DPLL fabricated in Texas Instruments' 90 nm CMOS technology. The DPLL has roughly 10K-20K gates. The chip was fitted with four p+ substrate contacts surrounding the system core that acted as substrate noise sensors (refer to Figure 6). The DPLL was run with a reference clock frequency of 80 MHz resulting in an output frequency of 480 MHz. The noise spectrum was measured using a spectrum analyzer. Due to measurement constraints, a time domain measurement could not be obtained.

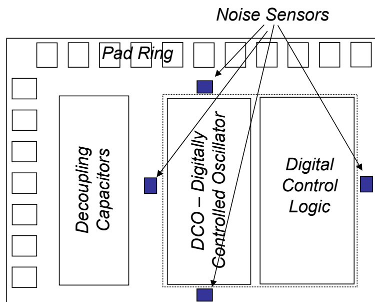


Fig. 6. Block Diagram of DPLL.

A. Noise Signature Generation

SNAT was run with the same test conditions as the measurements. A model for the package and experimental setup was also included.

1) Event Model : Simulations over 10 different granularity levels were performed to determine the effect of each step in granularity on accuracy. Table I describes the inputs at each granularity level. Figure 7 shows the noise spectrum generated for a granularity level of 9. Table III shows the accuracy in predicting each tone of the noise spectrum for all the granularity levels. The simulated spectrum correlates very closely with that of the measured data with an error less than 15% for all tones with the exception of 80 MHz and 480 MHz, which show substantially higher error. This is discussed further in the next subsection.

Simulations were run with two different event models. Both were generated from Nanosim; however, the second model was run with the accuracy level reduced to emulate that of a gate-level simulation since a gate-level netlist was not available. Using the Nanosim2 event model results in a doubling of the error in the RMS voltage. Figure 8 shows the time domain voltages for three granularity levels. The run times for each step in the analysis is summarized in Table II.

TABLE I
Granularity Level Description

Level	*Event Model*	*Parasitics?*	*Substrate*
1	Nanosim2	no	SNAT+no layout
2	Nanosim2	no	SNAT+layout
3	Nanosim2	yes	SNAT+layout
4	Nanosim2	no	SubstrateStorm
5	Nanosim2	yes	SubstrateStorm
6	Nanosim1	no	SNAT+no layout
7	Nanosim1	no	SNAT+layout
8	Nanosim1	yes	SNAT+layout
9	Nanosim1	no	SubstrateStorm
10	Nanosim1	yes	SubstrateStorm

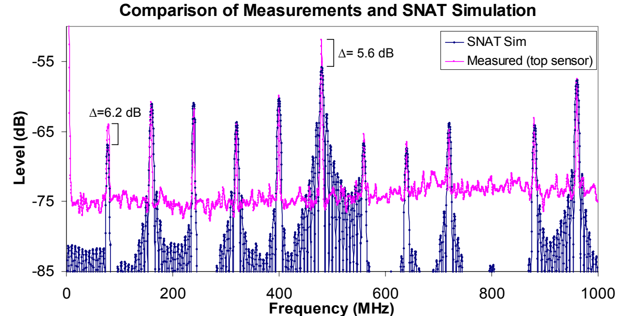


Fig. 7. Measured and simulated noise spectrum at top sensor.

TABLE II
Run times of each step

Step	*Run Time*
Library Characterization	18 hrs
Nanosim1	56 min
Nanosim2	7.5 min
SubstrateStorm	51 hrs
SNAT+layout	14.5 min
SNAT+no layout	5 sec

2) Effect of Parasitics: The increased error in the 80 MHz and 480 MHz components is a result of an incomplete parasitics model. Both the reference clock and the output clock are connected externally; thus, the effect of pad parasitics need to be incorporated. The pad capacitance to substrate and capacitance from ESD structures were included in the granularity level 10 netlist. The incorporation of these parasitics reduces the error of the two tones significantly resulting in only 11.7% error in the RMS voltage.

B. Substrate Model

Simulation of the SubstrateStorm-generated substrate netlist together with the circuit netlist incorporating parasitics (granularity level 10) yields the least error when compared to measurements. However, the huge size of the substrate netlist greatly increased the simulation time. Using the coarser model

TABLE III

% ERROR OF EACH TONE FOR DIFFERENT GRANULARITY LEVELS

f(MHz)	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*
80	29.1	104.5	55	28.6	184.1	39.9	121.8	51.2	22.6	208.1
160	3.8	3.8	45.3	45.3	117.9	2.4	2.4	46	46	115.1
240	8.1	8.1	39.4	39.4	141.1	0.3	0.3	34.3	34.3	161.4
320	4.5	4.5	27.2	27.2	189.8	12.4	12.4	33.2	33.2	165.9
400	4.1	4.1	12.5	12.5	248.4	18.5	18.5	0.4	0.4	296.7
480	11.7	57.8	12.1	41.2	462	23.8	55.9	10.8	39.4	455.2
560	8.4	8.4	15	15	238.3	1.4	1.4	5.9	5.9	274.7
640	11.5	11.5	5.4	5.4	319.4	33.1	33.1	36.8	36.8	151.5
720	12.3	12.3	16.8	16.8	231.2	7	7	11.7	11.7	251
880	15	15	7	7	325.8	18	18	9.8	9.8	337.2
960	1.8	1.8	7	7	270.3	3.9	3.9	12.2	12.2	249.5

generated by SNAT, simulation time of the substrate can be cut from 51 hours to less than 15 minutes. This, however, can result in reduced accuracy. For the DPLL, the error in predicting the lower frequency components increases since the attenuation provided by wells is neglected; however, the error in the rms voltage is not significantly affected as the the main tone (480 MHz) largely sees the resistive effect of the substrate, which is adequately modeled using the coarse substrate model. Figure 8 shows the effect of the coarser substrate model in the time domain.

With no layout information, the error increases significantly since both the capacitive attenuation of the wells is ignored, and the resistive attenuation of the substrate is modeled less accurately. The information can still be useful as it gives an idea of the order for magnitude of the noise.

The results shown above are for measurements from the top sensor. Simulations and measurements were also compared for the other sensors. The same trends in accuracy over granularity level are also observed. Both the SubstrateStorm-generated substrate model and the SNAT-generated model from layout correctly encapsulate the sensor location dependency of the received substrate noise. However, the SNAT-generated model with no layout does not incorporate the location dependency.

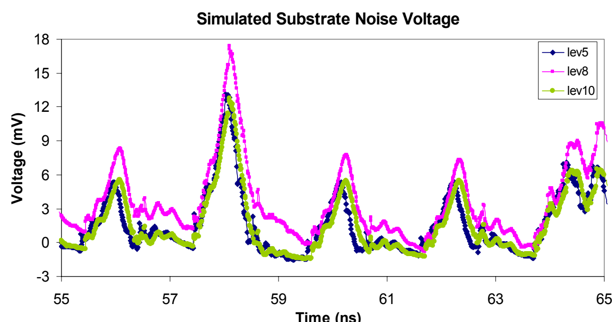


Fig. 8. Comparison over granularity level in time domain.

V. CONCLUSIONS

We have presented a tool that can be used to predict substrate noise generation of any digital system. Simulation times are greatly reduced by using a macromodel approach. Further reduction in run time can be achieved at the expense of accuracy. The tool can be used to preliminarily evaluate the substrate noise performance to doing a full chip final verification where excellent correlation (11.7% error) to measured data is observed.

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