Substrate Noise Analysis and Experimental Verification for the Efficient Noise Prediction of a Digital PLL

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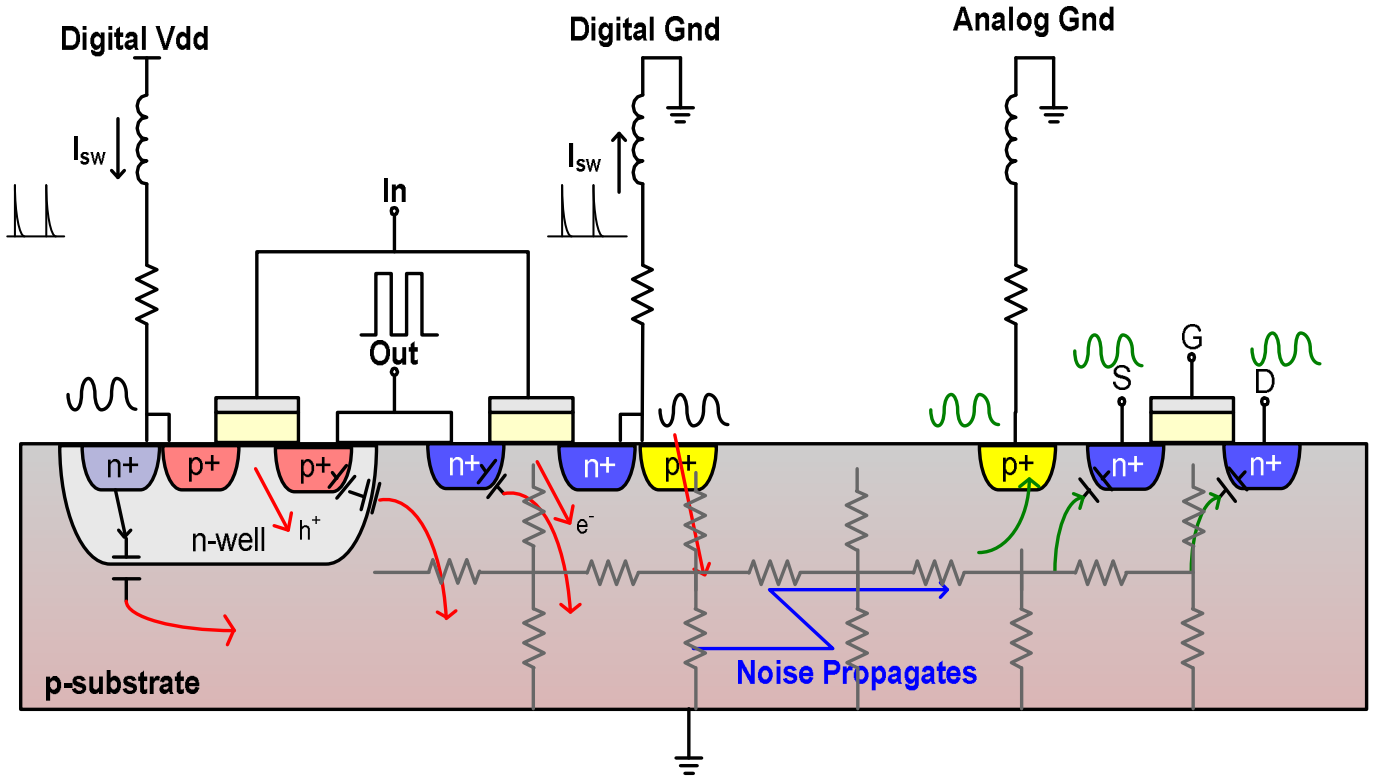
Outline

- Background
- Conventional substrate noise simulation
- Noise macromodels
- Substrate Noise Analysis Tool (SNAT)
  - Overview
  - Measurement comparison
- Summary

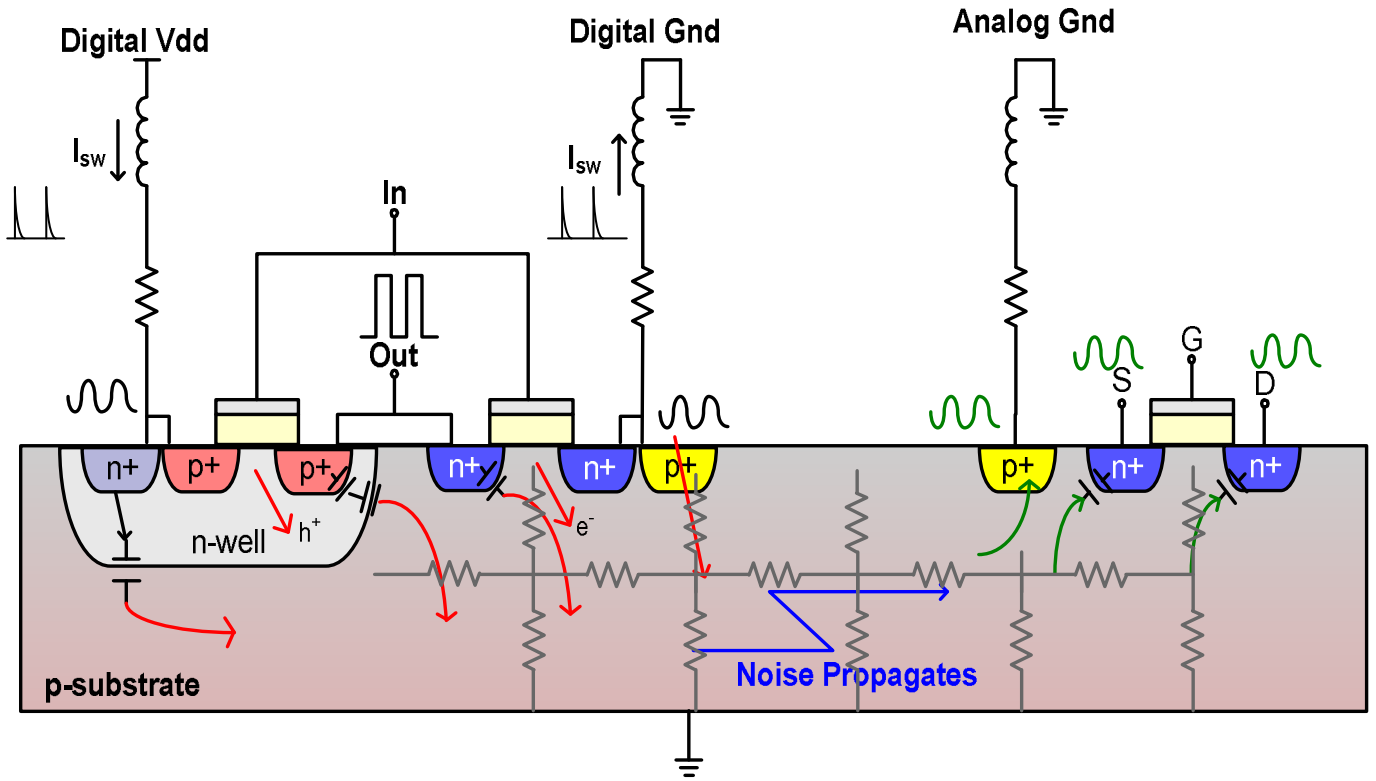
Background: Noise Generation

- Digital circuits inject noise into substrate during high speed switching
- Noise Sources:
  - Vdd/gnd bounce
  - Switching inputs/outputs
  - Bulk current



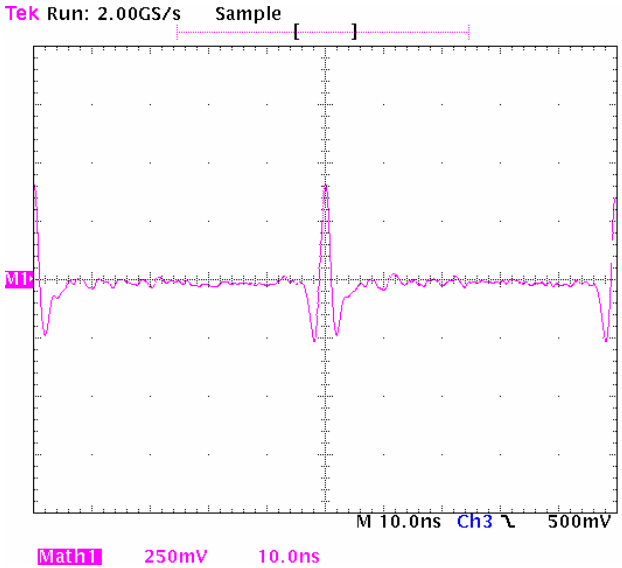
Background: Noise Generation

- Noise travels to analog section via conductive substrate
- Effect on analog circuits: power/gnd noise, pick-up through depletion capacitances, vary bias through V_T fluctuation, backgate effect

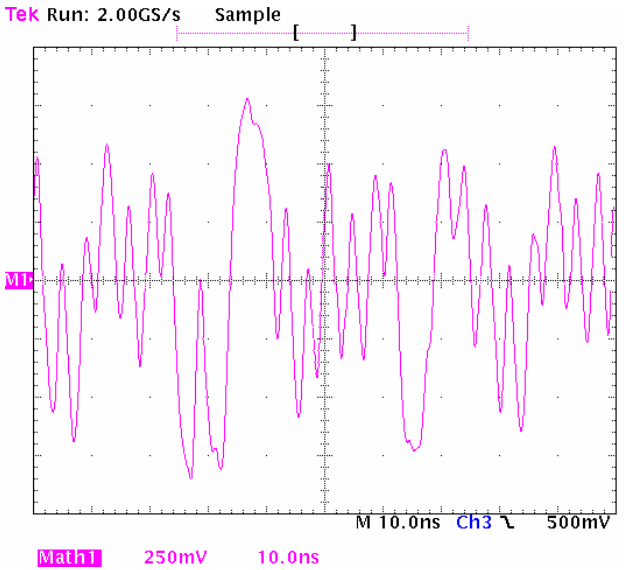


Motivation

- UWB transceiver chip
  - TSMC 0.18 μm mixed mode process



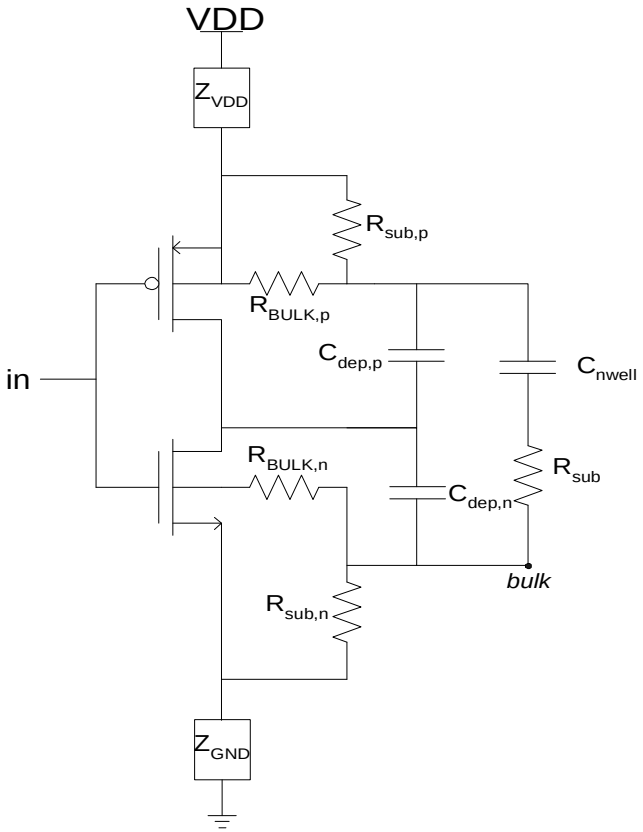
Digital OFF



Digital ON

Figures courtesy F. Lee

Simulation with Substrate Model



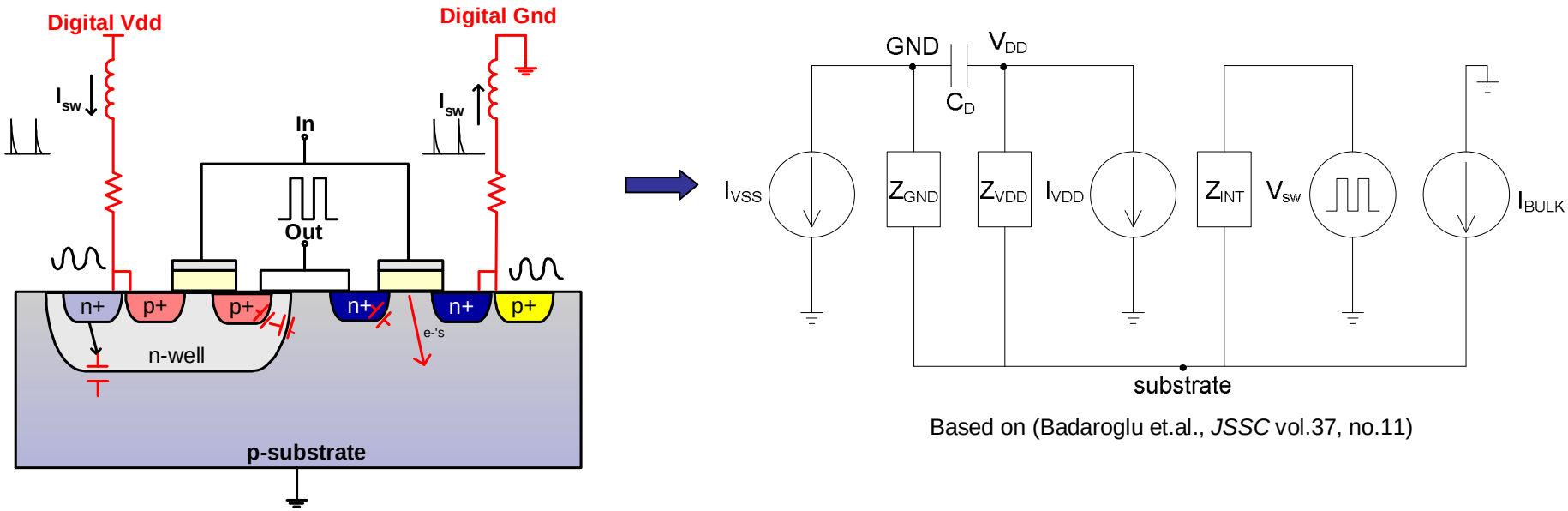
- Model for single inverter
- Substrate model (add'l 8 nodes):
  - NMOS: 3 elements
  - PMOS: 5 elements
- Example: Intel Pentium® 4 (Prescott) Microprocessor has 125 million transistors
  - ➢ ~ 500 million nodes for substrate! (excluding substrate model)

Model needs to be simplified to yield reasonable simulation times

➢ *Solution: Extract noise behavior into equivalent macromodel*

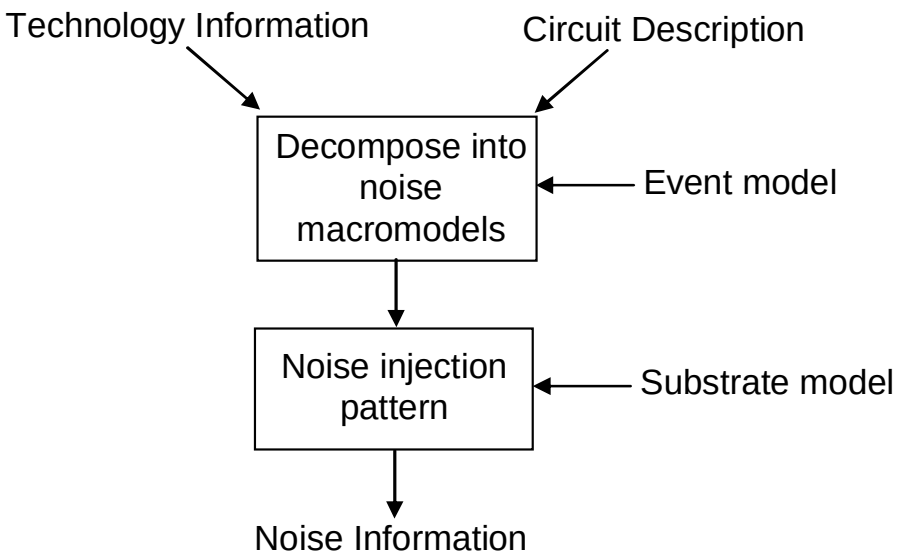
Noise Macromodel Derivation

- Represent each noise source with equivalent source in macromodel
  - Represent V_{dd}/gnd bounce with I_{VDD} and I_{VSS} and Z_{VDD} and Z_{GND}
  - Represent switching inputs/outputs with V_{sw} and Z_{INT}
  - Represent bulk current with I_{BULK}
- C_D represents circuit decoupling capacitance



Based on (Badaroglu et.al., *JSSC* vol.37, no.11)

Substrate Noise Analysis Tool



- Inputs
  - Circuit description: netlist or gate level description
  - Technology information: as detailed as substrate doping profiles, as coarse as substrate resistivity and type
- Outputs:
  - Time domain substrate noise
  - Noise spectrum

Granularity Level

- Inputs: Circuit Description

Short Run Time
Least Descriptive

Increasing Accuracy →

Long Run Time
Most Descriptive

Gate level netlist

```
module adder(A,B,Cin,S,Cout);
  input A, B, Cin;  output S, Cout;
  assign S = A ^ B ^ Cin;
  assign Cout = (A & B) | (A & Cin)
                | (B & Cin);
endmodule
```

SPICE netlist

```
MN0 out in vss bulk nch
+ L=0.18e-6 W=1.58e-6
+ AD=426.6e-15 AS=592.5e-15
+ PD=2.12e-6 PS=3.12E-6 M=4
…
```

SPICE netlist w/parasitics

```
MN0 out in vss bulk nch
+ L=0.18e-6 W=1.58e-6
+ AD=426.6e-15 AS=592.5e-15
+ PD=2.12e-6 PS=3.12E-6 M=4

Cint1 out bulk 0.5f
…
```

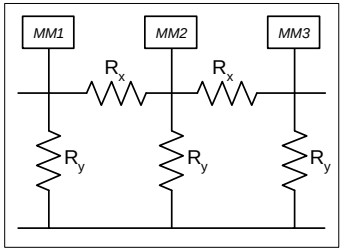
- Inputs: Technology Description

Short Run Time
Least Descriptive

Increasing Accuracy →

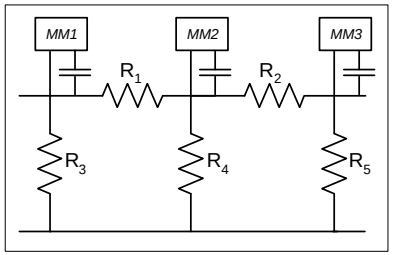
Long Run Time
Most Descriptive

Substrate resistivity
(no layout information)



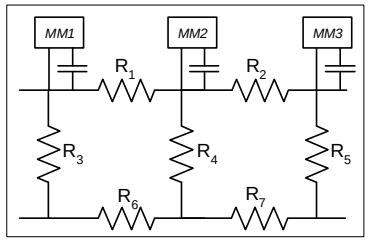
substrate model
SNAT Generated

Substrate resistivity
(w/ contacts layout)



substrate model
SNAT Generated

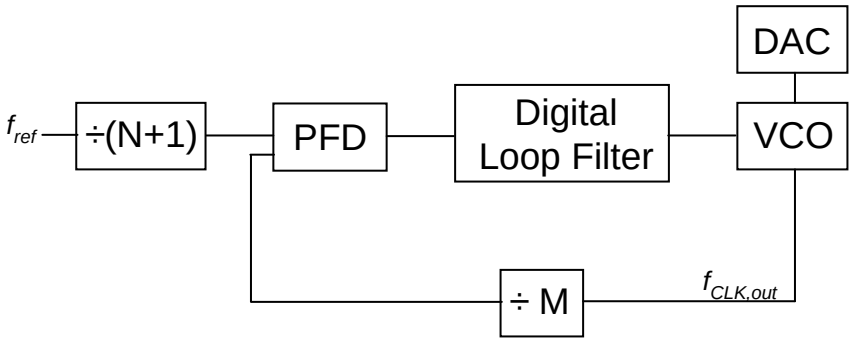
Substrate doping
profile (full layout)



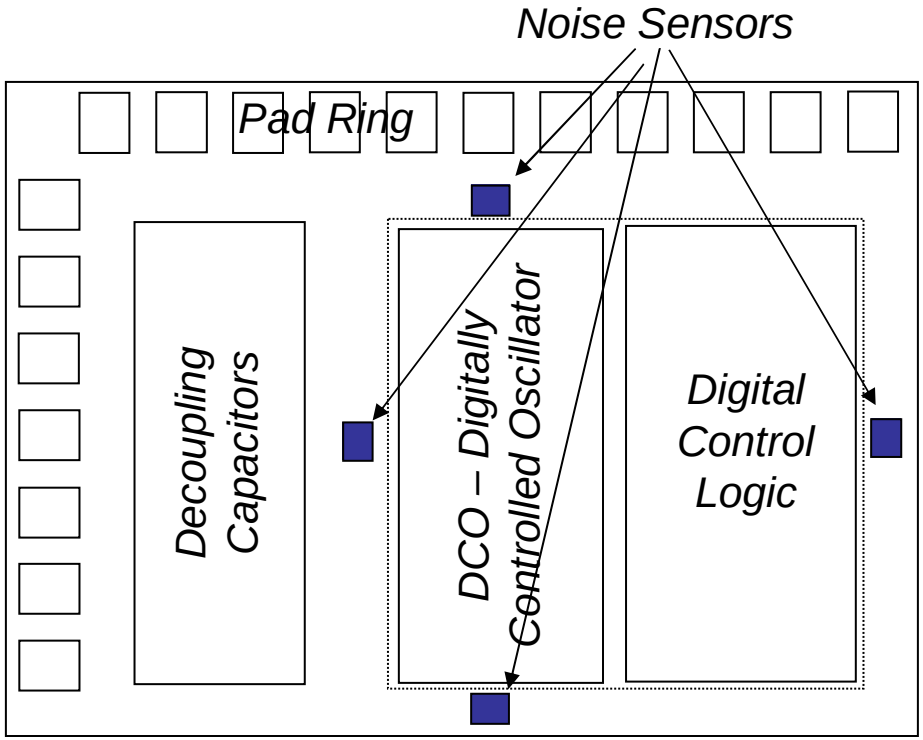
substrate model
SubstrateStorm Generated

Measurement Comparison

- Test circuit: Digital PLL (~ 15K gates)
  - Designed in TI's 90nm technology
  - f_{clkref} = 80 MHz, f_{out} = 480 MHz
  - Substrate noise sensors added around DPLL

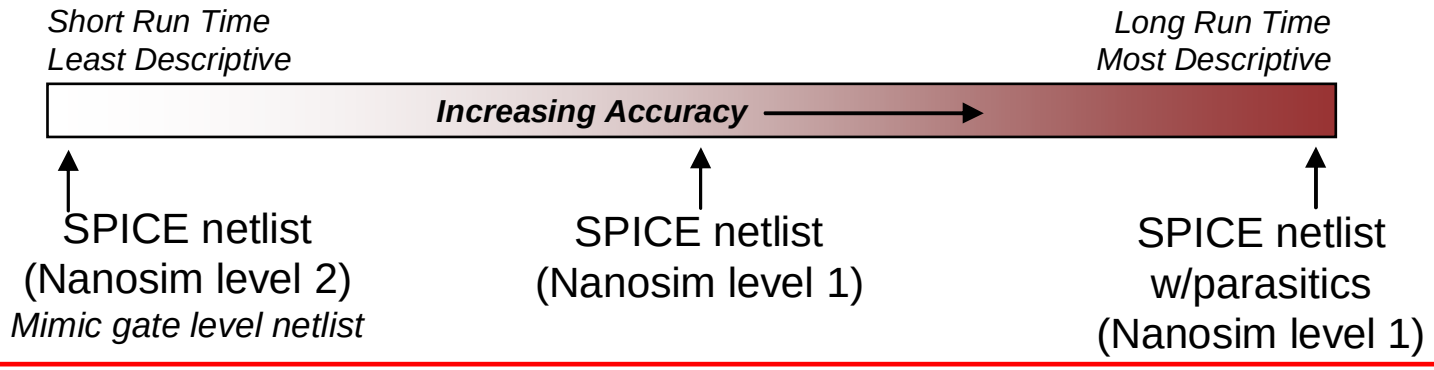


Digital PLL Block Diagram



Granularity Levels

- Inputs: Circuit Description



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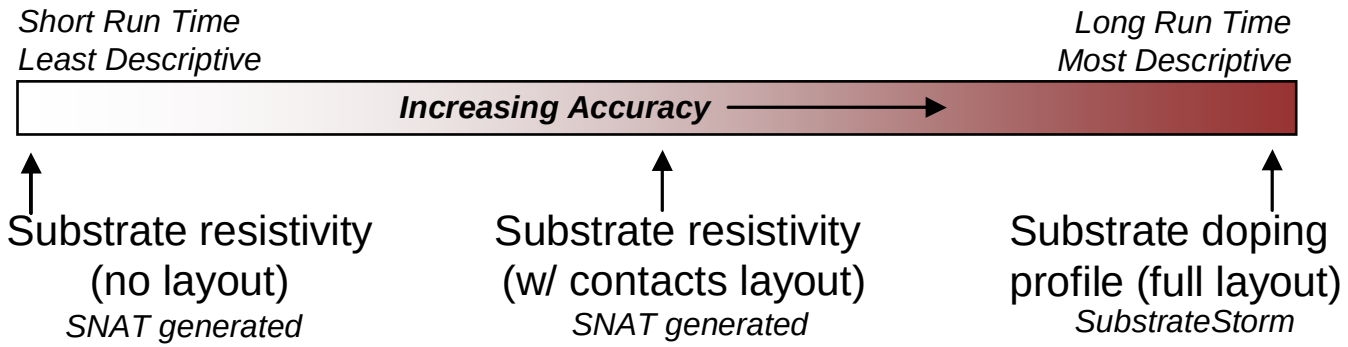
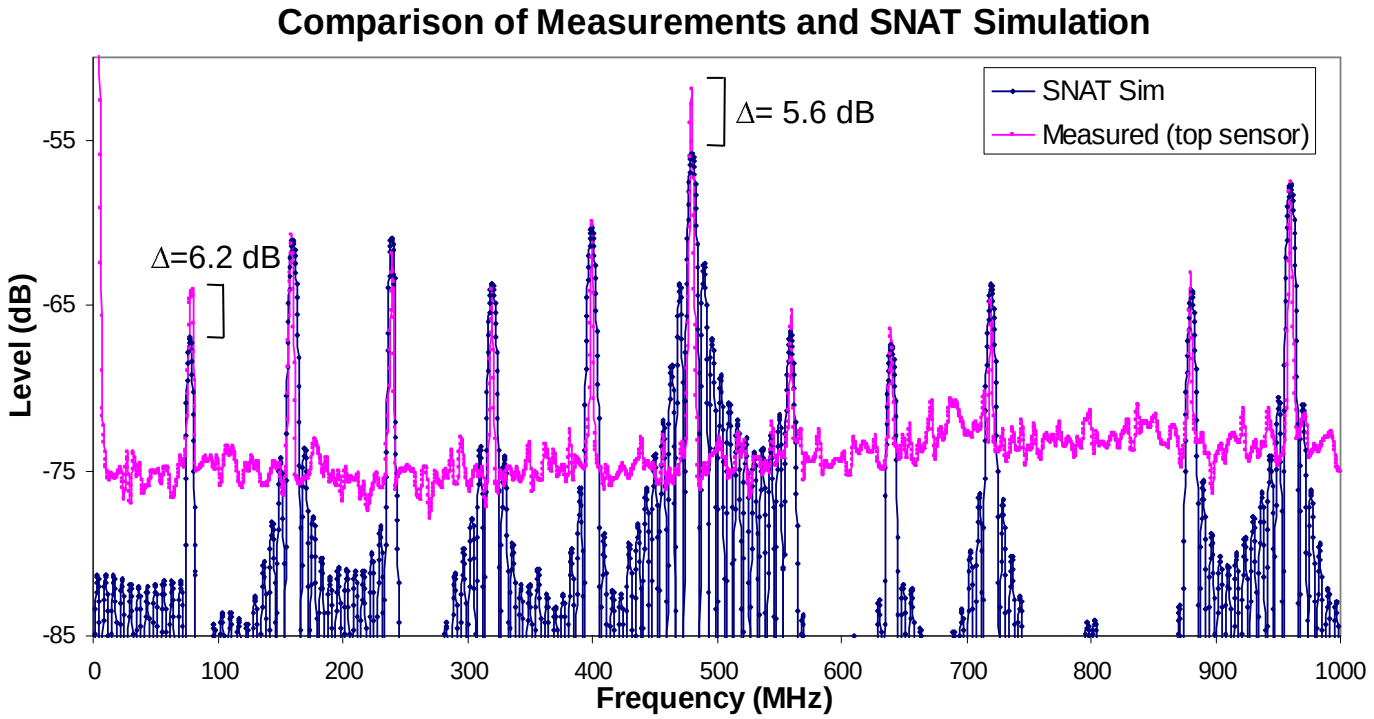


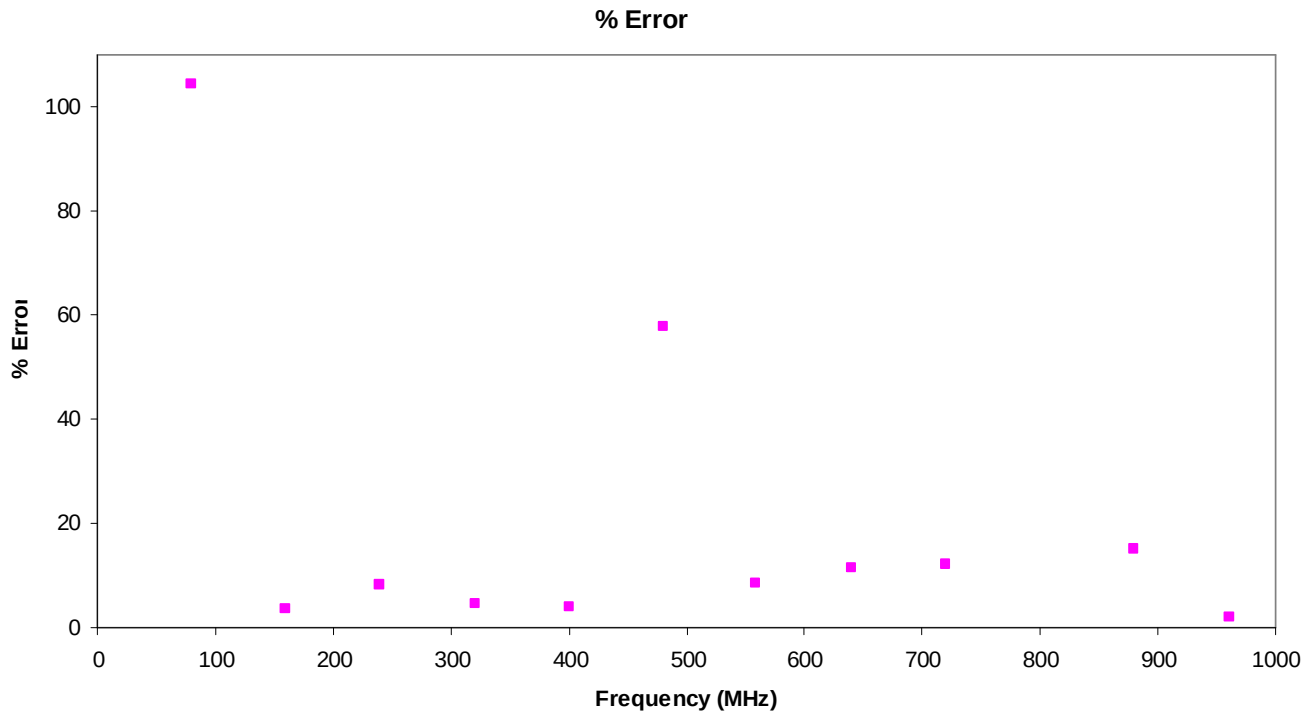
Noise Spectrum

- Top sensor
- SNAT Simulation:
  - Technology Description: SubstrateStorm generated model
    - ~ 30 minutes to generate netlist
    - ~ 51 hours to simulate
  - Circuit Description: SPICE netlist (no parasitics)
    - ~ 6 minutes



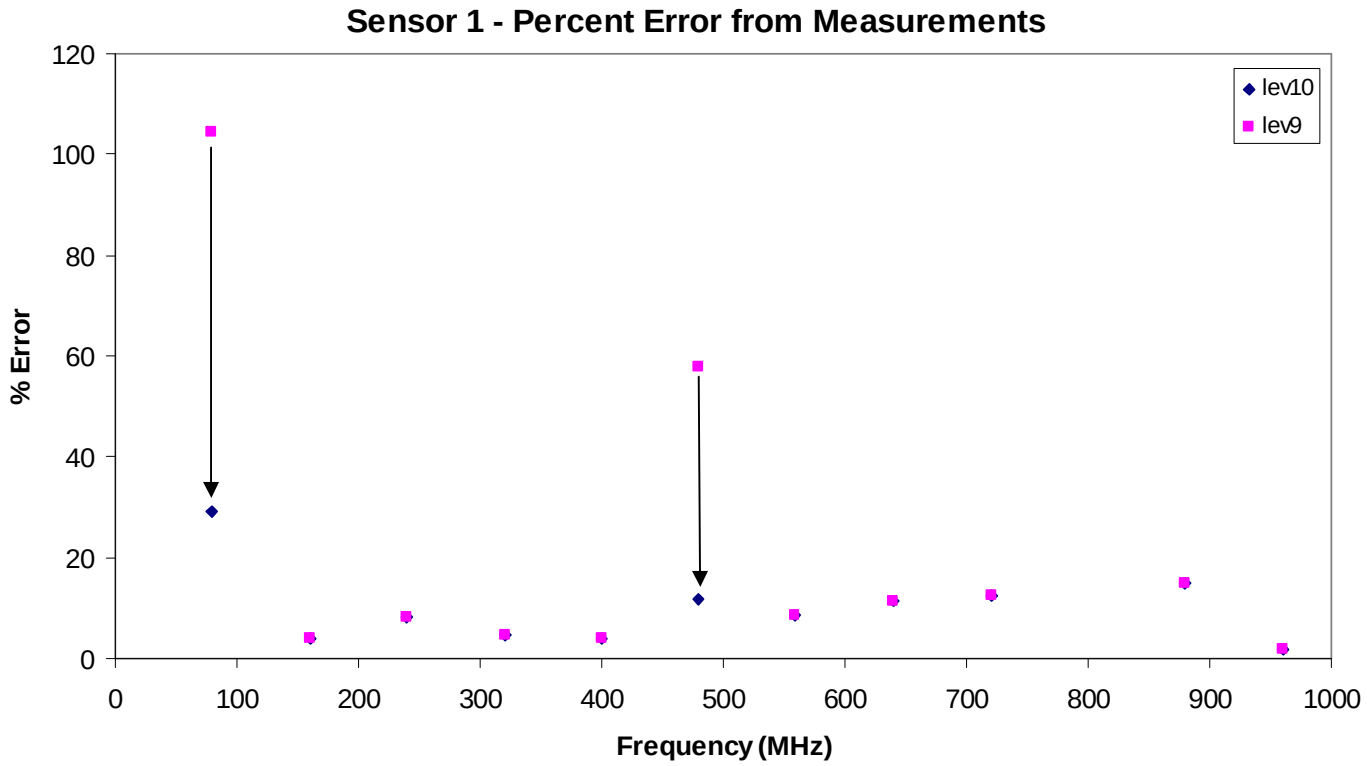
Error

- Most error at 80 MHz (f_{clkref}) and 480 MHz (f_{out})



Parasitics

- Incorporate effect of pad parasitics – REFCLK pad and CLKOUT pad
  - Pad to substrate capacitance
  - Capacitance to substrate of ESD structures
- Highest accuracy level – 11.7% error in RMS voltage



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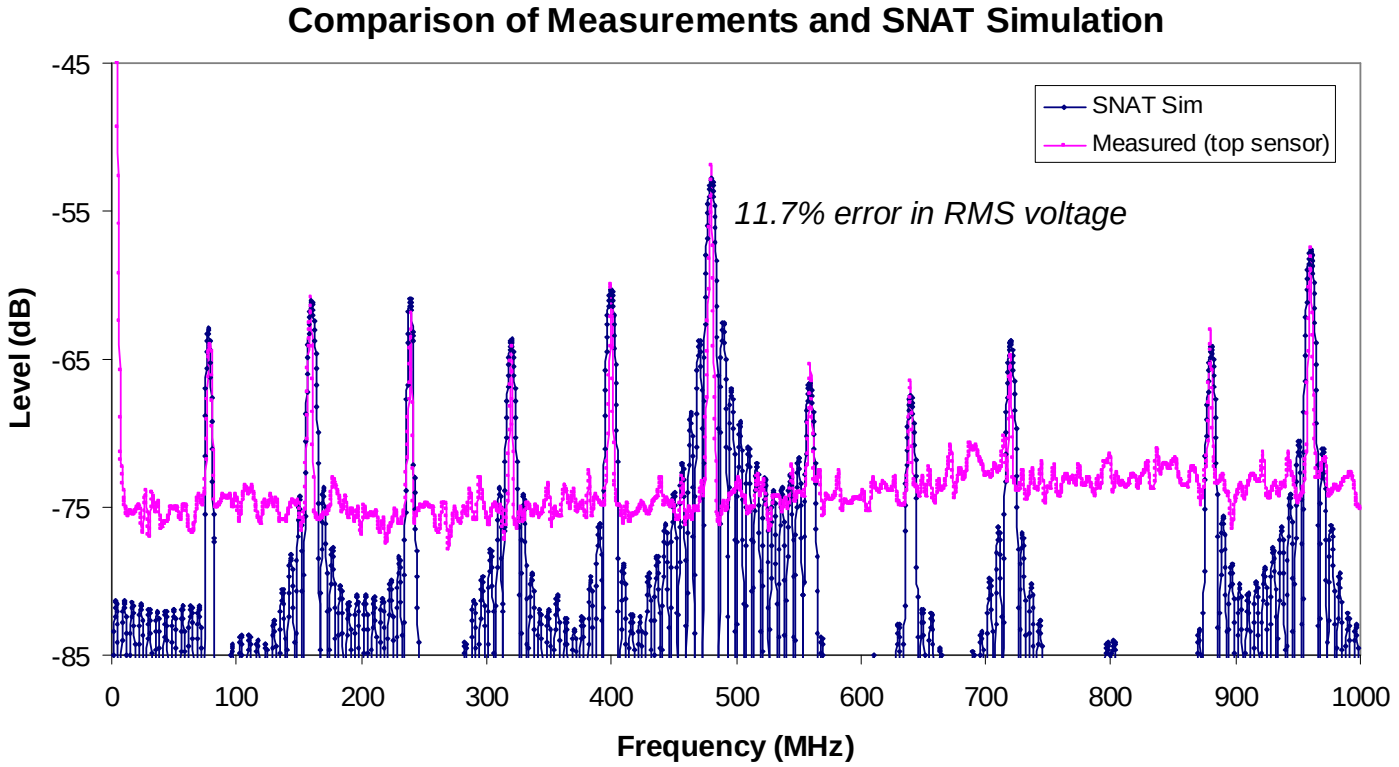
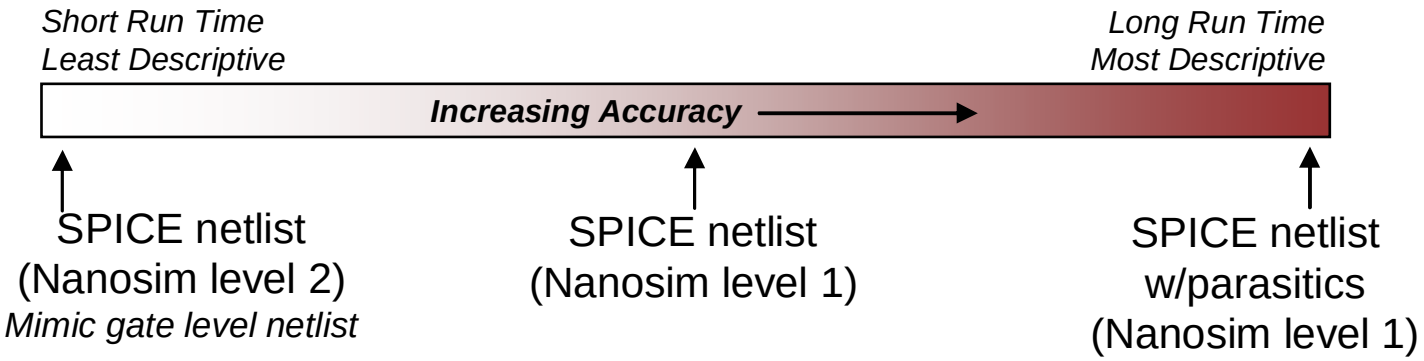


Effect of Substrate Model

Granularity Levels

- Inputs: Circuit Description



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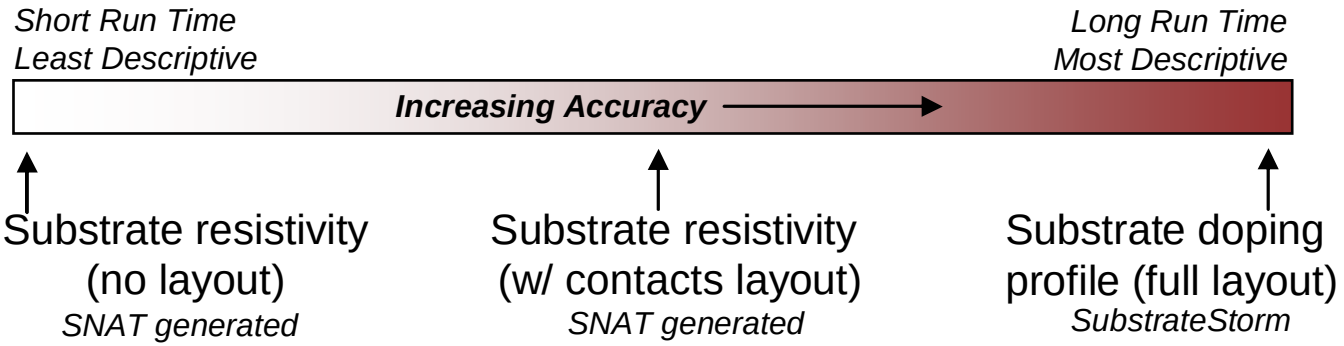
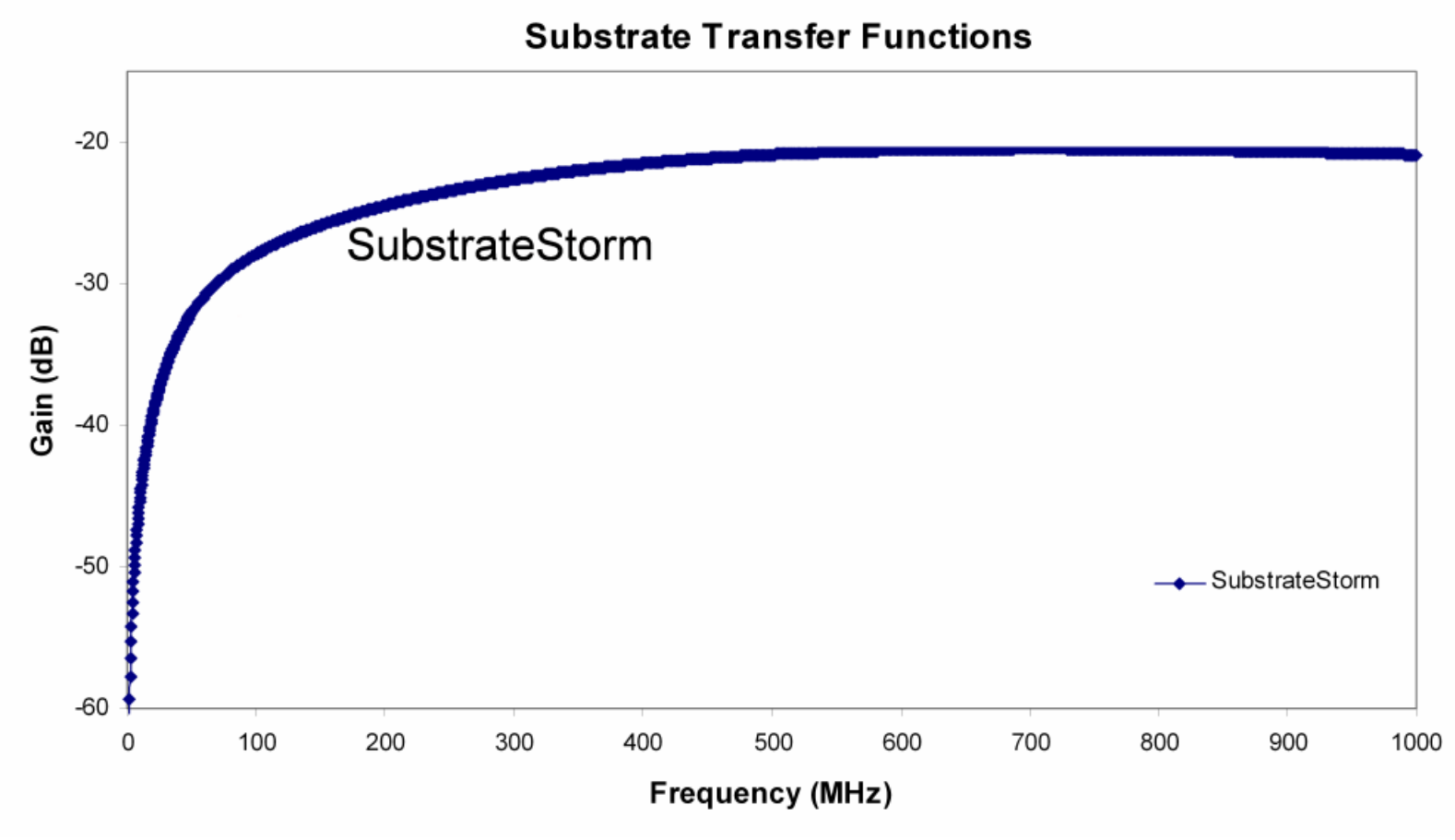
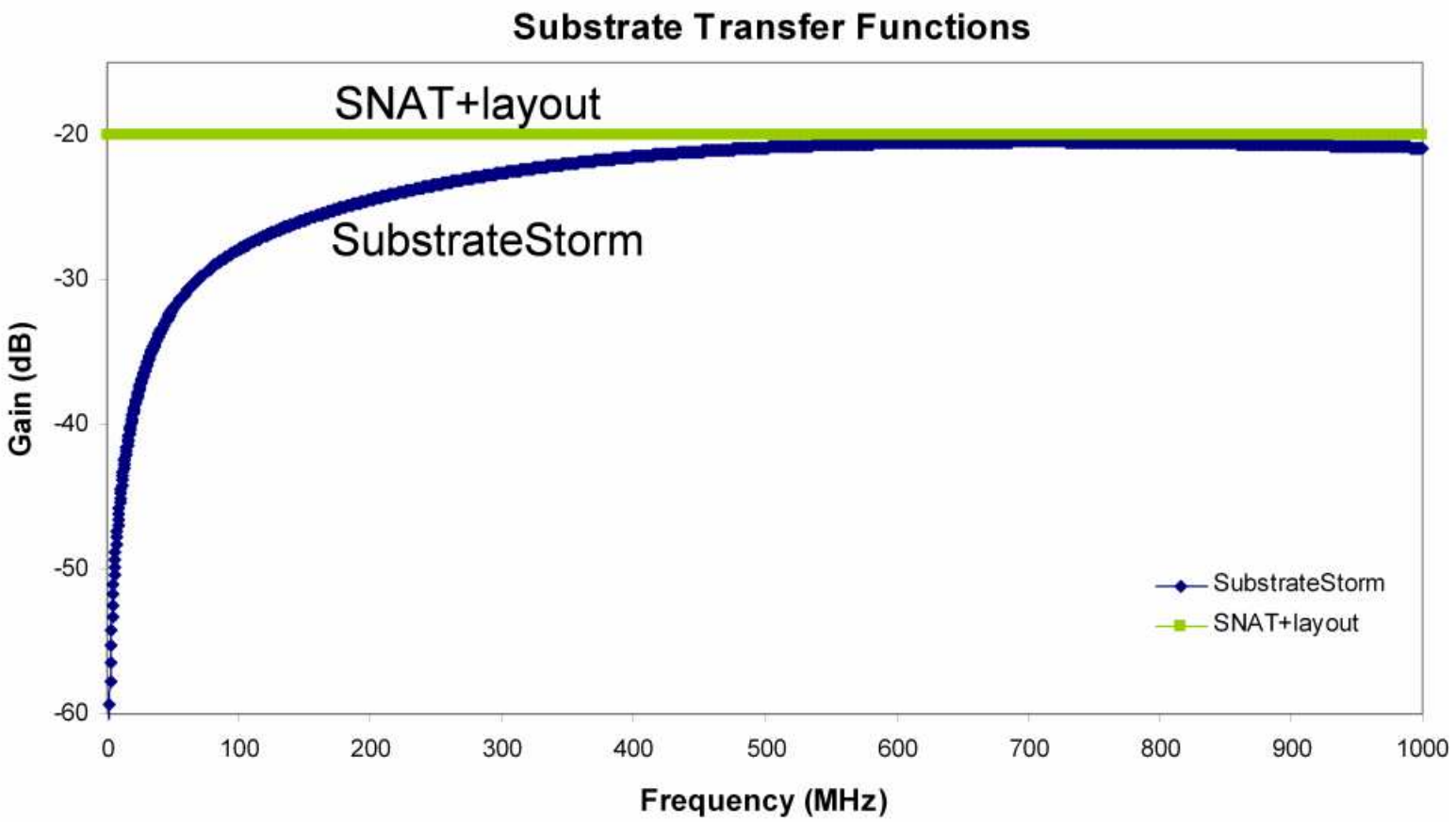


Substrate Model



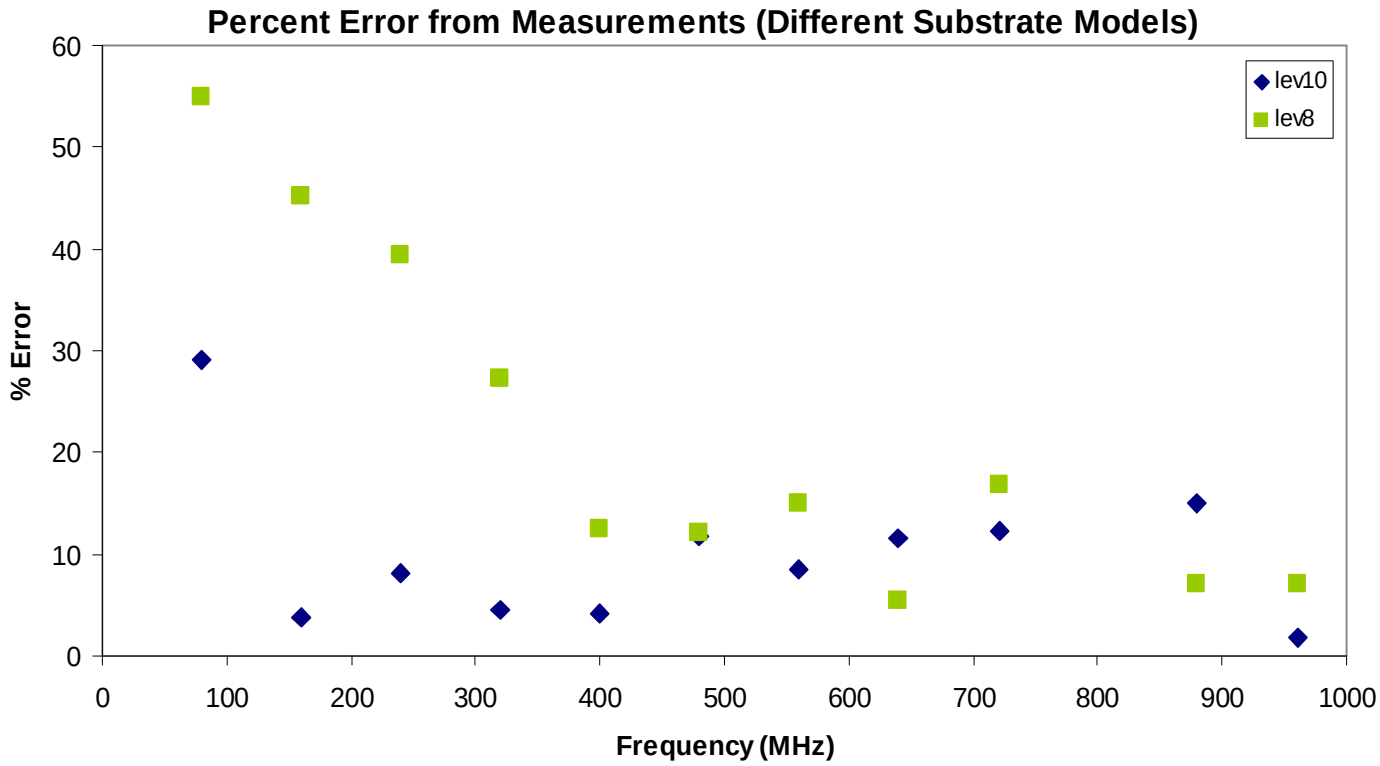
Substrate Model

- SNAT does not consider capacitive effects of wells and junctions
  - Treats substrate as purely resistive



Error

- Parasitics included
- SNAT-generated substrate model (<15 mins) vs. SubstrateStorm-generated model (51+ hrs)



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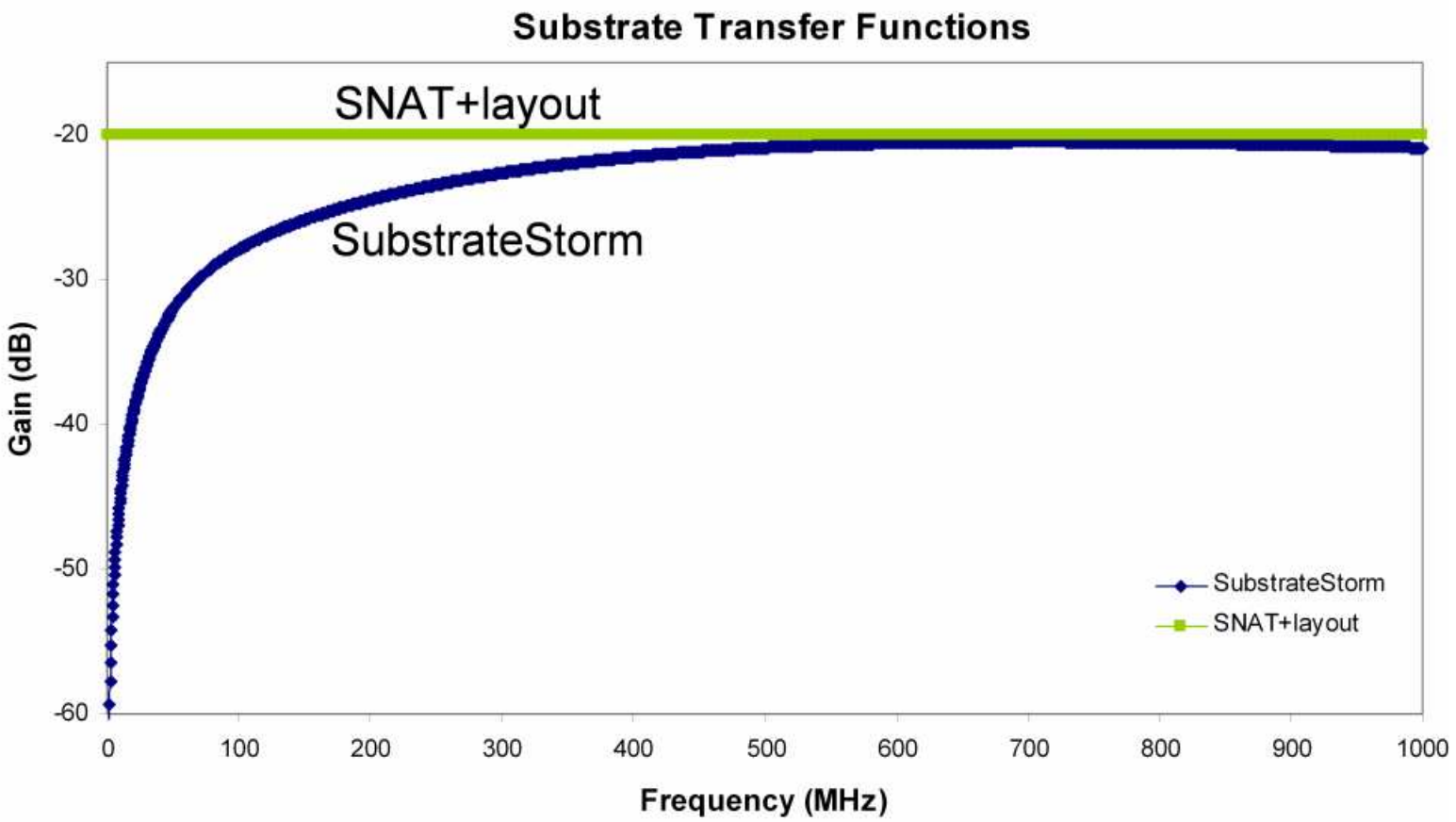

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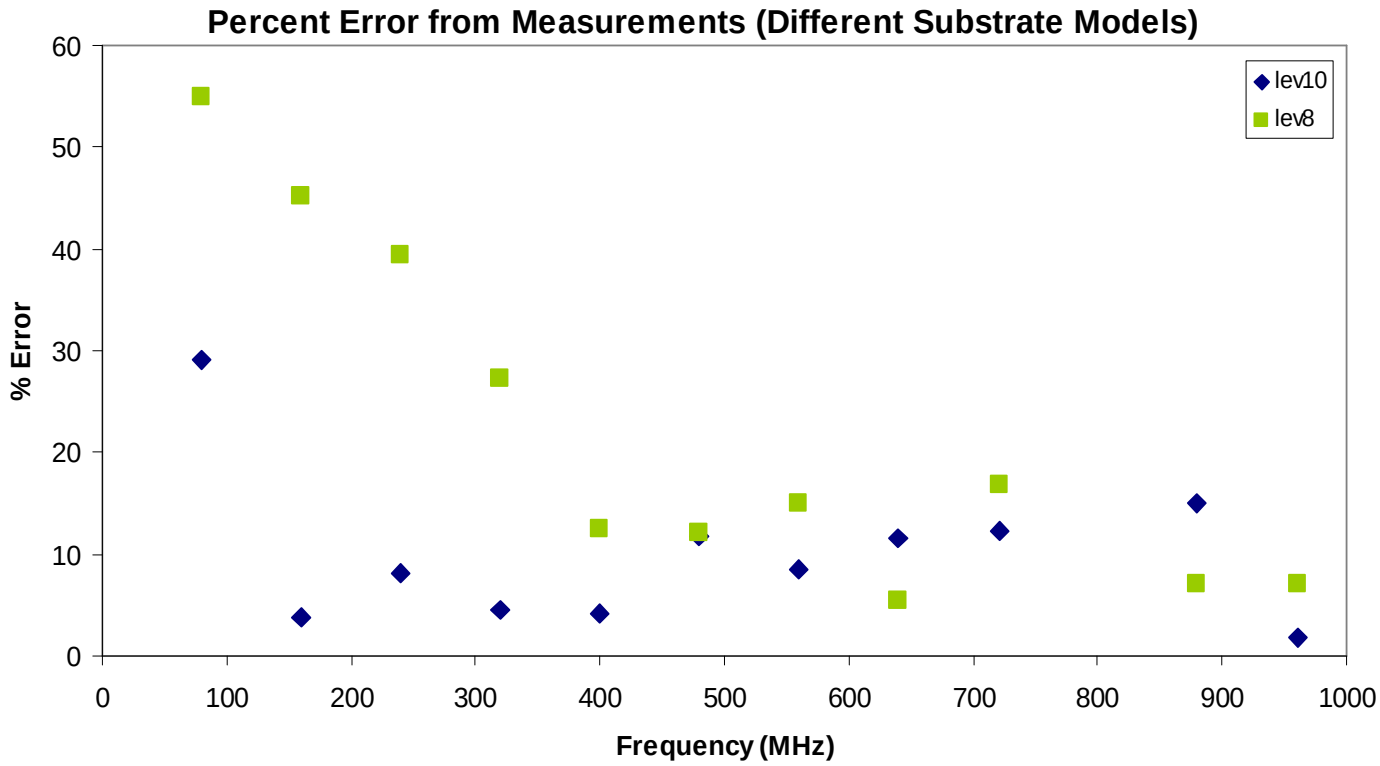
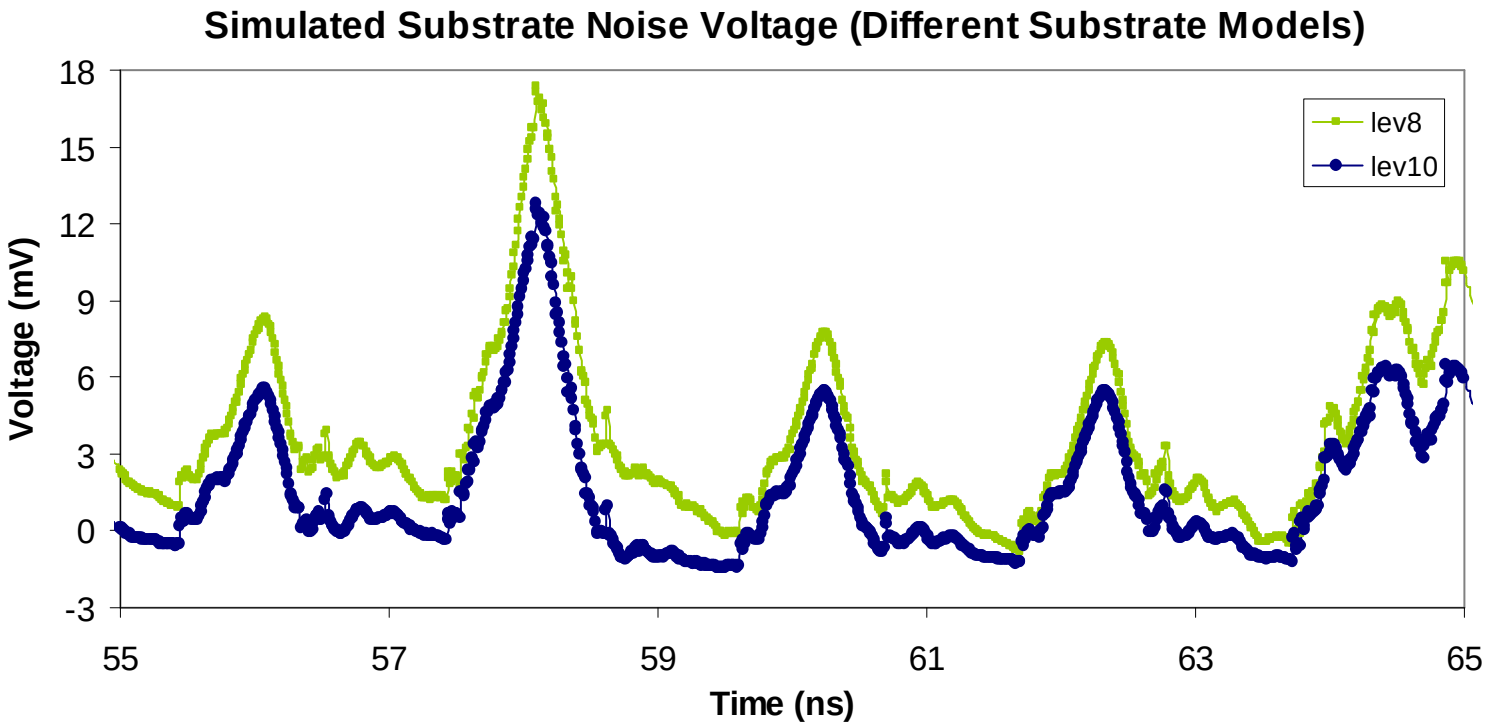


Time Domain – Effect of Substrate Model



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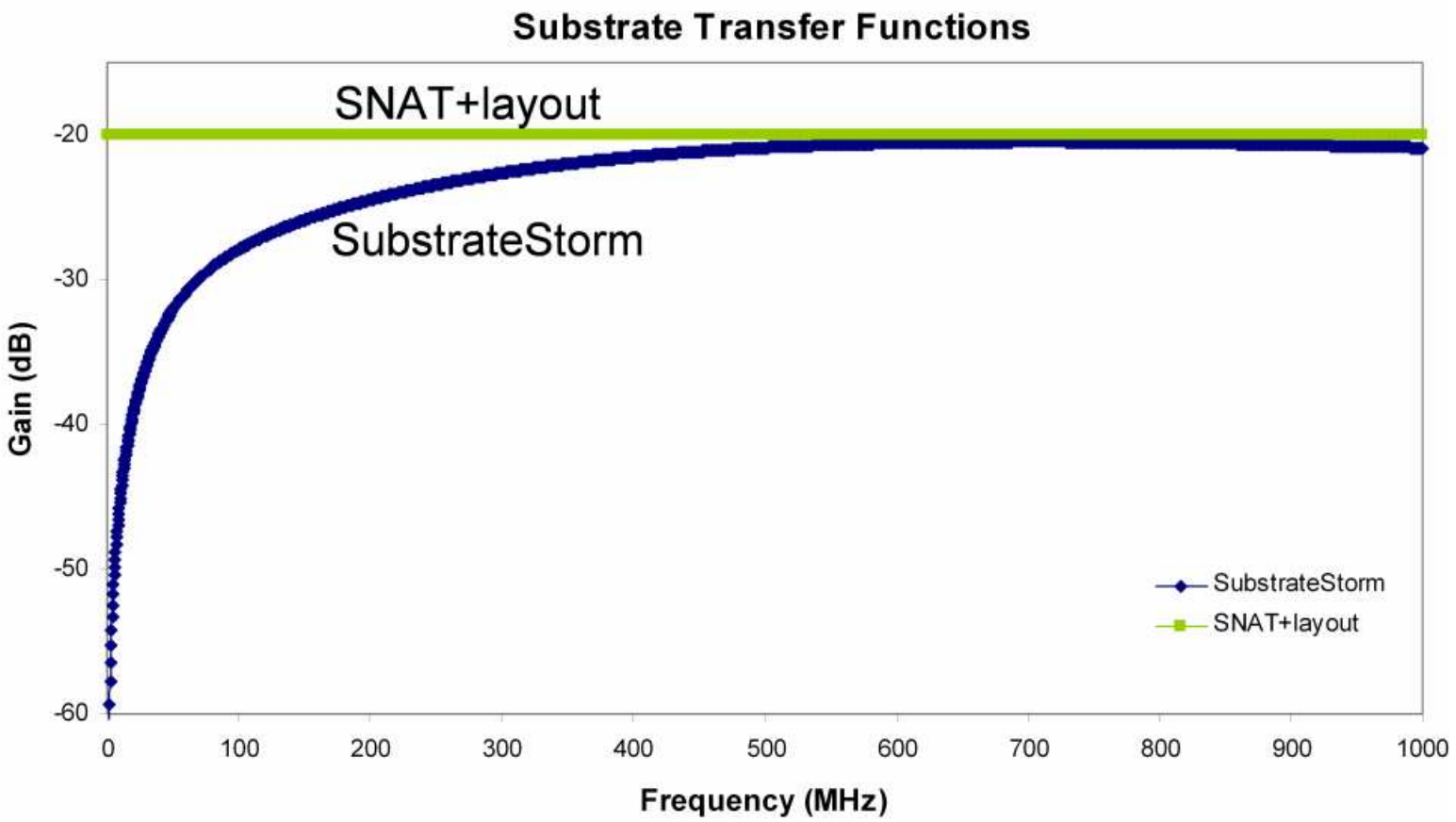

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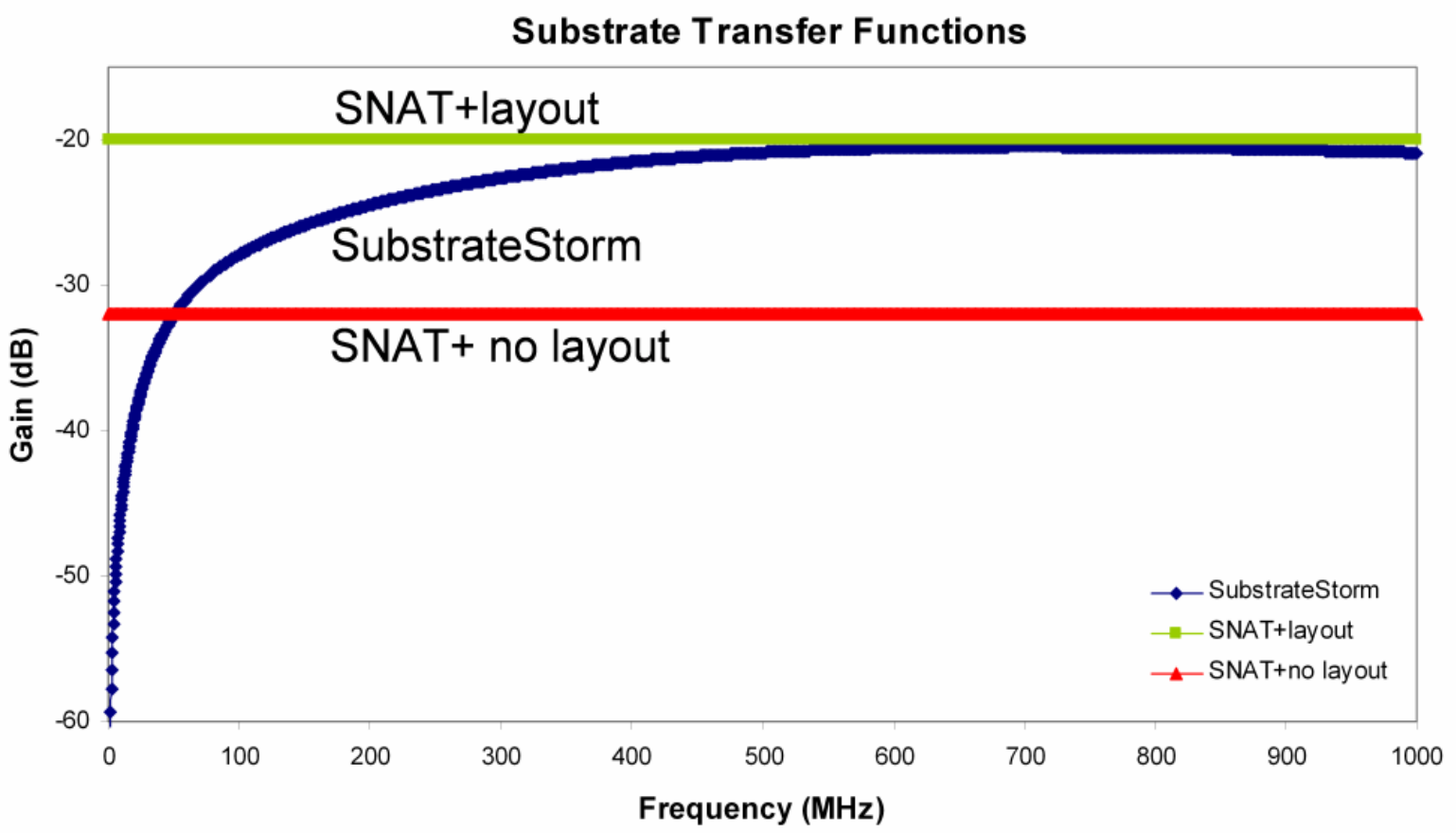
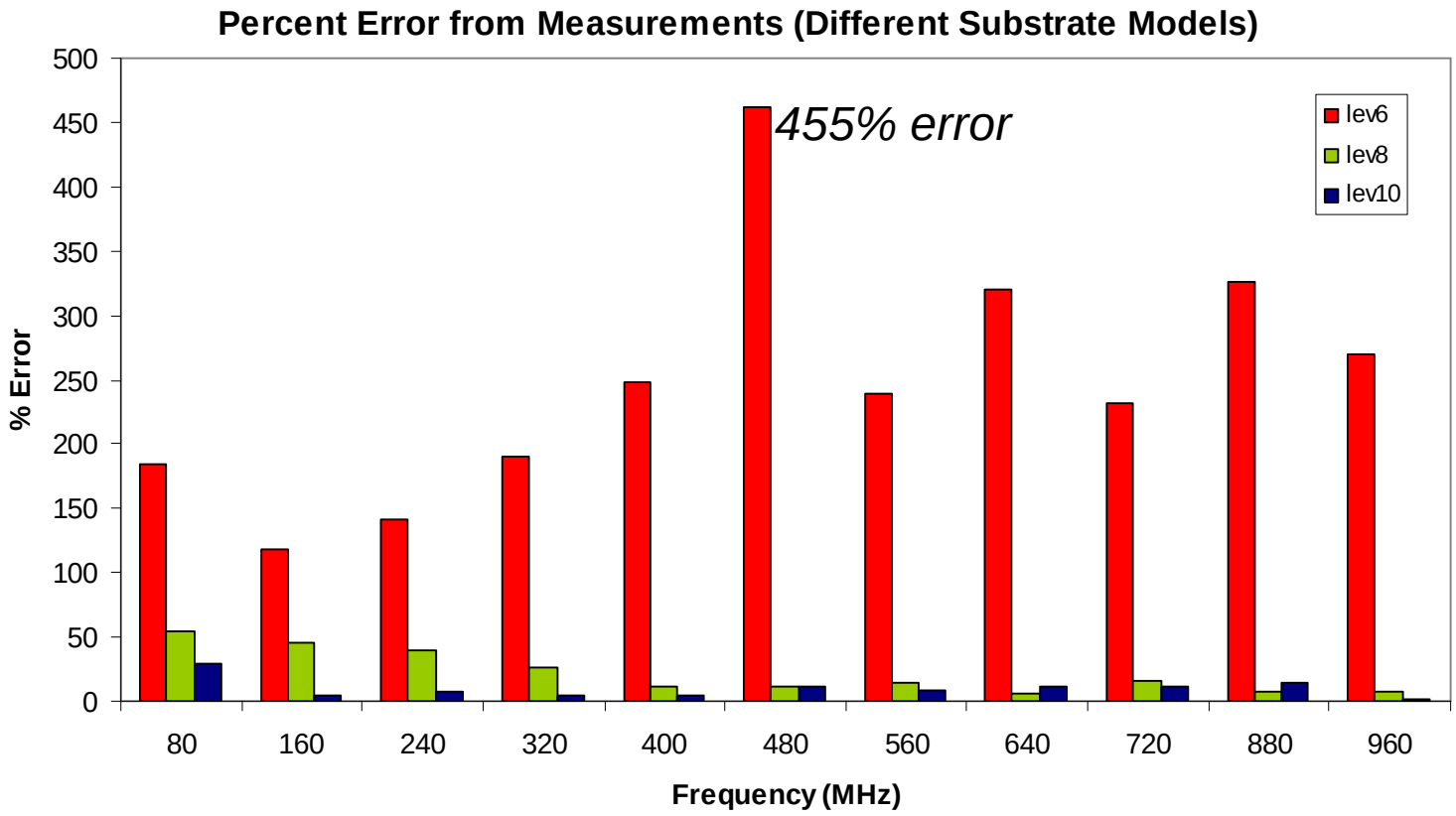


Error

- Parasitics included
- Substrate models:
  - SNAT + no layout substrate model (<10 seconds)
  - SNAT + layout substrate model (<15 mins)
  - SubstrateStorm generated model (51+ hrs)



Measurement Comparison

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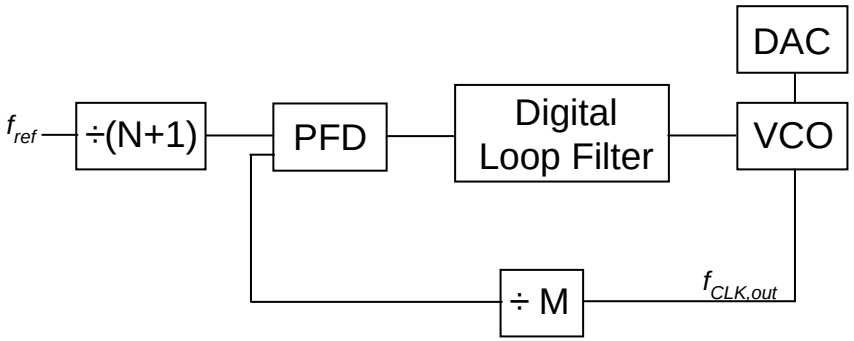
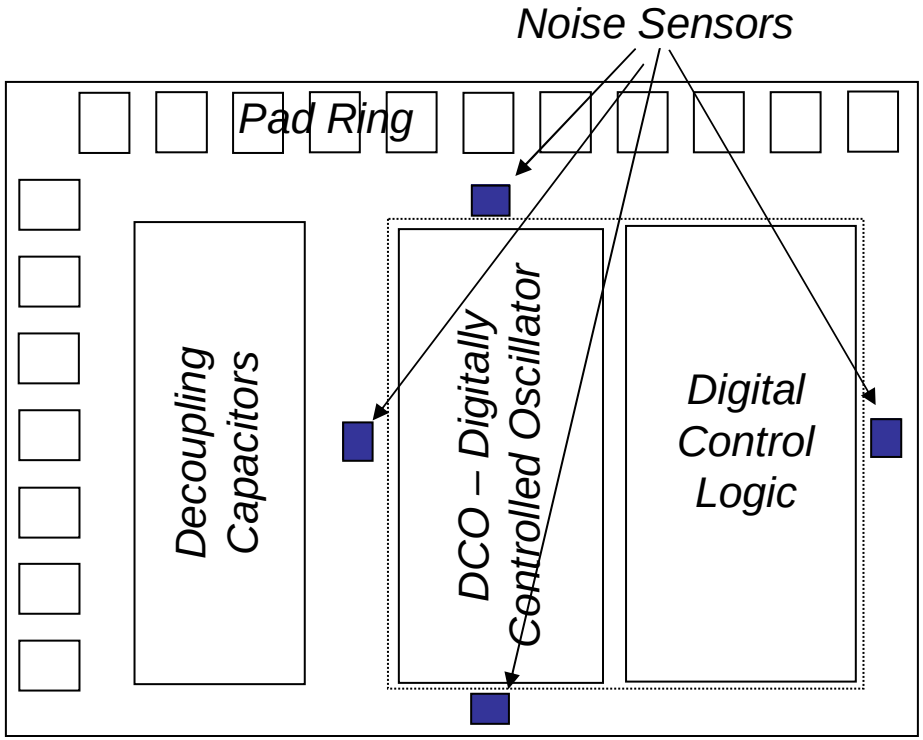
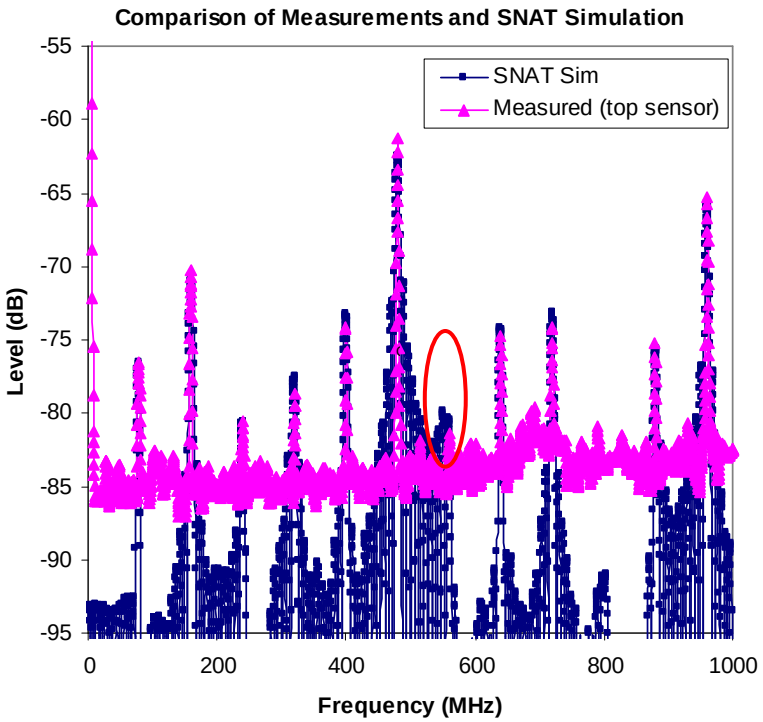


Digital PLL Block Diagram

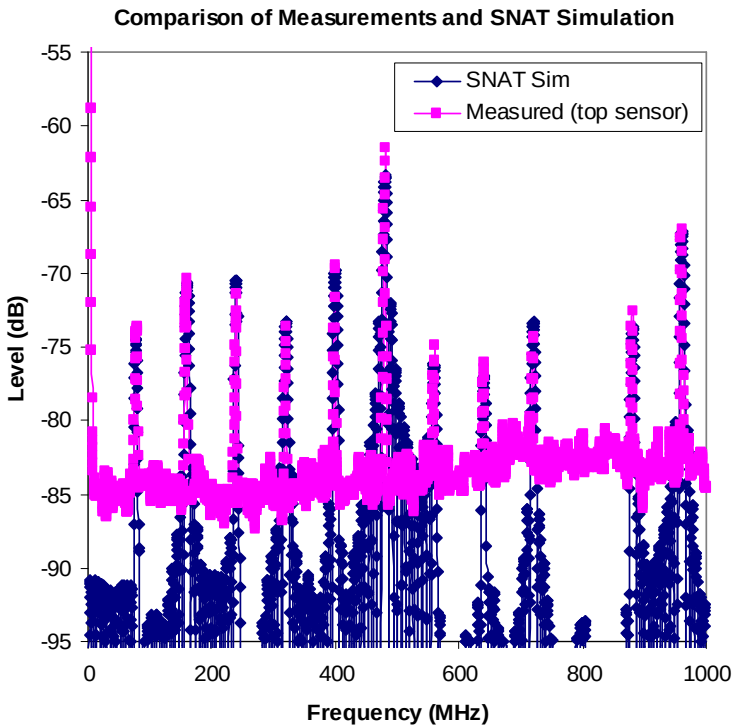


Right Sensor

- Substrate transfer function varies with sensor location



Right Sensor



Top Sensor

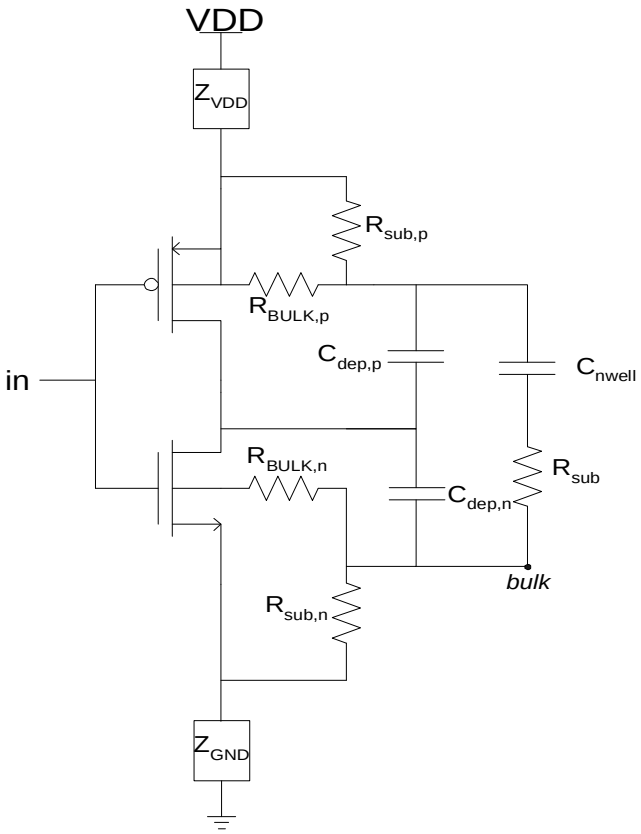
Summary

- Substrate Noise Analysis Tool (SNAT)
  - Works at any point in design cycle
  - Measured substrate noise performance of the TI DPLL
    - 11.7% error in RMS voltage
  - Can achieve a dramatic speed-up in run-time with a doubling in the error
  - Coarsest macromodel simulation can get used to yield noise order of magnitude estimate in minutes

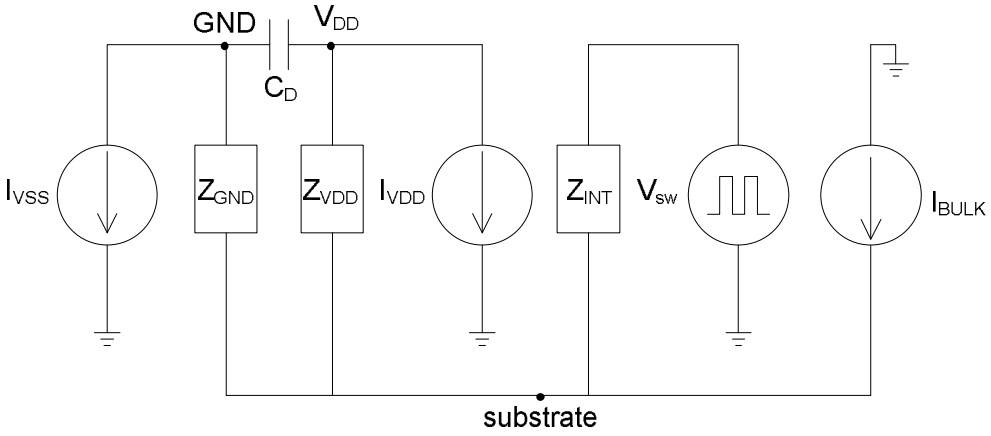
Acknowledgements

- MARCO Interconnect Focus Center
- Texas Instruments, Inc.
  - Fellowship support
  - Neeraj Nayak, Mohamed Mahmoud, Chris Barr, Baher Haroun

Macromodel Simulation



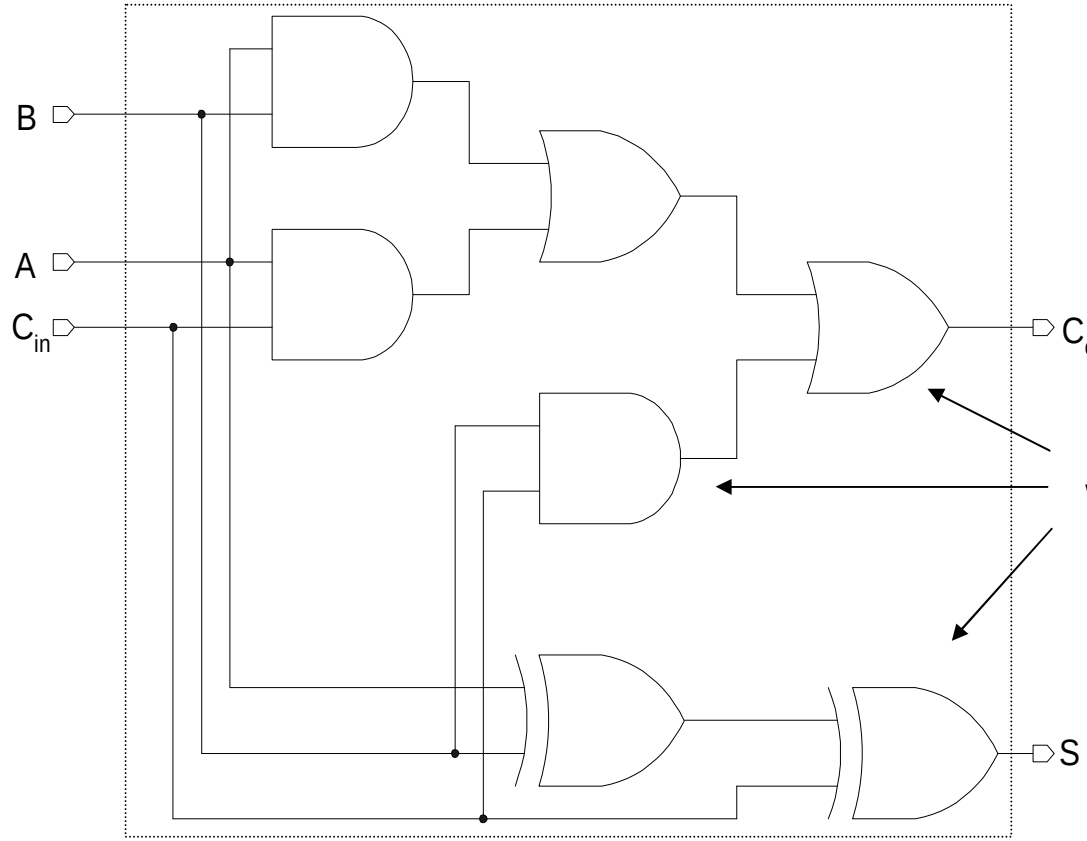
Original circuit



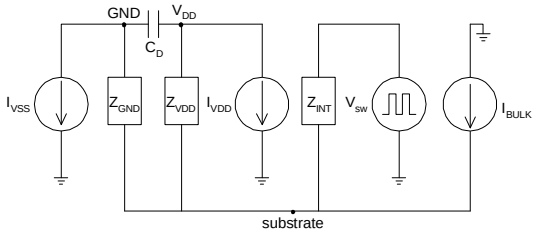
Equivalent Macromodel

Example

- Granularity level
  - Circuit: gate level netlist



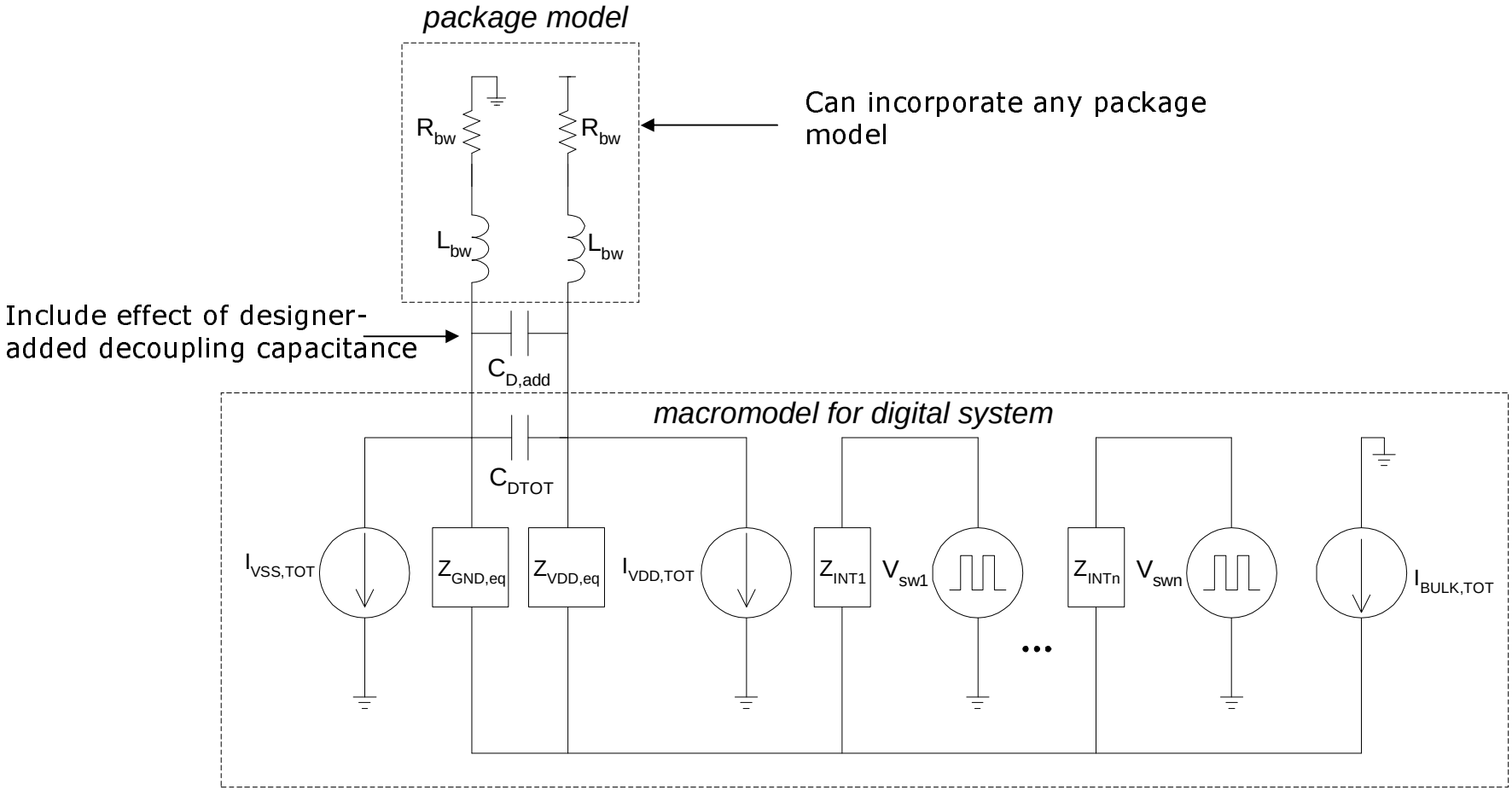
Replace each cell with equivalent macromodel



Example: One bit adder

Noise Simulation

- Represent each digital block with equivalent macromodel
- Construct macromodel for entire chip



Sample macromodel for entire digital system (assuming epi substrate)