The Effect of Substrate Noise on VCO Performance

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Abstract—The effect of substrate noise on the performance of voltage controlled oscillators (VCO) as a function of circuit isolation, bias current, and center frequency is presented. Guard rings provide as much as 25 dB of isolation for the 900 MHz VCO down to 10 dB of isolation for the 5.2 GHz VCO.

 ${\it Index\ Terms} {-\!\!\!\!--} \ substrate\ noise,\ crosstalk,\ voltage\ controlled\ oscillator$

I. INTRODUCTION

The explosive growth of the wireless telecommunications industry has resulted in increased demands for portability while achieving enhanced functionality and low power consumption. As a result of these demands, digital circuits are being placed on the same chip as sensitive radio frequency (RF) circuits.

One challenge that arises as a result of single chip integration is parasitic interactions through the shared silicon substrate. Each time a digital circuit transitions, switching currents working in tandem with circuit parasitics, such as those associated with bond wires, inject noise into the substrate. Since the silicon substrate is conductive, the noise easily propagates to analog circuits detrimentally affecting their performance as they lack the noise immunity of digital circuits.

Several papers have studied both the generation of substrate noise and characterization of the silicon substrate [5] [6]. Little research has focused on the effect of this noise on analog circuits. This study characterizes the effect of substrate noise on a standard component of the RF front end: the voltage controlled oscillator (VCO), as well as evaluating the effect of VCO bias current and guard rings on noise performance. Frequency effects of substrate noise are also examined through the study of VCOs at three different center frequencies: 900 MHz, 2.4 GHz, and 5.2 GHz.

II. TEST CHIP

The test chip was fabricated in a $0.18\mu m$ mixed-signal CMOS technology with six metal layers on a high resistivity (10-15 Ωcm) non-epi substrate.

The chip consists of seven different VCOs of varying center frequency and noise isolation schemes. The die photo is shown in Figure 1. 900 MHz, 2.4 GHz, and 5.2

GHz were chosen as the VCO center frequencies as they represent the typical operating frequencies for wireless systems such as cellular and wireless LAN.

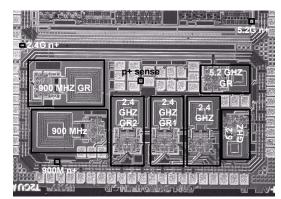


Fig. 1. Die Microphotograph of Test Chip.

For each center frequency, a VCO with and without guard ring isolation was designed. The VCOs are identical with the exception of the added guard ring surrounding the transistors of the VCO. Moreover, the test chip included several noise injection points and noise sensor locations spread over the entire die.

III. EXPERIMENTAL SETUP

The test chip was mounted onto a metal plate using conductive silver epoxy. The chip was then wafer-probed using a Cascade Microtech Summit 9000 probe station. Figure 2 depicts the experimental setup.

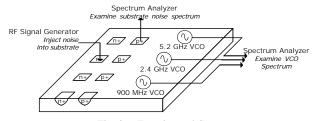


Fig. 2. Experimental Setup.

An HP83732B RF signal generator is used to generate the noise signal. RF ground-signal-ground (GSG) probes are used for all RF measurements. The RF signal is

injected into a 240 μm^2 n+ diffusion region simulating the drain of a transistor. Several n+ regions are interspersed throughout the chip so that the injection location can be varied. The locations of these regions are marked in Figure 1.

Several p+ diffusion regions are located throughout the chip so that the substrate noise at various points across the die can be probed. A spectrum analyzer is used to examine both the substrate noise spectrum and VCO output.

IV. SUBSTRATE NOISE AND VCO PERFORMANCE

The schematic for all the VCOs is shown in Figure 3. The same core is used for all VCOs with varying inductances and varactor capacitances to implement the correct center frequency. The VCO operates from a 1.8 V power supply and requires bias currents for the VCO core and output buffers that are provided off-chip.

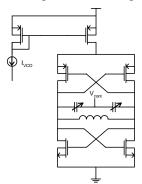


Fig. 3. VCO Schematic.

A noise signal of power -15 dBm is injected at the point labeled 900M n+, and the substrate noise is probed at the location labeled p+ sense in Figure 1. Over the frequency range from 500 MHz to 5.5 GHz, the measured gain is approximately constant at -50 dB, which corresponds to a noise level of -65 dBm. This power level was chosen to emulate the noise power levels of a large digital system. Intel reported that the noise due to the fundamental of the 1 GHz clock of the Pentium 4[®] has a power of roughly -52 dBm [4]. Even the clock harmonics contain significant power. The fifth harmonic has a power of -62 dBm while the power level of the random digital activity is approximately -75 dBm [4].

When the VCOs are powered off, and a noise signal of power -15 dBm is injected into the substrate, some noise couples directly to the output of the VCOs. This is shown in Figure 4. This indicates that noise couples either through the inductor-substrate capacitance or through the pad capacitance. To determine which of the two dominates, the noise is measured at an unconnected pad. The noise coupled through the pad capacitance is only 1-2 dB above the noise floor. Thus, all the noise that appears at the VCO output when powered off is a result of the inductor-substrate capacitance. This result is consistent with [3],

which showed that a significant amount of noise can be injected into the substrate through the inductor-substrate capacitance.

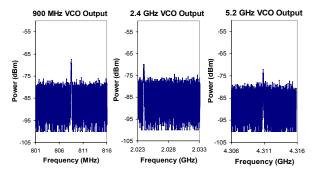


Fig. 4. VCO outputs with VCO off and noise injection.

It can be seen that as the operation frequency increases from 900 MHz to 5.2 GHz, the magnitude of the noise that couples through the inductor decreases. From 900 MHz to 5.2 GHz, the inductor area decreases by a factor of 6. Simulations using ASITIC [1] show that the inductor capacitance decreases from 220 fF for the 900 MHz VCO to 38 fF for the 5.2 GHz VCO. The reduced inductor-substrate capacitance accounts for the reduction in coupled noise as the operating frequency is increased.

When power is applied to the VCO, the noise that appears at the output is amplified as shown in Figure 5. This indicates that the noise consists of two components: noise coupling through the inductor and noise from ground. Substrate taps around the periphery of the die are connected to the circuit ground. Therefore, any substrate noise directly appears at the VCO ground.

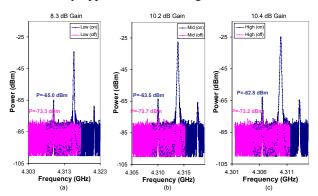


Fig. 5. 5.2 GHz VCO output with noise on and off for varying I_{VCO} . I_{low} =1.81 mA, I_{mid} =2.71 mA, I_{high} =3.41 mA.

In Figure 5a, the VCO center frequency is 4.316 GHz while the noise frequency is 4.31 GHz. The VCO output spectrum shows three peaks. The peak at 4.316 GHz corresponds to the carrier while the peak at 4.31 GHz corresponds to noise coupling to the output. The third peak is at 4.322 GHz and represents an intermodulation product as a result of the nonlinearity of the VCO [8]. The

nonlinearity of the differential stages causes mixing of the noise and the carrier resulting in intermodulation products.

For the noise depicted in Figure 5a, the higher order intermodulation terms are below the noise floor of the system. However, as the noise frequency approaches that of the VCO center frequency, the main noise component as well as the intermodulation terms are amplified as result of shaping by the LC tank. This resonance gain behavior is observed in Figure 6. As a result, higher order intermodulation terms appear at the VCO output as the noise frequency approaches that of the carrier. This is depicted in Figure 7.

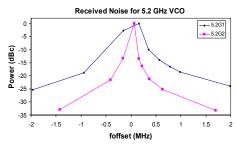


Fig. 6. Effect of guard rings on the noise power of the 5.2 GHz VCO around $f_{carrier}$. 5.2G1 has no guard ring. 5.2G2 has a guard ring.

A. Effect of VCO Bias Current

As the VCO bias current is increased, the gain experienced by the noise increases as shown in Figure 5. This is most likely a result of the ground noise being multiplied by g_m to appear at the VCO output. For increasing bias current and operation in the current-limited regime, the VCO phase noise does not degrade despite the increased noise level as the carrier power also increases with bias current [7]. For the 5.2 GHz VCO, a bias current of 2.7 mA places the VCO at the edge of the current-limited regime. Increasing the bias current beyond this level places the VCO in the voltage-limited regime where the carrier power is limited by the power supply and no longer scales with current. The noise level still scales with current; therefore, when operating in the voltage-limited regime, the phase noise actually degrades since the carrier power remains constant. This is depicted in Figure 7. Table I shows the ratio of carrier power to noise power for the 5.2 GHz VCO over three different bias current levels.

 $\label{eq:table I} \textbf{TABLE I}$ Ratio of carrier to noise power for 5.2 GHz VCO

I_{VCO}	P_c/P_n
1.81 mA	9.9 dB
2.71 mA	26.3 dB
3.41 mA	23.1 dB

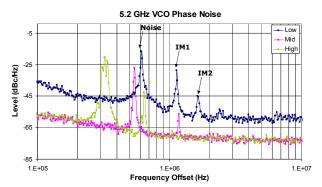


Fig. 7. Phase noise of the 5.2 GHz VCO for varying I_{VCO} . I_{low} =1.81 mA, I_{mid} =2.71 mA, I_{high} =3.41 mA.

B. Effect of Guard Rings

Double guard rings consisting of p+ and n-well annular regions were placed surrounding the active devices of the VCO but not surrounding the inductor. Guard rings mitigate substrate noise by sinking the surface portion of the substrate current to a lower impedance supply.

The output spectrums of the VCOs with and without guard ring isolation were examined in the presence of substrate noise.

The guard rings could only attenuate the circuit component of the noise and not the inductor component as they were placed surrounding only the active devices. Figure 6 shows that the guard ring provides roughly 10 dB of isolation around the carrier frequency for the 5.2 GHz VCO. The guard ring isolation degrades closer to the carrier frequency as both the circuit and inductor components of the noise experience a higher gain from the resonance of the LC tank; however, the guard ring only attenuates the circuit component.

Figure 8 shows that guard rings can significantly attenuate the circuit noise component at lower operating frequencies; however, their effectiveness degrades at higher frequencies due to circuit parasitics. For example, at 900 MHz, guard rings provide approximately 15-20 dB of isolation around the carrier frequency. That isolation reduces to approximately 10 dB at 5.2 GHz.

V. INJECTION LOCKING

If the frequency of an interferer approaches the resonant frequency of a VCO, the oscillator can lock to the interference frequency instead of the resonant frequency of the LC tank if the power of the interferer is comparable to that of the carrier [2]. The design of injection locked frequency synthesizers relies on this phenomenon.

It has been well established that injection locking is a serious impediment to the single chip integration of an RF power amplifier and a VCO as the transmitted signal is of appreciable power and acts as an interferer to the VCO [9]. This study shows that without careful design, digital

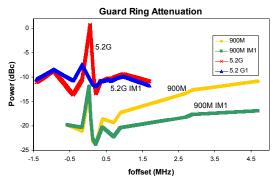


Fig. 8. Guard ring attenuation around $f_{carrier}$ for the noise component and IM1

TABLE II 5.2 GHz VCO AND INJECTION LOCKING

GR?	f_{center}	Locking Frequency Range
No GR	4.3148 GHz	500 kHz
GR	4.314 GHz	200 kHz

circuit generated substrate noise can also result in VCO injection locking.

As mentioned in Section IV, the substrate noise levels considered in this work are on par with that of higher order clock harmonics of a large digital system. The shaping behavior of the resonant tank causes noise around the resonant frequency to be amplified as discussed in Section IV. The shaping function can cause the noise to become significant enough to result in injection locking. Figure 9 shows that the 5.2 GHz VCO locks to substrate noise offset from the center frequency by 20 kHz. Because

5.2 GHz VCO Spectrum

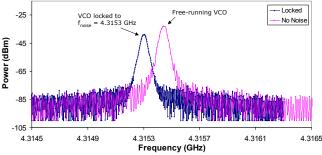


Fig. 9. Spectrum of 5.2 GHz VCO.

guard rings can attenuate noise by as much as 25 dB for the 900 MHz VCO, guard rings also reduce the range of frequencies for injection locking. Tables II-IV show the range of frequencies for which injection locking occurs.

VI. CONCLUSIONS

Substrate noise is a serious problem that continues to plague mixed-signal designs. Components of the RF front

TABLE III
2.4 GHZ VCO AND INJECTION LOCKING

Γ	GR?	f_{center}	Locking Frequency Range
	No GR	2.027 GHz	50 kHz
	GR	2.031 GHz	30 kHz

TABLE IV 900 MHz VCO and Injection Locking

GR?	f_{center}	Locking Frequency Range
No GR	812.89 MHz	5 kHz
GR	805.13 MHz	Doesn't Lock

end are particularly sensitive to substrate noise as the effectiveness of standard isolation techniques degrades at higher frequencies. This study has shown that the phase noise of a VCO is adversely affected by substrate noise. In the extreme, the VCO can lock to the substrate noise.

Guard rings can effectively attenuate substrate noise at lower frequencies. For example, at 900 MHz, as much as 25 dB of isolation is observed. At 5.2 GHz, the isolation reduces to 10 dB. Furthermore, the use of guard rings can improve the response of the VCO to injection locking.

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REFERENCES

- [1] http://rfic.eecs.berkeley.edu/ niknejad/asitic.html.
- [2] Razavi, B. "A study of injection locking and pulling in oscillators," Solid-State Circuits, IEEE Journal of, vol. 39(9), pp. 1415-1424, Sept. 2004.
- [3] Pun, A.L.L, et.al. "Substrate noise coupling through planar spiral inductor," *Solid-State Circuits, IEEE Journal of*, vol. 33(6), pp. 877-884, June 1998.
- [4] Franca-Neto, L.M., et.al. "Enabling high-performance mixed-signal system-on-a-chip (SoC) in high performance logic CMOS technology," VLSI Circuits Digest of Technical Papers, pp. 164-167.
- [5] Badaroglu, M., et.al. "Modeling and experimental verification of substrate noise generation in a 220-Kgates WLAN system-on-chip with multiple supplies," *Solid-State Circuit, IEEE Journal of*, vol. 38(7), pp. 1250-1260, July 2003.
- [6] Kristiansson, S., et.al. "Substrate resistance modeling for noise coupling analysis," *Microelectronic Test Structures, International Conference on*, pp. 123-129, March 2003.
- [7] Lee, T.H. and Hajimiri, A. "Oscillator phase noise: a tutorial," *Solid-State Circuits, IEEE Journal of*, vol. 35(3), pp. 326-336, March 2000.
- [8] Razavi, B. "A study of phase noise in CMOS oscillators Razavi," Solid-State Circuits, IEEE Journal of, vol. 31(3), pp. 331-343, March 1996
- [9] Razavi, B. RF Microelectronics, Prenctice-Hall, Location, 1998.