Modeling and Analysis for Substrate Noise Mitigation in High Frequency Integrated Circuits

SRC CADTS Design Review

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Karti Mayaram and Terri Fiez

School of EECS

Oregon State University, Corvallis OR

Task ID: 1299.001 (Cont. of 911)

Technical Thrust:	Physical Design
Task Leaders:	Karti Mayaram and Terri Fiez
Students:	Kyle Webb (M.S., June 2005) Martin Held (M.S., June 2005) Sasi Arunachalam (M.S., Aug 2005) Matt MacClary (M.S., Aug 2006) Andrew Tabalujan (M.S., Aug 2007) Chenggang Xu (Postdoc)
Industrial Liaisons:	James Falbo (Mentor)
Anticipated Result:	An overall design-oriented approach for substrate noise analysis and planning in high frequency mixed-signal ICs. This will include developing substrate models for high frequencies, identifying efficient approaches for simulation of substrate noise, and developing and validating isolation strategies.

Task Deliverables

- **Report on the frequency behavior of substrate coupling for both heavily and lightly doped substrates (Planned: 31-Mar-2006)**
- **Report on the development of accurate scalable equivalent circuit models for multi-gigahertz applications (Planned: 31-Mar-2007)**
- **Report on the design of test structures for extraction of parameters for the substrate coupling models (Planned: 31-Aug-2007)**
- **Report on the model validation with silicon measurements and incorporation into the Silencer! tool framework (Planned: 31-Mar-2008)**

Task Description

The focus of our work is on management of substrate noise early in the overall design flow as well as techniques for mitigating the noise. In our approach, a scalable model simplifies the overall approach so that the designer can incorporate simple networks into their design. In addition, we have developed a Green's function solver that will be used for a detailed examination of the silicon substrate behavior over frequency. Our preliminary simulation results point out the need for use of different types of equivalent circuit models for the self and mutual-coupling admittances. These results will be verified with fabricated test structures. The equivalent circuit representations will be extracted from the measured data. Once the frequency dependence and the equivalent circuit models have been modified, development of scalable models will take place. We will use numerical simulations to understand the complete parameter space and develop appropriate functional dependencies for the coupling impedances.

Executive Summary

- **Accomplishments during the past year**
  - ✓ Developed an error control method for discrete cosine transforms (DCT) used in substrate parasitic extraction
  - ✓ Demonstrated efficient Green's function formulation for inhomogeneous substrate layers
  - ✓ Developed new techniques for high frequency (<20GHz) substrate characterization
  - ✓ Integrated compression algorithm into Silencer! for digital substrate noise prediction

Executive Summary

- **Future direction**
  - ✓Characterize frequency behavior of substrate coupling for silicon substrates
  - ✓Develop accurate scalable equivalent circuit models for multi-gigahertz applications
  - ✓Validate model with silicon measurements and incorporate into the Silencer! tool framework

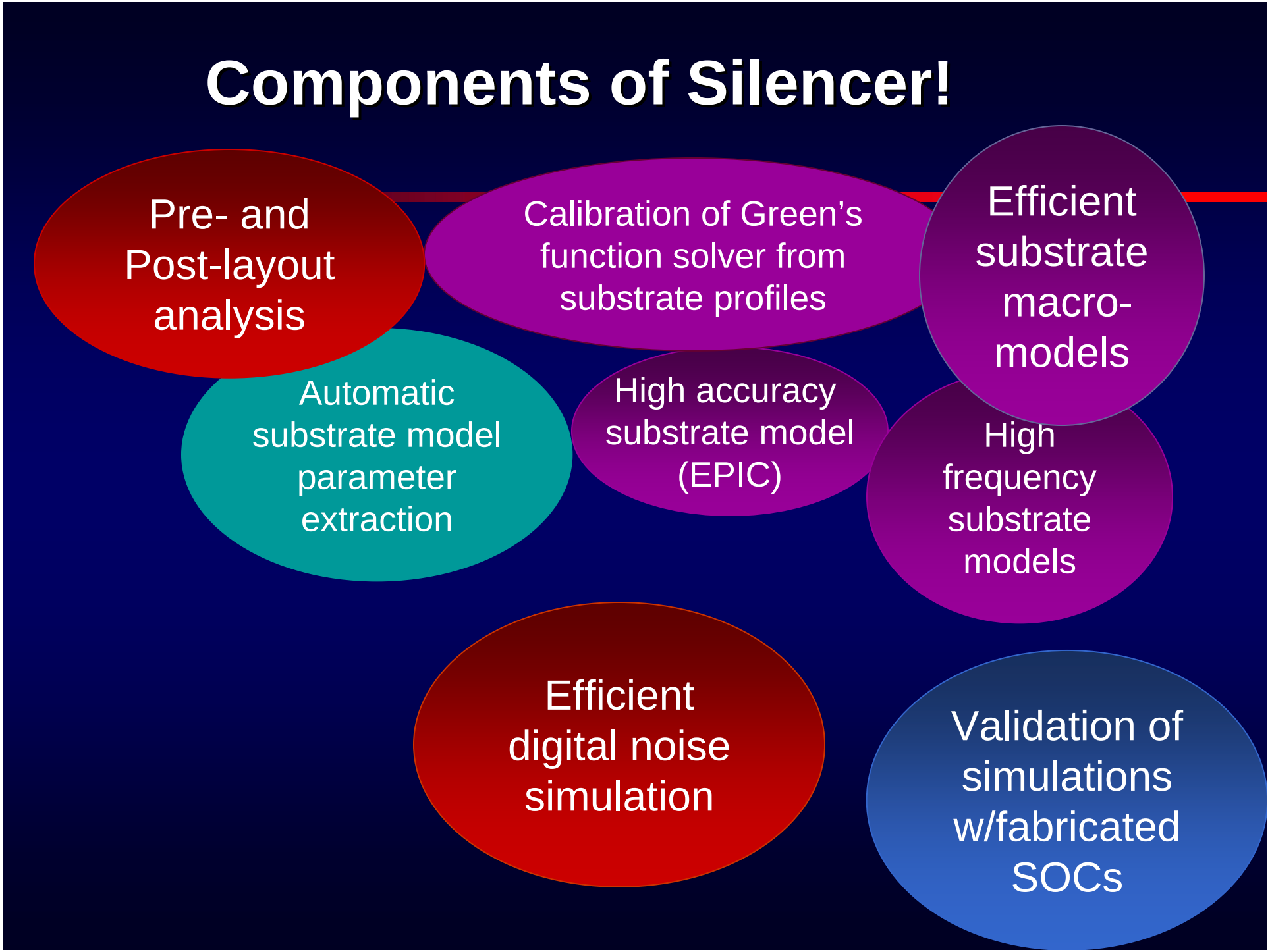
Executive Summary

- **Technology transfer & industrial interactions**
  - ✓ SRC eworkshop
  - ✓ Silencer! transferred to National
  - ✓ Interactions with Mentor, Intel, and Freescale
- **Publications**
  - ✓ B. Owens, S. Adluri, P. Birrer, R. Shreeve, S. Arunachalam, K. Mayaram, and T. S. Fiez, "Simulation and measurement of supply and substrate noise in mixed-signal ICs," *IEEE J. Solid-State Circuits*, vol. 40, pp. 382-391, Feb. 2005.
  - ✓ H. Habal, K. Mayaram, and T. S. Fiez, Accurate and efficient simulation of synchronous digital switching noise in systems on a chip," *IEEE Trans. VLSI*, vol. 13, pp. 330-338, March 2005.
  - ✓ C. Xu, T. Fiez, and K. Mayaram, "On the numerical stability of Green's function for substrate coupling in integrated circuits," *IEEE Trans. Computer-Aided Design*, vol. 24, pp. 653-658, April 2005.

Executive Summary

- **Publications**
  - ✓ C. Xu, R. Gharpurey, T. S. Fiez, and K. Mayaram, “A Green function-based parasitic extraction method for inhomogeneous substrate layers,” *Proc. DAC 2005*, pp. 141 - 146, June 2005.
  - ✓ A. Sharma, P. Birrer, S. K. Arunachalam, C. Xu, T. S. Fiez, and K. Mayaram, “Accurate prediction of substrate parasitics in heavily doped CMOS processes using a calibrated boundary element solver,” *IEEE Trans. VLSI*, pp. 843-851, July 2005.
  - ✓ S. Hsu, T. S. Fiez, and K. Mayaram, “Modeling of substrate noise coupling for NMOS transistors in heavily doped substrates,” *IEEE Trans. Electron Devices*, pp. 1880 -1886, Aug. 2005.
  - ✓ C. Xu, T. Fiez, and K. Mayaram, “An error control method for application of the discrete cosine transform to extraction of substrate parasitics in ICs,” *IEEE Trans. Computer-Aided Design*, March 2006.
- **Patentable inventions, patent applications**
  - ✓ None

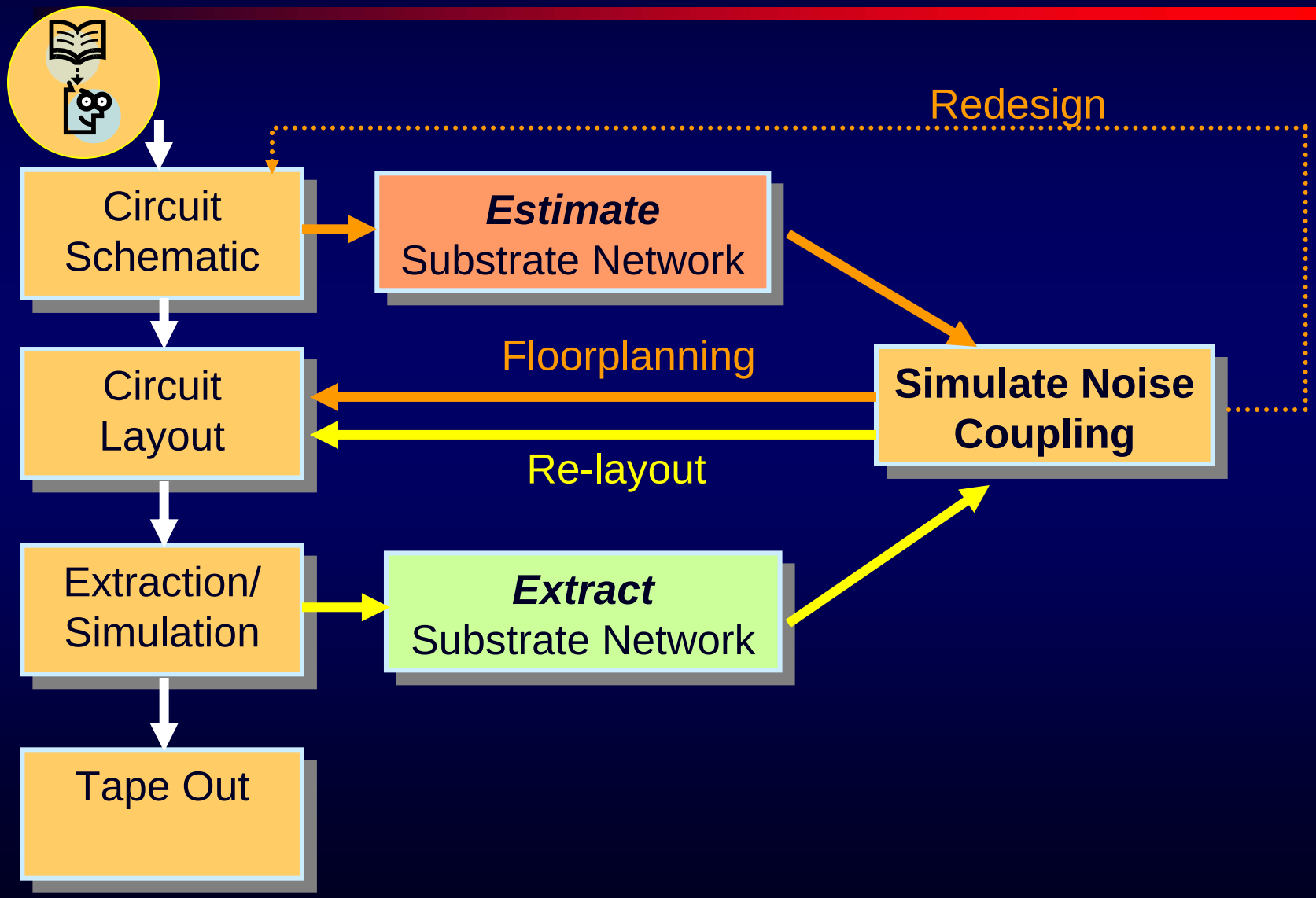
Components of Silencer!



Components of Silencer!

Pre- and Post-layout analysis

Substrate Noise Coupling in Design Flow



Components of Silencer!

Efficient substrate macro-models

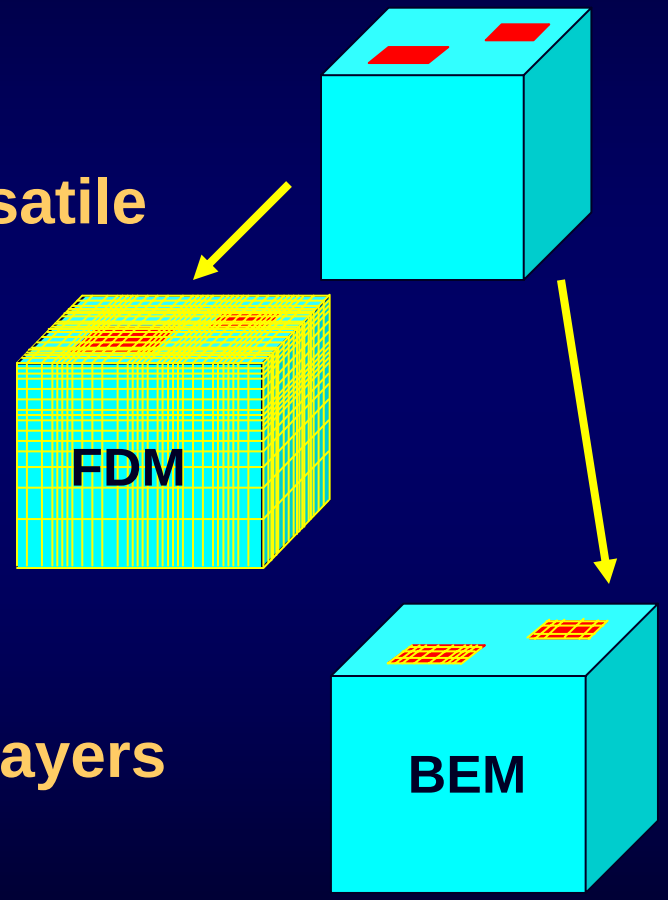
High accuracy substrate model (EPIC)

Numerical Methods for Substrate Parasitic Extraction

Finite difference methods (FDM)

Computationally expensive but versatile

- ✓ **Large number of nodes**
- ✓ **Suitable for complex structures**



Boundary element methods (BEM)

Computationally more efficient but normally limited to homogeneous layers

- ✓ **Smaller number of nodes**
- ✓ **Suitable for simple structures**

EPIC Enhancements

- **EPIC is a custom Green's function solver developed at Oregon State University for accurately extracting substrate parasitics**
  - ✓An error control method for discrete cosine transforms (DCT) used in substrate parasitic extraction
  - ✓Efficient Green's function formulation for inhomogeneous substrate layers

Discrete Cosine Transform (DCT) Approximation and Error Sources

- **Matrix entries can be expressed in terms of the following form**

$$\sum_{m=1}^{\infty}\sum_{n=1}^{\infty} F_{mn} \cos\left(m\pi \left(\frac{x^{\xi}}{a} \pm \frac{x^{\eta}}{a} \right) \right) \cos\left(n\pi \left(\frac{y^{\xi}}{b} \pm \frac{y^{\eta}}{b} \right) \right)$$

where $\left(x^{\xi}, y^{\xi}\right)$ and $\left(x^{\eta}, y^{\eta}\right)$ are the vertex coordinates of panel ξ and η

  - ✓ **Too expensive for direct calculation even after truncation**
- **DCT calculation efficient with a FFT-based method***

$$\sum_{m=1}^{P-1}\sum_{n=1}^{Q-1} F_{mn} \cos\left(m\pi \left(\frac{p}{P} \right) \right) \cos\left(n\pi \left(\frac{q}{Q} \right) \right)$$

where p, P, q, and Q are integers

- **DCT approximation of the matrix entry equation***
  - ✓ Series truncation: $m_{\max} = P - 1 \quad n_{\max} = Q - 1$
  - ✓ Ratios' integer-rounding: $\frac{x}{a} \cong \frac{p}{P} \qquad \frac{y}{b} \cong \frac{q}{Q}$

*R. Gharpurey, *Ph.D. Dissertation*, 1995

Rounding Error Control by Interpolation

- **Transform (instead of approximating) the truncated series into the following form[+]**

$$\sum_{m=1}^{P-1}\sum_{n=1}^{Q-1} F'_{mn} \cos\left(m\pi\frac{\tilde{x}}{P}\right)\cos\left(n\pi\frac{\tilde{y}}{Q}\right)$$

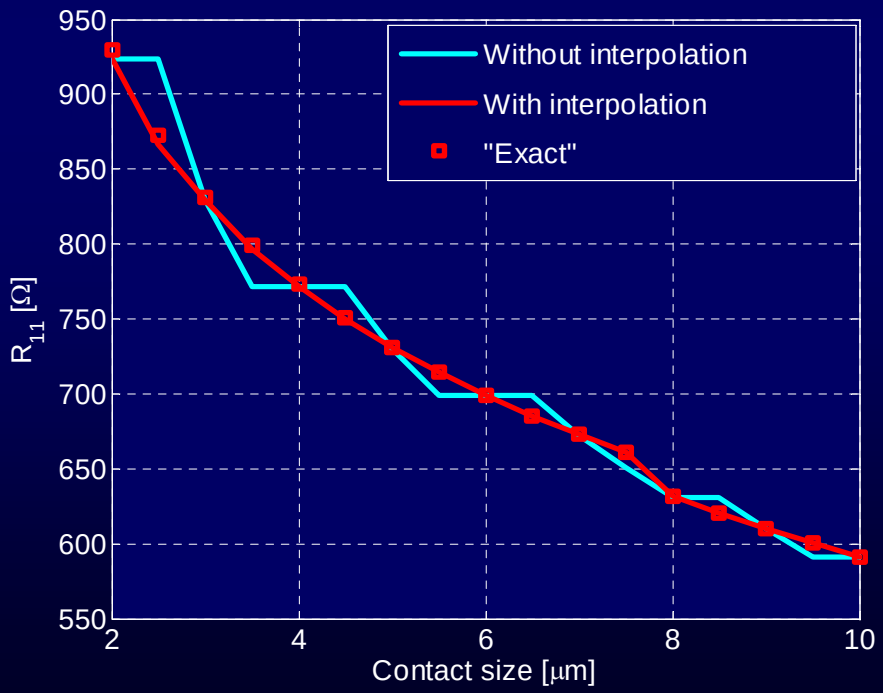
Where $\tilde{x}$ and $\tilde{y}$ are, in general, not integers. Therefore, the formulation above is not a DCT, but a function of $\tilde{x}$ and $\tilde{y}$, i.e., $f(\tilde{x},\tilde{y})$

- **Using DCT establish for function $f(\tilde{x},\tilde{y})$ a companion 2-D table $f(i,j)$, where i, and j are integers**
- **Use $f(i,j)$ to interpolate $f(\tilde{x},\tilde{y})$ when $\tilde{x}$ and $\tilde{y}$ are not integers**

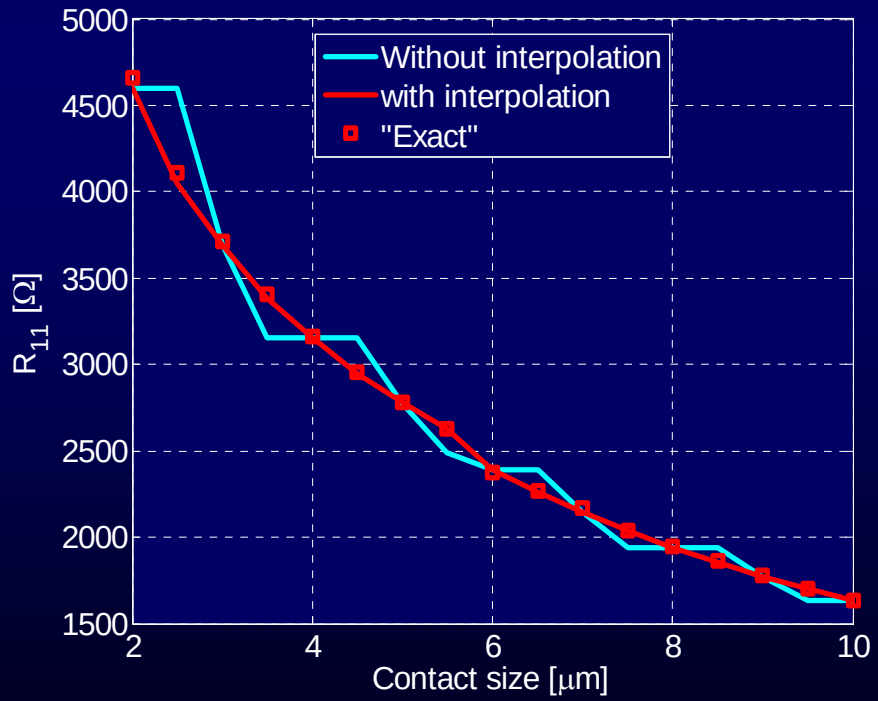
[+]**C. Xu, T. Fiez, and K. Mayaram, *IEEE Trans. CAD*, March 2006**

Error in Contact Area Due to Rounding

- **One contact in a substrate with different contact sizes**
  - ✓ **Very large DCT size (16,384) for "Exact" results**
  - ✓ **Smaller DCT size (1024) without interpolation**
  - ✓ **Smaller DCT size (1024) with Interpolation**



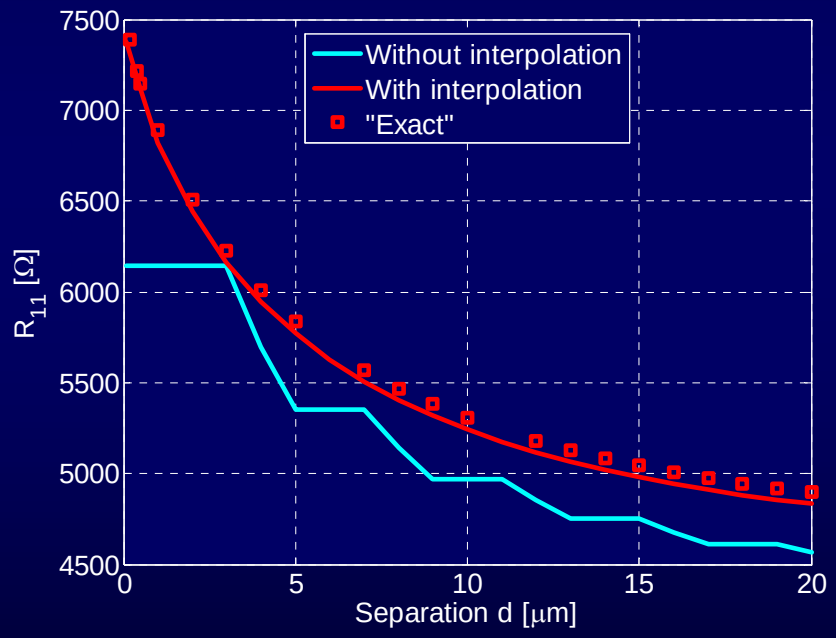
Heavily Doped Substrate



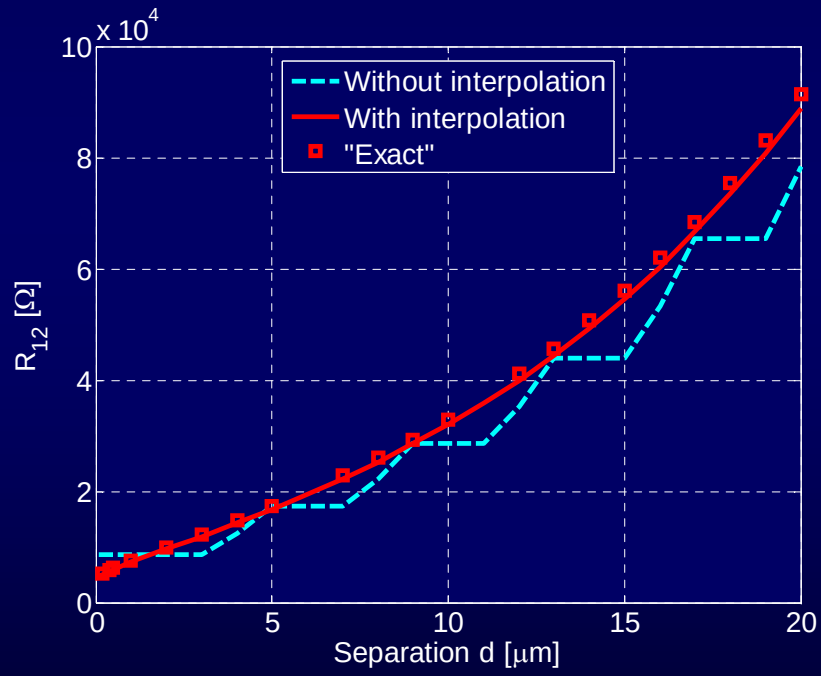
Lightly Doped Substrate

Error in Contact Separation Due to Rounding

- **Two identical contacts at different separations**



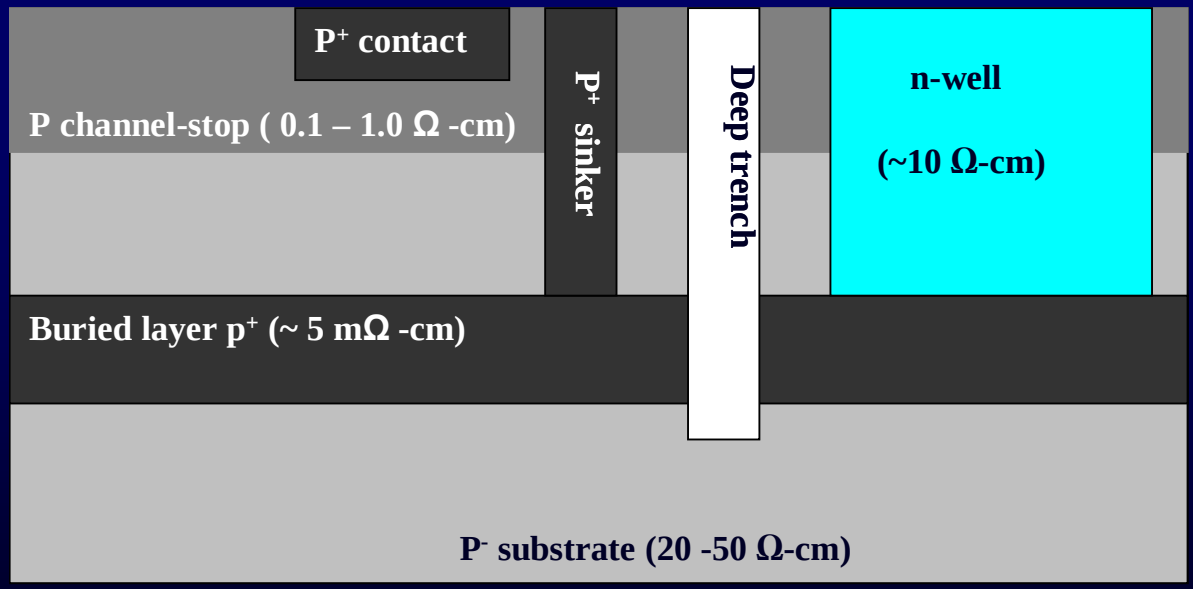
R_{11} as a function of contact separation



R_{12} as a function of contact separation

Inhomogeneous Substrate Layers

- **Homogeneous approximation not valid for sinkers, wells, and trenches**
- **Difficult to derive an analytical Green's function for complex substrate structures**



Cross section of typical BiCMOS process

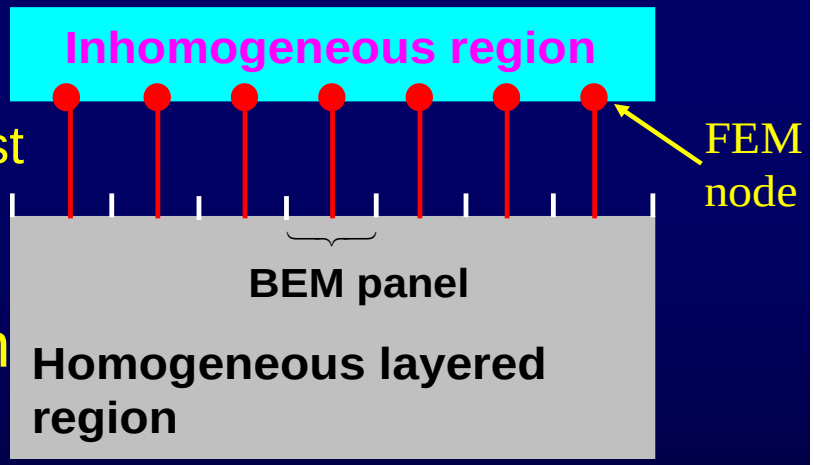
Combined FEM/BEM Method[+]

Basic idea

- ✓ Split substrate into two regions
  - ⇨ BEM for homogeneous region
  - ⇨ FEM for inhomogeneous region
- ✓ Reduced volume for FEM
  - ⇨ Reduced matrix size and CPU cost

Possible problems

- ✓ FEM for inhomogeneous region
  - ⇨ Large number of nodes
- ✓ BEM meshing of interface
  - ⇨ Large number of panels



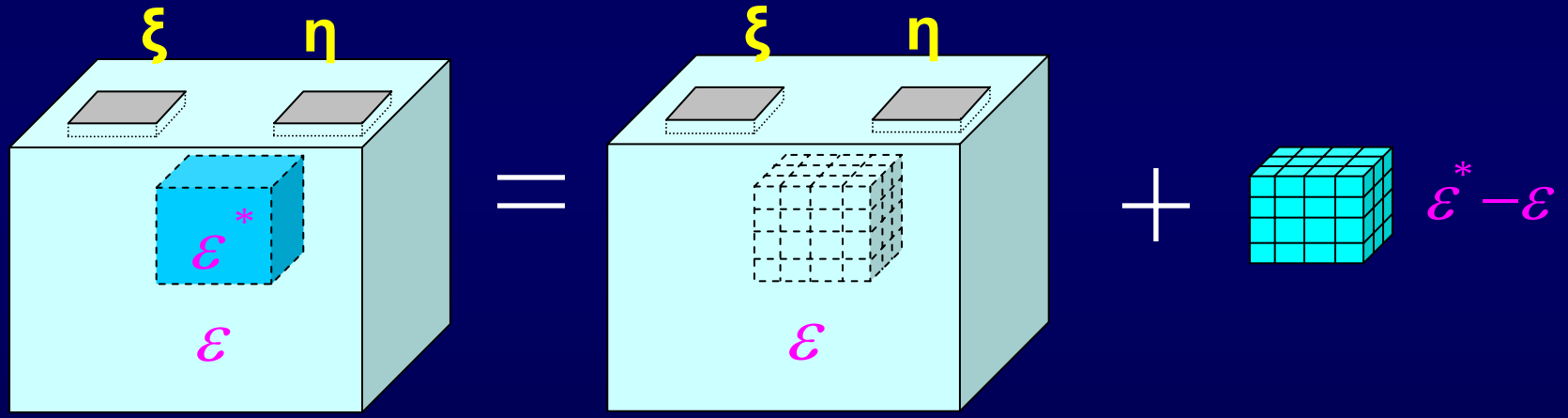
[+]**E. Schrik and N.R. van der Meijs, *Proc. 39th DAC*, 2002**

Lateral Inhomogenity Is Local

- **Sinkers, wells, and trenches are locally inhomogeneous regions**
- **Combined FEM/BEM methods ignore local inhomogenity**
- **Possible ways to reduce problem size**
  - ✓Reduce volume for FEM meshing
    - ⇨Constrain volume meshing to local regions
  - ✓Reduce area for BEM meshing
    - ⇨Constrain area for BEM meshing to surfaces of local regions

Two-Problem Approach[+]

Two contacts in a substrate with one local inhomogeneous region



Original problem local region permittivity ε^*

Homogenous substrate of permittivity ε

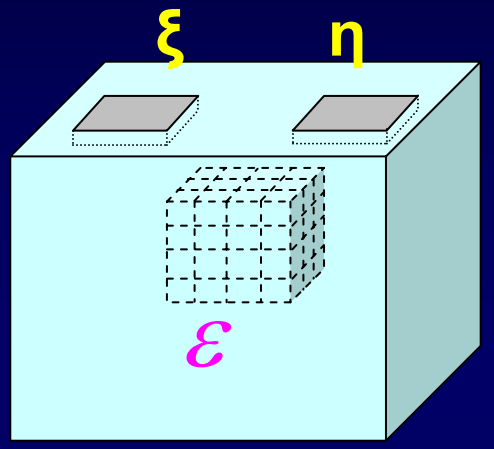
Companion region of permittivity $\varepsilon^* - \varepsilon$

[+]**R. Gharpurey, *Ph.D. Dissertation*, UC Berkeley, 1995**

Two-Problem Approach - Implementation

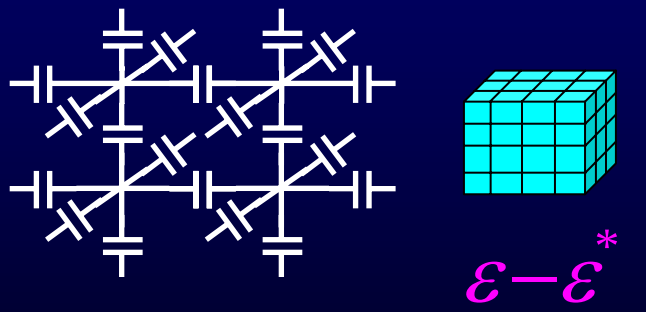
Problem 1:

- ✓ Insert ‘sockets’ for ‘plugging in’ parasitic circuit of companion region
  - ⇨ Virtual contacts for meshing local surfaces
- ✓ Extract the parasitics for real and virtual contacts



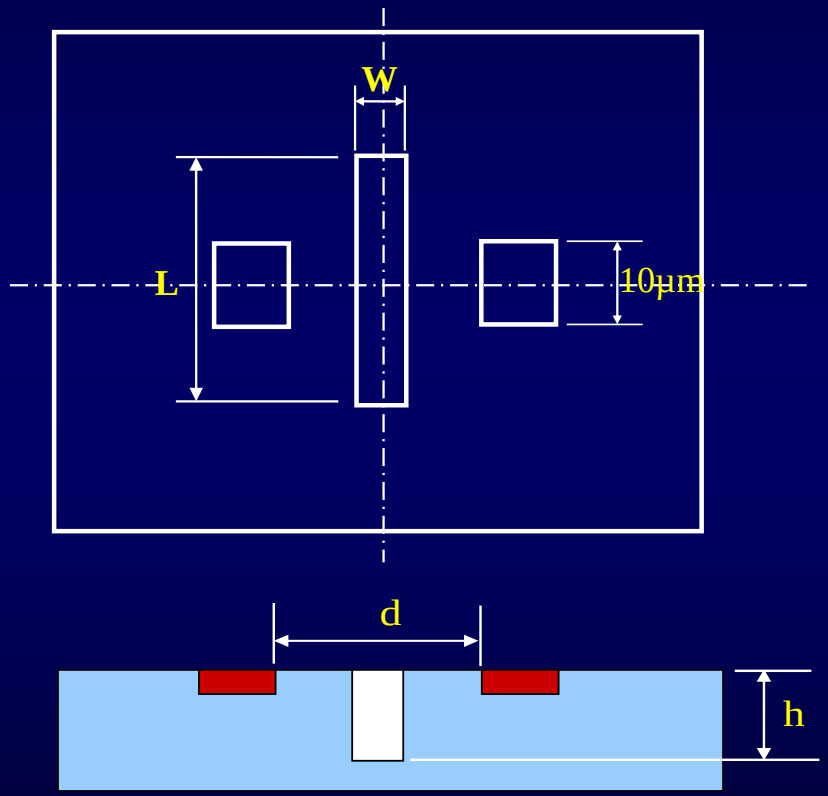
Problem 2:

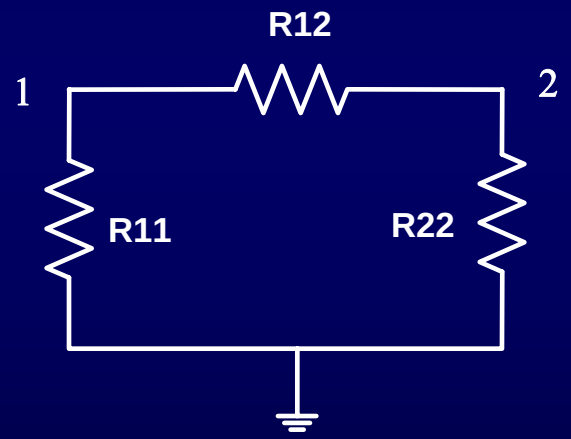
- ✓ Grid representation of companion region



Complete network obtained by ‘plugging’ network from Problem 2 into network for Problem 1

Two Contacts Separated by Trench



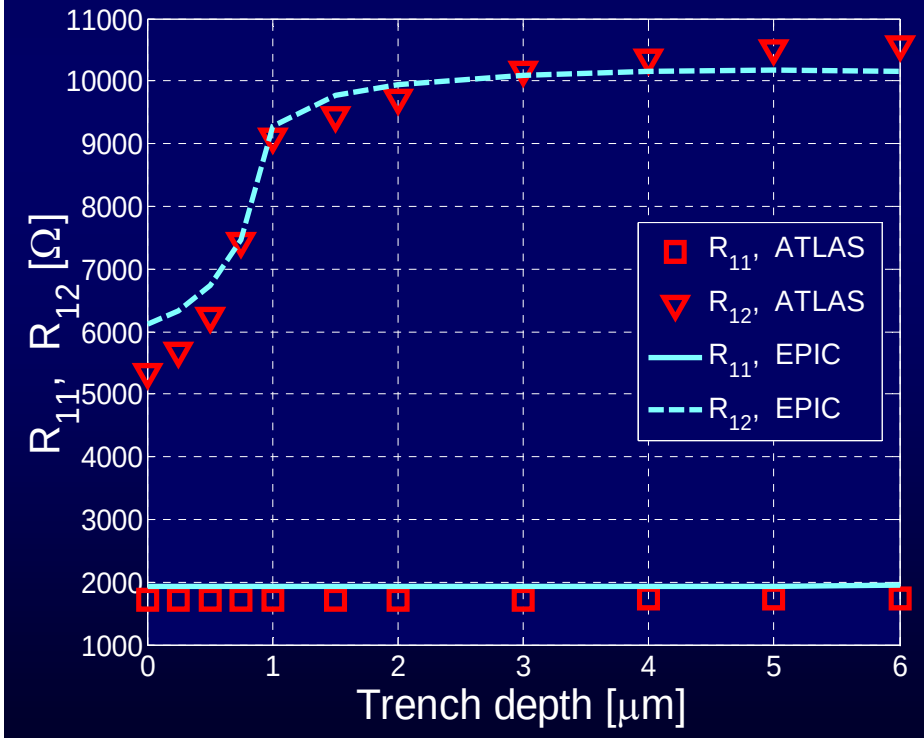


Two contacts and a trench

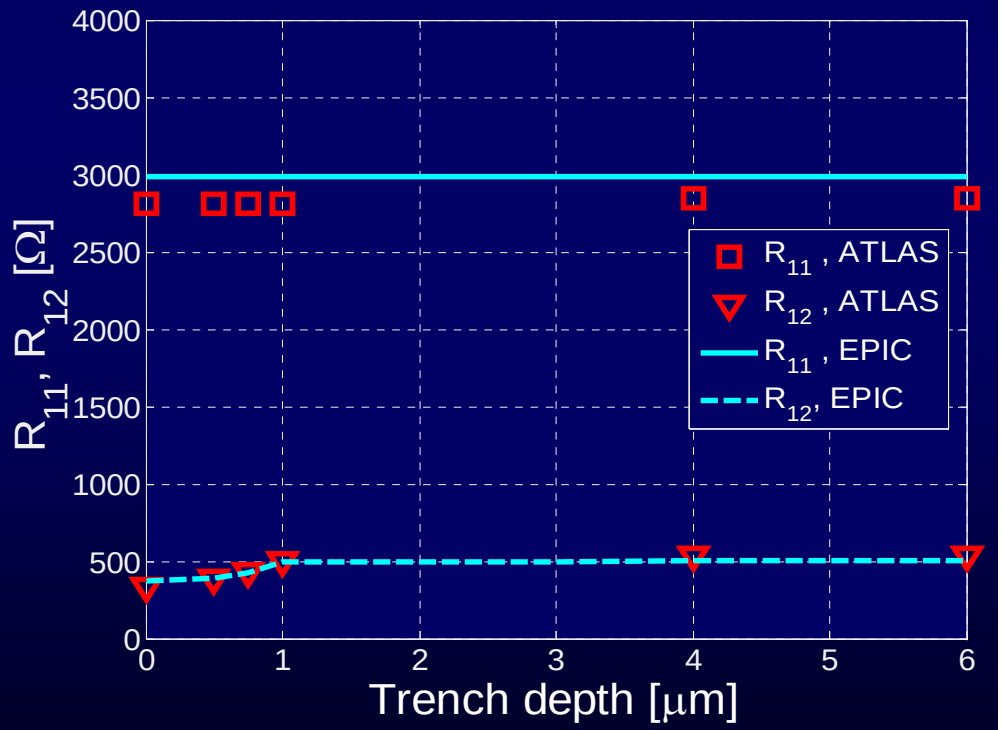
Equivalent circuit model

EPIC and ATLAS (3D Device Simulator) Comparisons

- **EPIC shows good agreement with ATLAS for both heavily and lightly substrates**



Heavily Doped Substrate

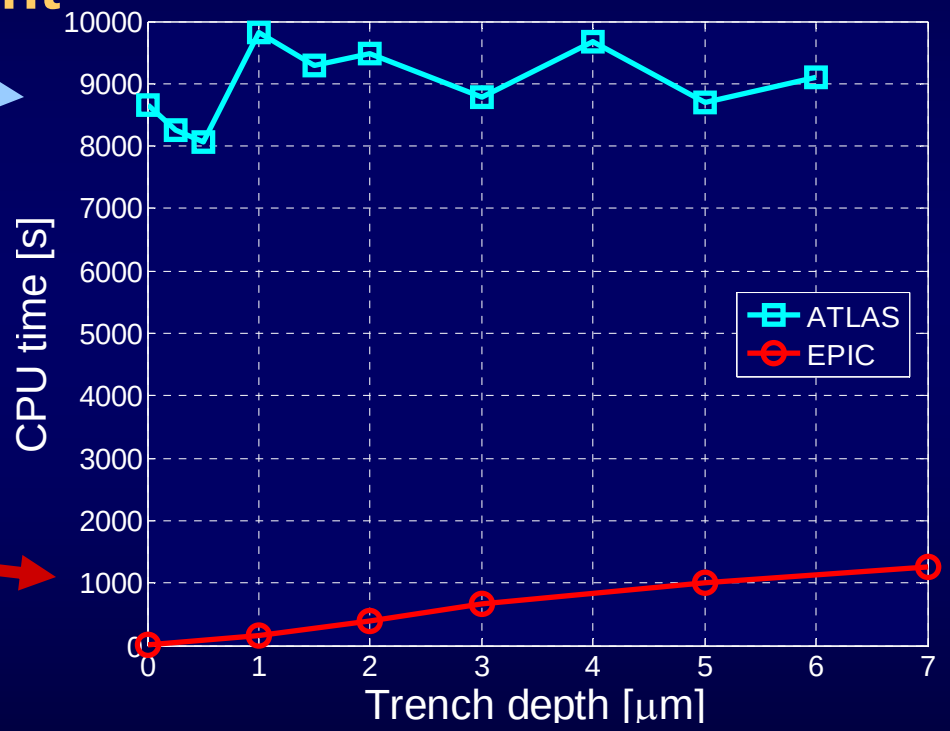


Lightly Doped Substrate

EPIC Orders of Magnitude Faster than Device Simulation

ATLAS CPU time independent of trench depth

EPIC CPU time increases with trench depth



Summary

- **Developed a two-problem approach for Green function based parasitic extraction with inhomogeneous substrate layers**
- **Numerical accuracy and efficiency verified with three-dimensional device simulation (ATLAS)**
  - ✓Accuracy to within 10% of ATLAS
  - ✓Orders of magnitude speedup over ATLAS

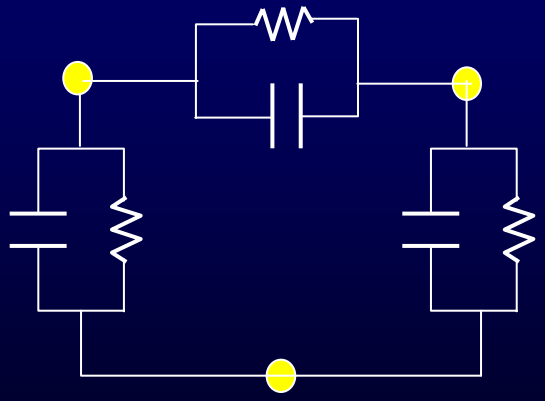
* **Nominated for best paper award at DAC'05**

Components of Silencer!

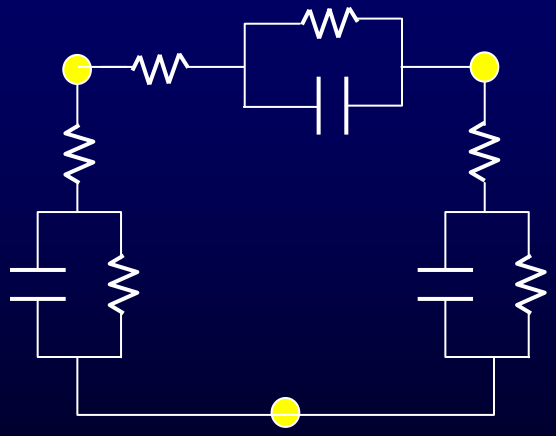
High frequency substrate models

Previous High Frequency Analysis

- **High frequency coupling behavior and models**
  - ✓ Capacitive behavior [R. Gharpurey,1997]
  - ✓ Inductive behavior [H. Li, et. al, 2002]
  - ✓ Equivalent circuit models [H. Lan, 2003]

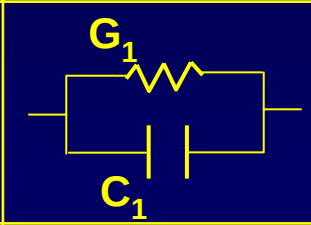
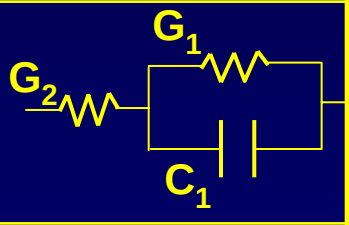
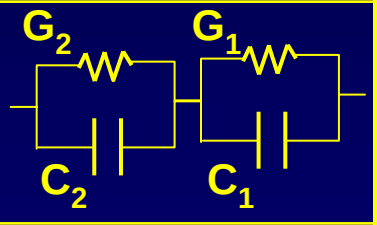


Model I



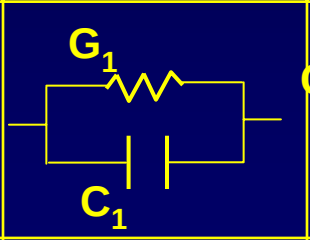
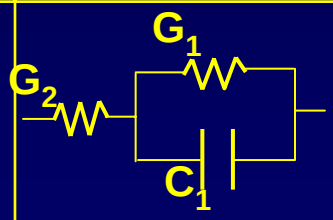
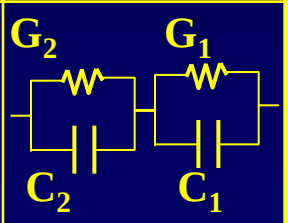
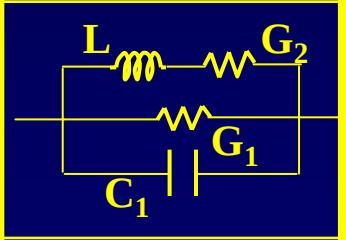
Model II

Self Admittance Models

	Model 0	Model I	Model II	Model III
Circuit				
Suitable frequency range	*f* < 1 GHz	1 G < *f* < 5 G	5 G < *f* < 10 G	*f* > 5 GHz
Comments	Simplest low frequency model	Cannot model the frequency dependence of G	Models the frequency dependence of G and B	Similar to Model II but with better agreement with simulations

- Model 0 through Model II are existing models
- Model III proposed new model

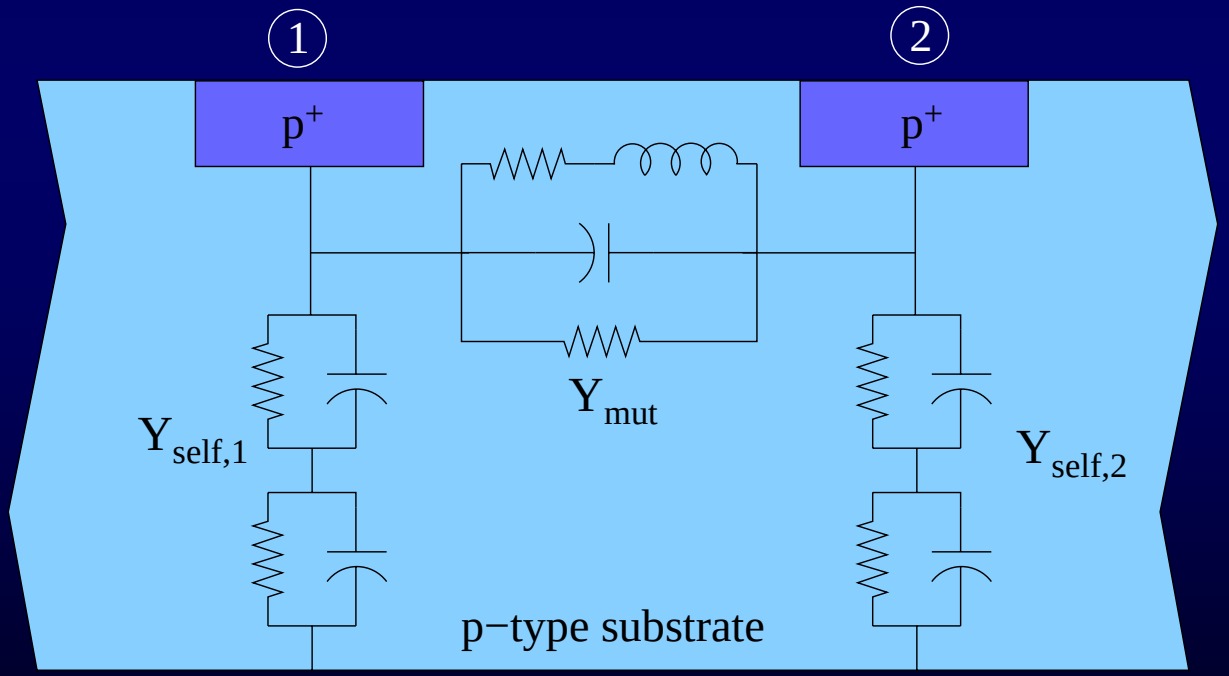
Mutual Admittance Models

	Model 0	Model I	Model II	Model III	Model IV
Circuit					
Suitable frequency range	*f* < 1GHz	1 G < *f* < 5 G	5 G < *f* < 10 G	*f* > 5 GHz	*f* > 1GHz
Comments	Simplest low frequency model	Cannot model the frequency dependence of G. Capacitive coupling only	Models the frequency dependence of G and B. Capacitive susceptance	Similar to Model II but with better agreement with simulations	Suitable for both capacitive and inductive coupling. Very good agreement with simulations

- Model 0 through Model III are existing models
- Model IV proposed new model

High-Frequency Substrate Model

- **Above 2 GHz, account for reactive nature of the substrate**



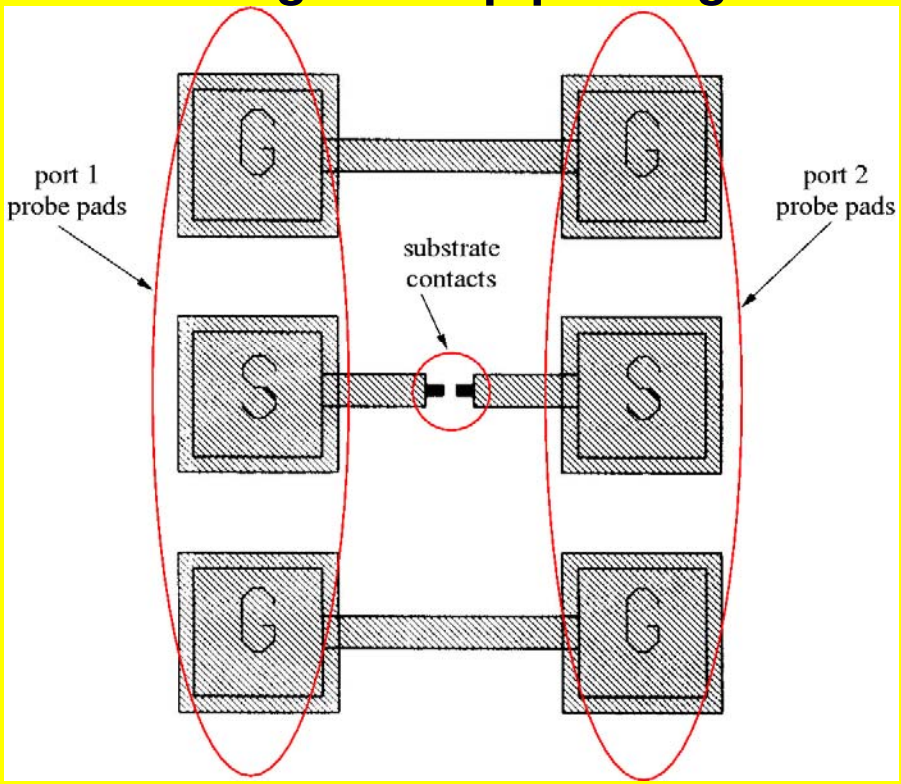
Xu et al., BMAS ’03

Substrate Characterization

- **Low frequency – below 1-2 GHz**
  - ✓Resistive substrate models
  - ✓Validate with DC measurements
- **High frequency – above 2 GHz**
  - ✓Reactive substrate models
  - ✓Network analyzer measurements
    - ⇨Careful test fixture and measurement, deembedding procedure required

Problem with On-Chip Probing

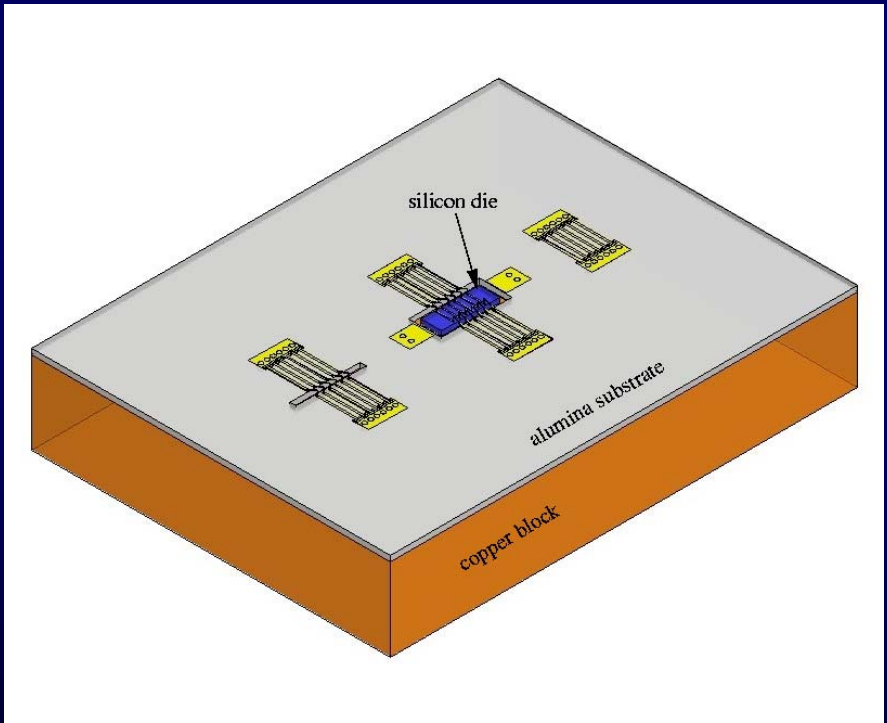
Typical substrate test structure using on-chip probing



- **Probe grounds define reference nodes for ports**
  - ✓ Probe grounds connect only to each other
  - ✓ Poorly defined ports
  - ✓ Interactions with probe station chuck
- **Models assume die back side is reference node**
  - ✓ Probe grounds should connect to back side

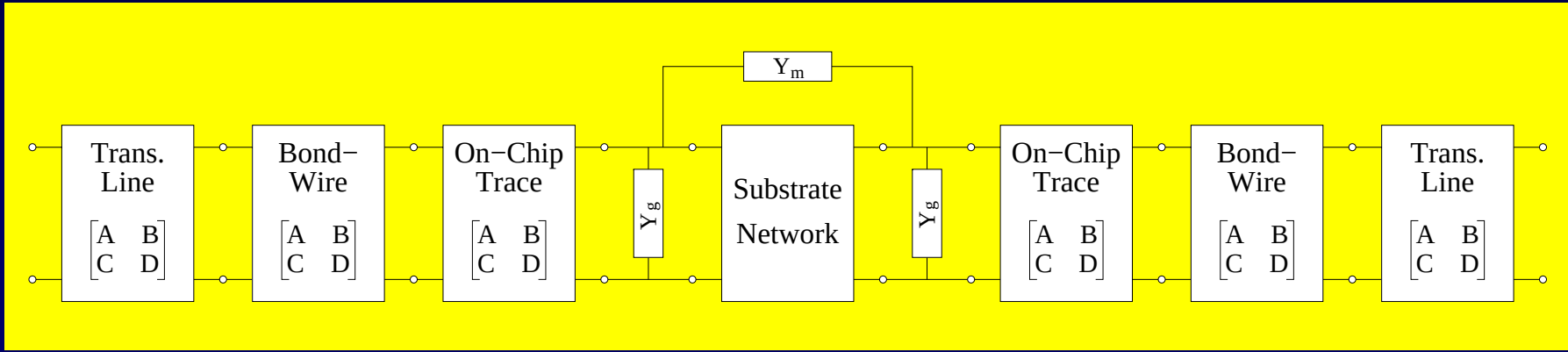
Test Fixture Using Off-Chip Probing

- **Off-chip probing**
  - ✓Die back side is measurement system ground



- **Ceramic substrate**
  - ✓Bondwire and micro-strip characterization structures
- **Test chip**
  - ✓4 substrate structures
  - ✓2 deembedding structures
- **Copper block**

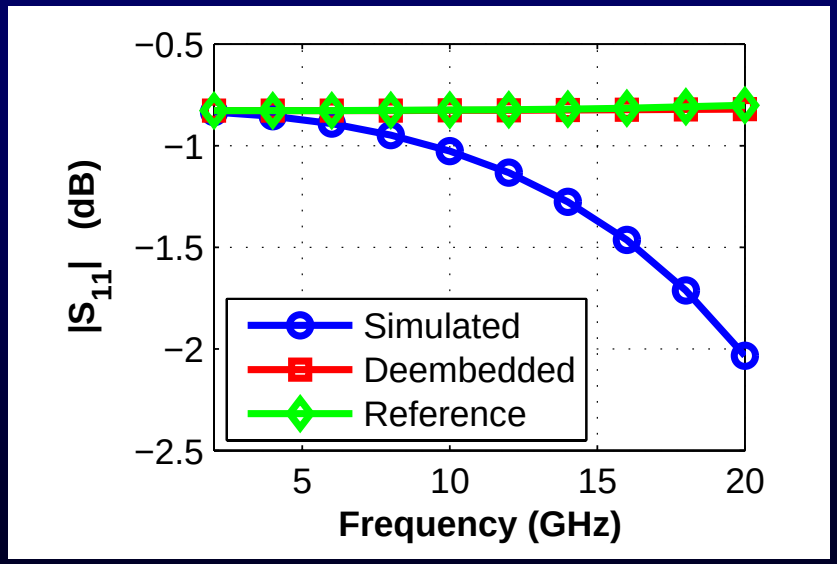
Four-Step Deembedding Procedure

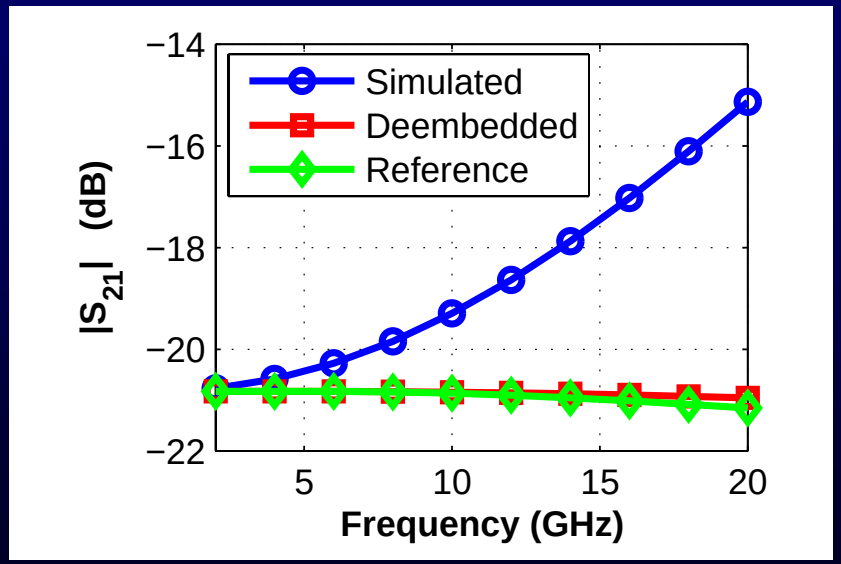


- **Four blocks of test fixture parasitics**
  - ✓ Micro-strip transmission lines
  - ✓ Bond wires
  - ✓ On-chip traces
  - ✓ Shunt admittances
- **Characterize blocks then deembed in four steps**

HFSS Simulations

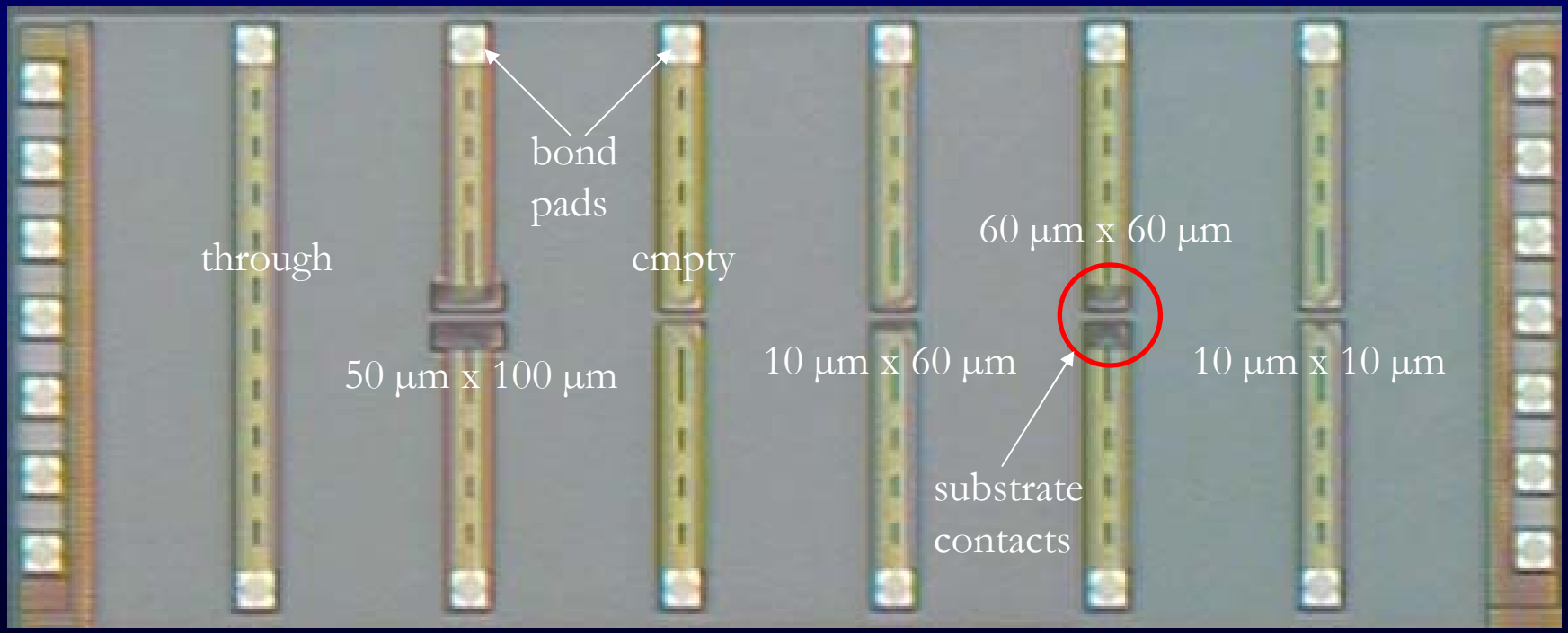
- **Simulations aided the design of the test fixture and deembedding procedure**
- **S-parameters of 1KΩ resistor in the test fixture**



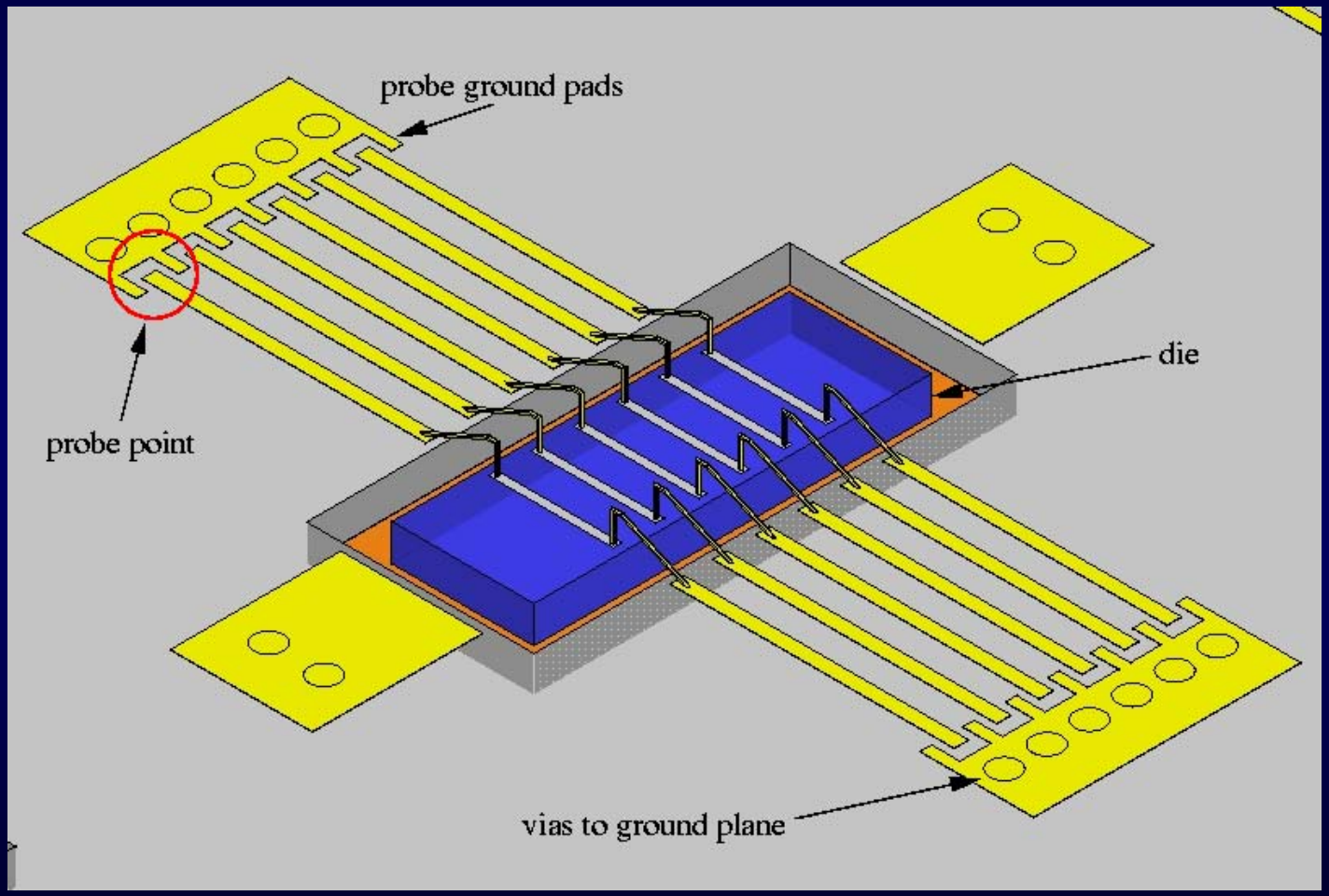


Test Chip

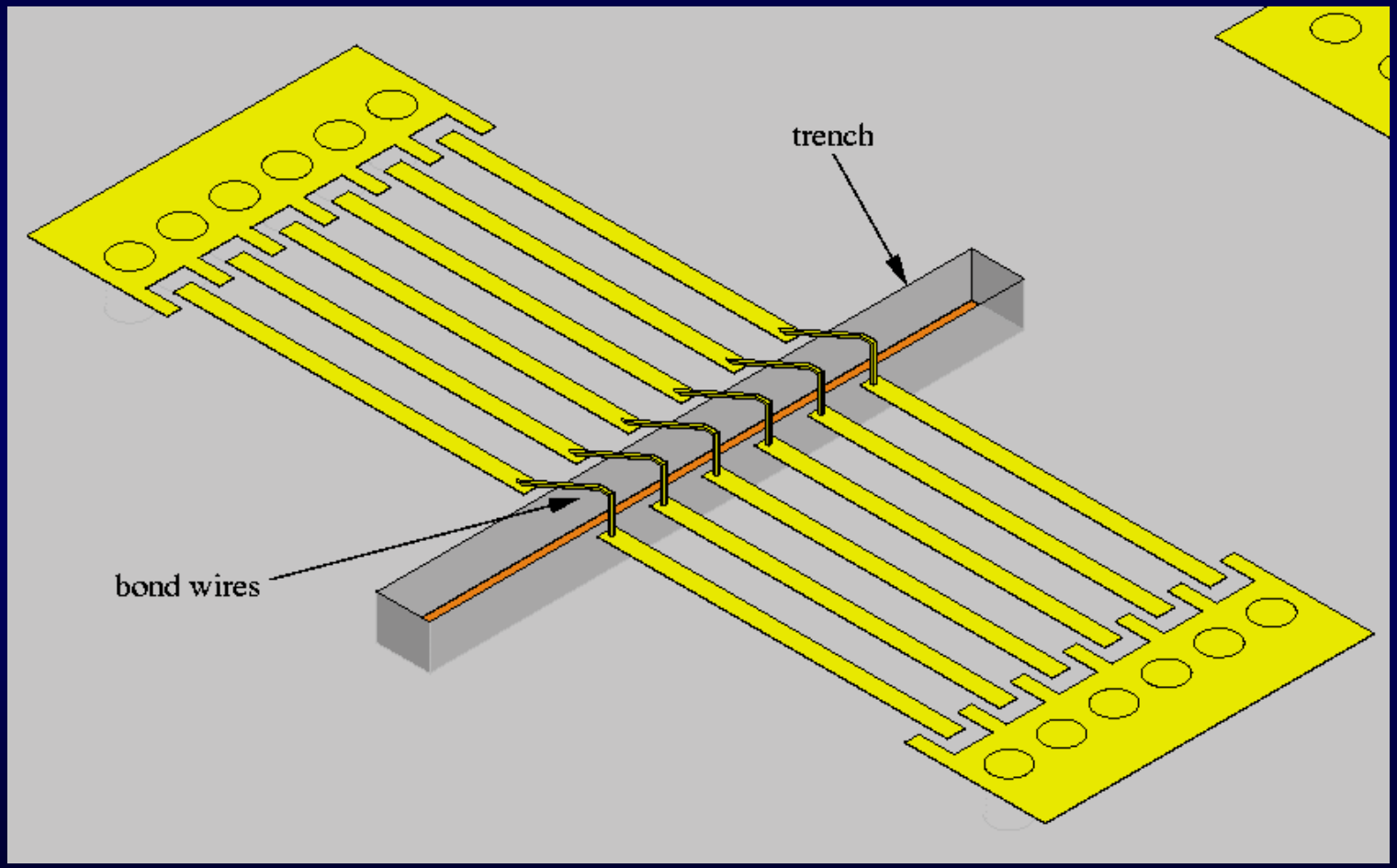
- **TSMC 0.35 µm CMOS process**



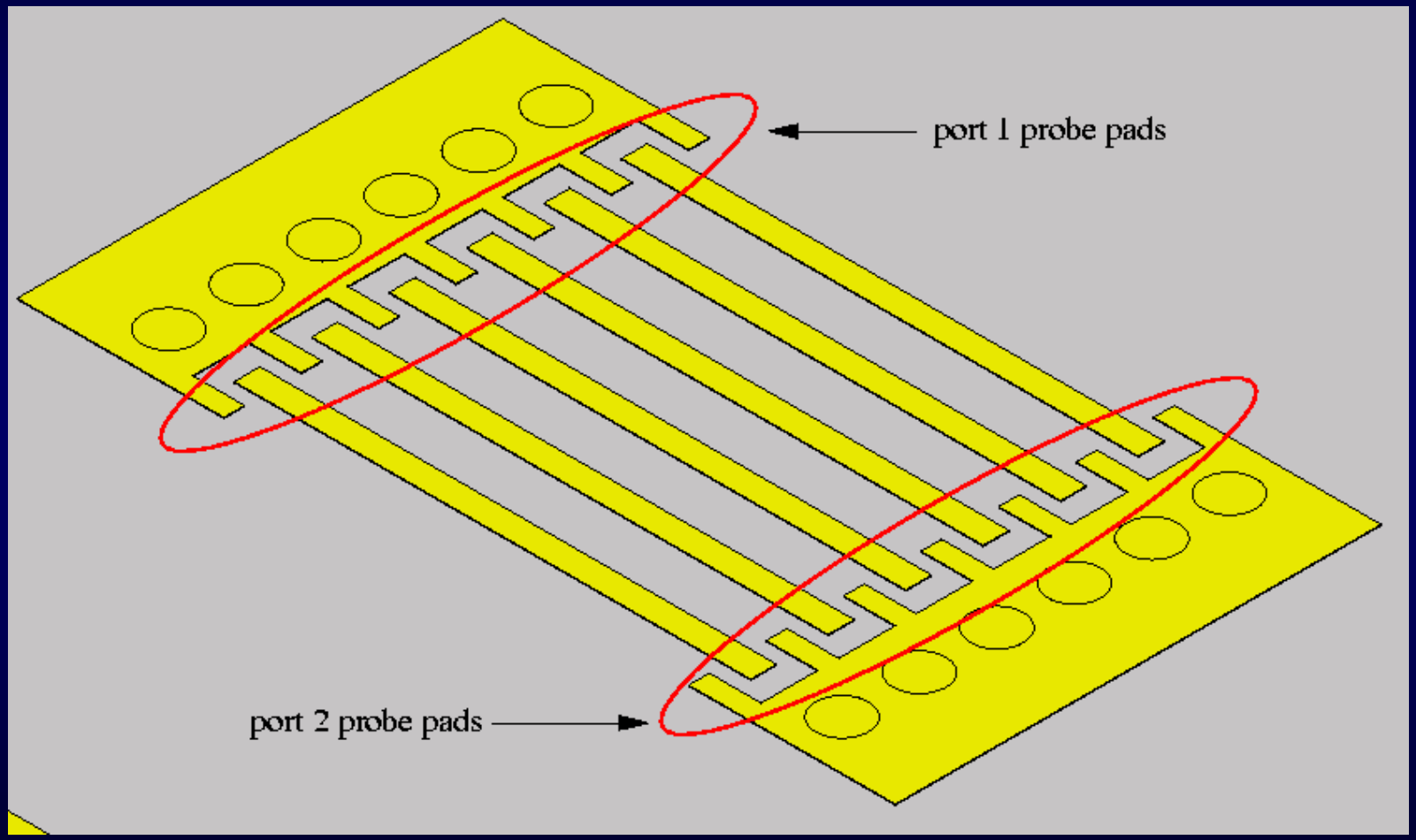
Ceramic Substrate



Bond Wire Characterization Structure

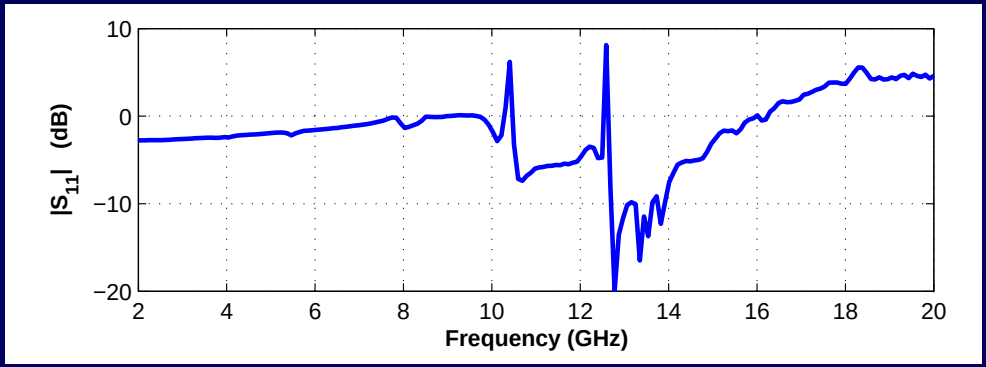


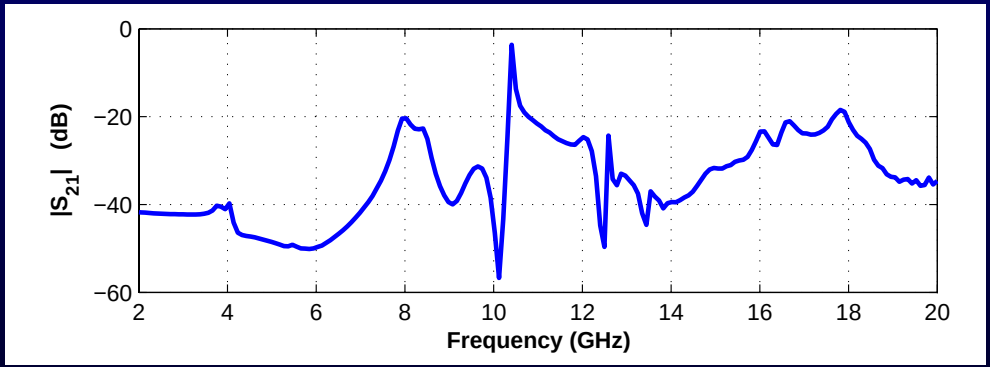
Transmission Line Characterization Structure



Measurement Results

- **Initial measurements show the failure of the test fixture and deembedding approach**

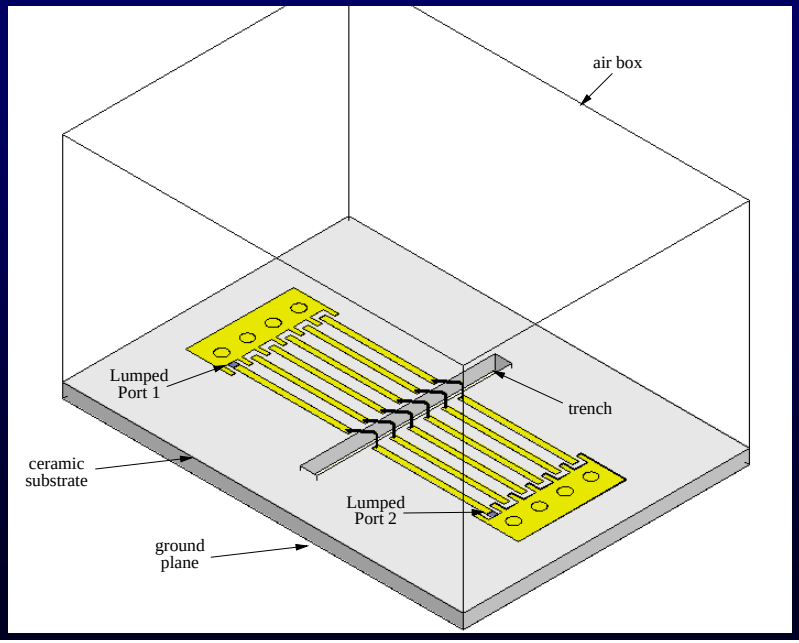


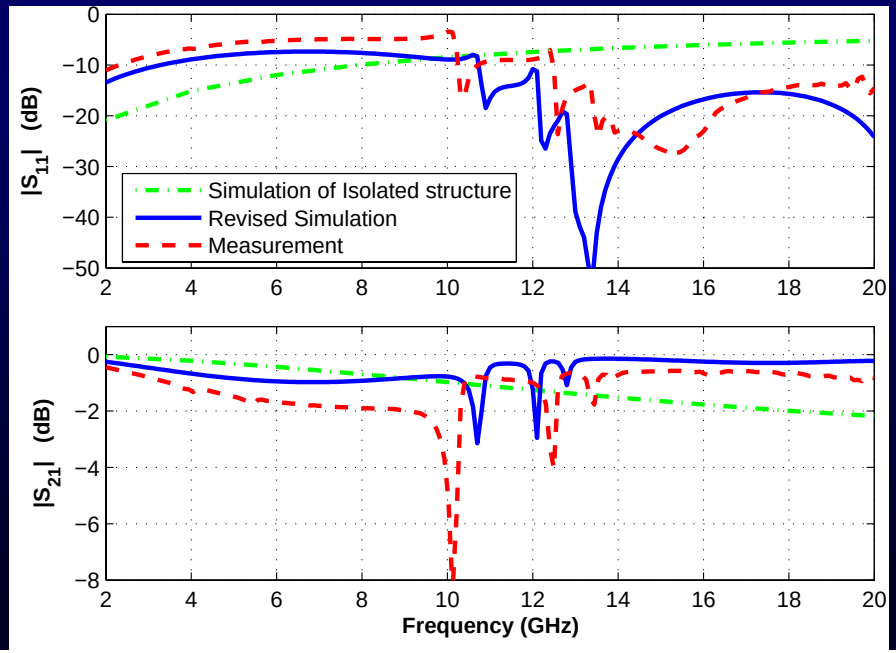


- ✓|S11| > 0 dB
- ✓Resonances indicate coupling mechanisms neglected in test fixture model and simulations

Updated Simulations

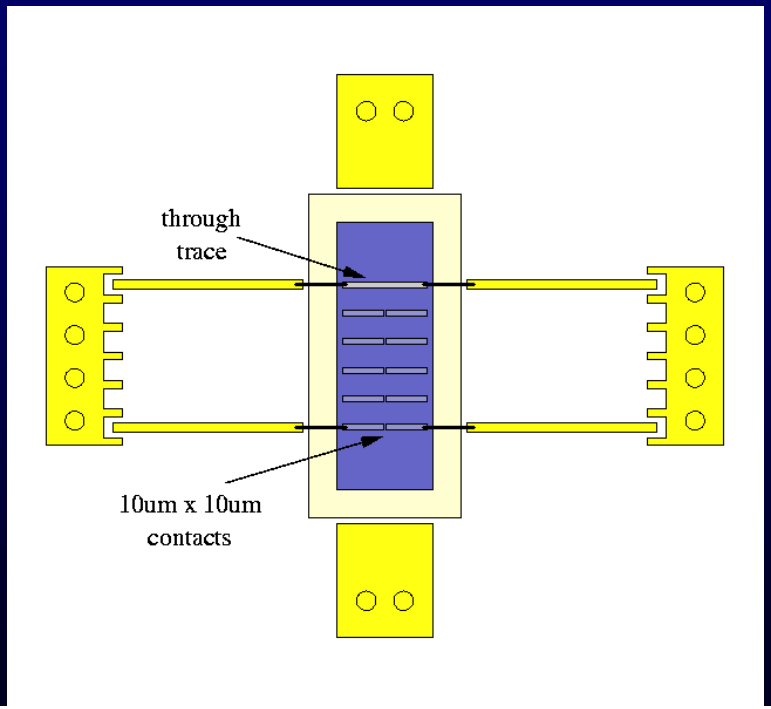
- **Simulate entire test structure**
- **Fair agreement between simulation and measurements**

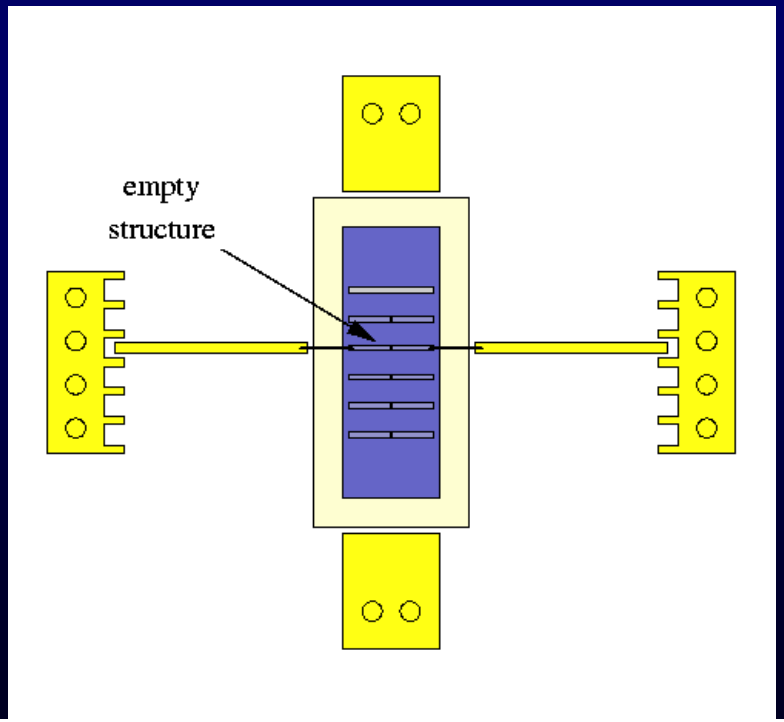




Test Fixture Modifications in Progress

- **Use two test fixtures for one substrate measurement**





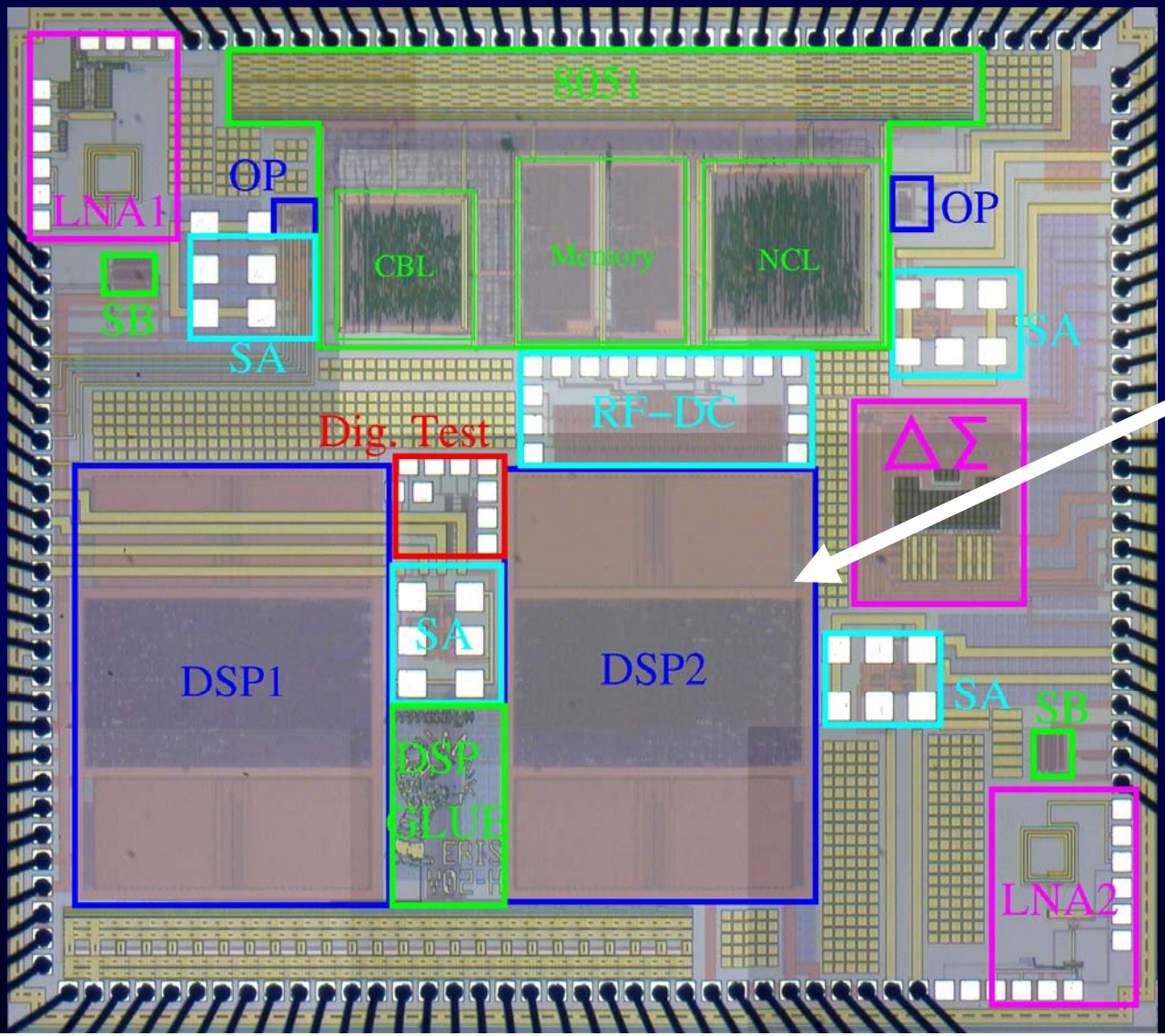
Components of Silencer!

Efficient digital noise simulation

Implementation of Digital Noise Analysis Flow in Silencer!

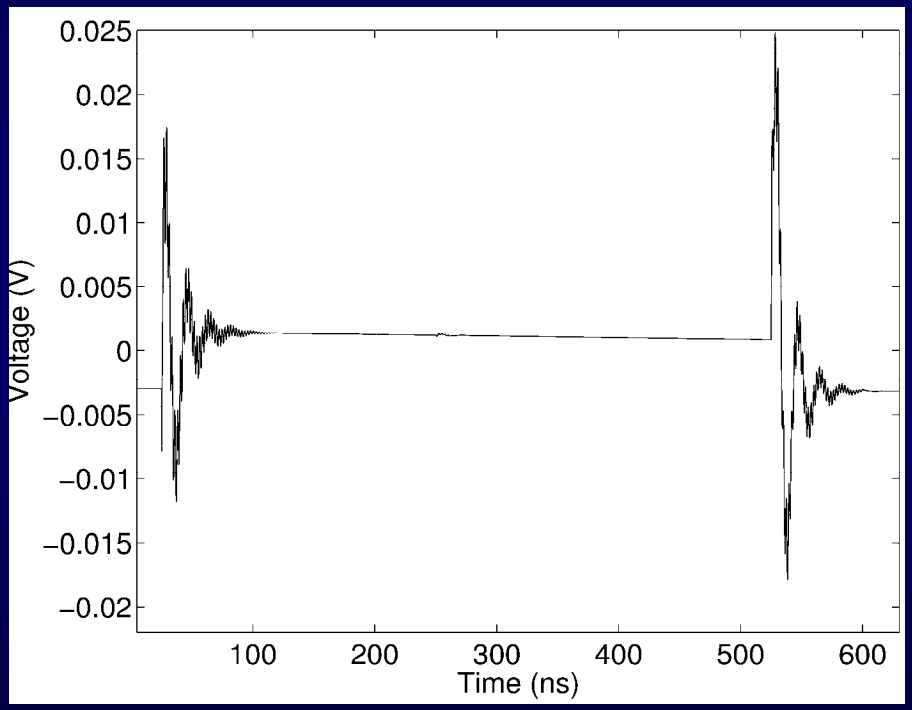
- **Integrated into Cadence DFII**
- **Uses Mentor Graphics ModelSim for digital simulation**
- **Custom C programs for noise generation**
- **Spectre for library generation and top level simulation**
- **Unix scripts for file processing**

Test Chip for Measurement Validation
0.25μm CMOS process

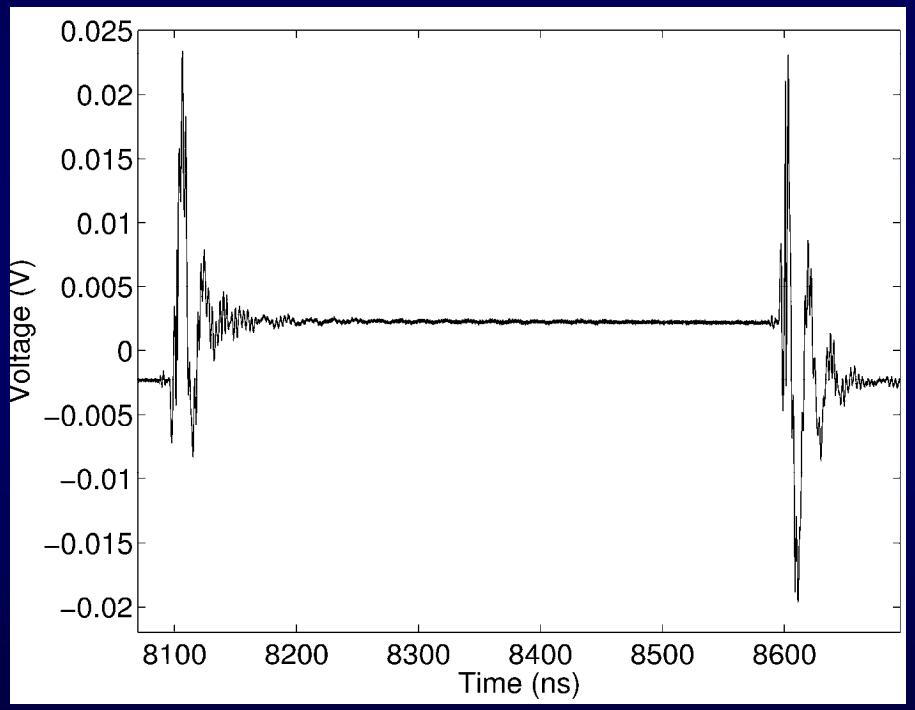


500,000 Transistor DSP

Good Agreement Between Simulation and Measurement Results



Simulation



Measurement

Computation Requirements

	Execution Time
One Step Methodology	204 hours
Silencer! Methodology	2.5 hours
Gate level simulation	2 hours
Vector Generation	25 minutes
Top level SPICE	5 minutes

Comprehensive Approach to Substrate Noise Coupling