Modeling and Analysis for Substrate Noise Mitigation in High Frequency Integrated Circuits

CADTS LPD Review

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Task ID: 1299.001 (Cont. of 911)

Technical Thrust:	**Physical Design**
Task Leaders:	**Karti Mayaram and Terri Fiez**
Students:	Matt MacClary (M.S., Dec 2006) Andrew Tabalujan (M.S., Aug 2007) Jacky Wong (Ph.D., Dec 2009) Arathi Sundaresan (M.S., Aug 2006) Cheng-gang Xu (Postdoc, now at IBM)
Industrial Liaisons:	James Falbo (Mentor) Ravi Naiknaware (Intel)
Anticipated Result:	An overall design-oriented approach for substrate noise analysis and planning in high frequency mixed-signal ICs. This will include developing substrate models for high frequencies, identifying efficient approaches for simulation of substrate noise, and developing and validating isolation strategies.

Task Deliverables

- Report on the frequency behavior of substrate coupling for both heavily and lightly doped substrates (Completed)
- Report on the development of accurate scalable equivalent circuit models for multi-gigahertz applications (Planned: 31-Mar-2007)
- Report on the design of test structures for extraction of parameters for the substrate coupling models (Planned: 31-Aug-2007)
- Report on the model validation with silicon measurements and incorporation into the Silencer! tool framework (Planned: 31-Mar-2008)

Task Description

The focus of our work is on management of substrate noise early in the overall design flow as well as techniques for mitigating the noise. In our approach, a scalable model simplifies the overall approach so that the designer can incorporate simple networks into their design. In addition, we have developed a Green's function solver that will be used for a detailed examination of the silicon substrate behavior over frequency. Our preliminary simulation results point out the need for use of different types of equivalent circuit models for the self and mutual-coupling admittances. These results will be verified with fabricated test structures. The equivalent circuit representations will be extracted from the measured data. Once the frequency dependence and the equivalent circuit models have been modified, development of scalable models will take place. We will use numerical simulations to understand the complete parameter space and develop appropriate functional dependencies for the coupling impedances.

Executive Summary

- **Accomplishments during the past year**
  - ✓ Extended efficient Green's function formulation for inhomogeneous substrate layers for high frequencies
  - ✓ Extending Green's function solver for n-wells
  - ✓ Developed macromodel for lightly doped substrates
  - ✓ Developed tool for automatic model parameter extraction
  - ✓ Evaluated the impact of ground tap sizing for a RF LNA

Executive Summary

- **Future direction**
  - ✓Characterize frequency behavior of substrate coupling for silicon substrates with improved test structures
  - ✓Develop accurate scalable equivalent circuit models for multi-gigahertz applications
  - ✓Validate model with silicon measurements and incorporate into the Silencer! tool framework

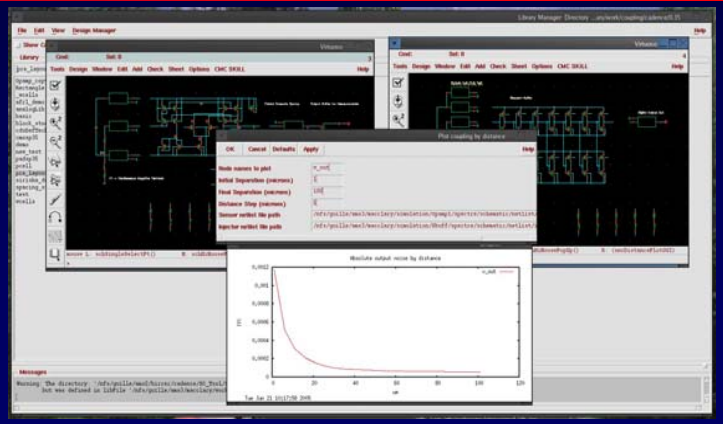
Executive Summary

- **Technology transfer & industrial interactions**
  - ✓ Discussions with Intel
- **Publications**
  - ✓ S. Hazenboom, T. S. Fiez, and K. Mayaram, “A comparison of substrate noise coupling in lightly and heavily doped CMOS processes for 2.4GHz LNA's,” *IEEE J. Solid-State Circuits*, pp. 574-587, March 2006.
  - ✓ C. Xu, T. Fiez, and K. Mayaram, “An error control method for application of the discrete cosine transform to extraction of substrate parasitics in ICs,” *IEEE Trans. Computer-Aided Design*, pp. 932-938, May 2006.
  - ✓ A. Sundaresan, T. Fiez, and K. Mayaram, “Sizing ground taps to minimize substrate noise coupling in RF LNAs,” *CICC 2006*, pp. 729-732, Sept. 2006.
  - ✓ P. Birrer, S. K. Arunachalam, M. Held, K. Mayaram, and T. S. Fiez, Schematic-driven substrate noise coupling analysis in mixed signal IC designs,” accepted *IEEE Trans. CAS-I*, 2006.
- **Patentable inventions, patent applications**
  - ✓ None

Comprehensive Approach to Substrate Noise Coupling & Suppression

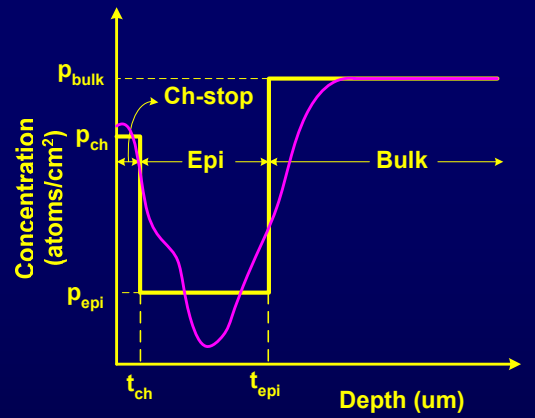
Design & Analysis

Tools



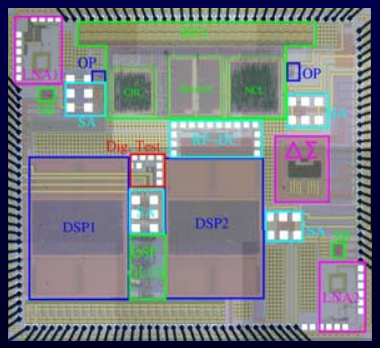
Fast & Accurate Noise Prediction

Models

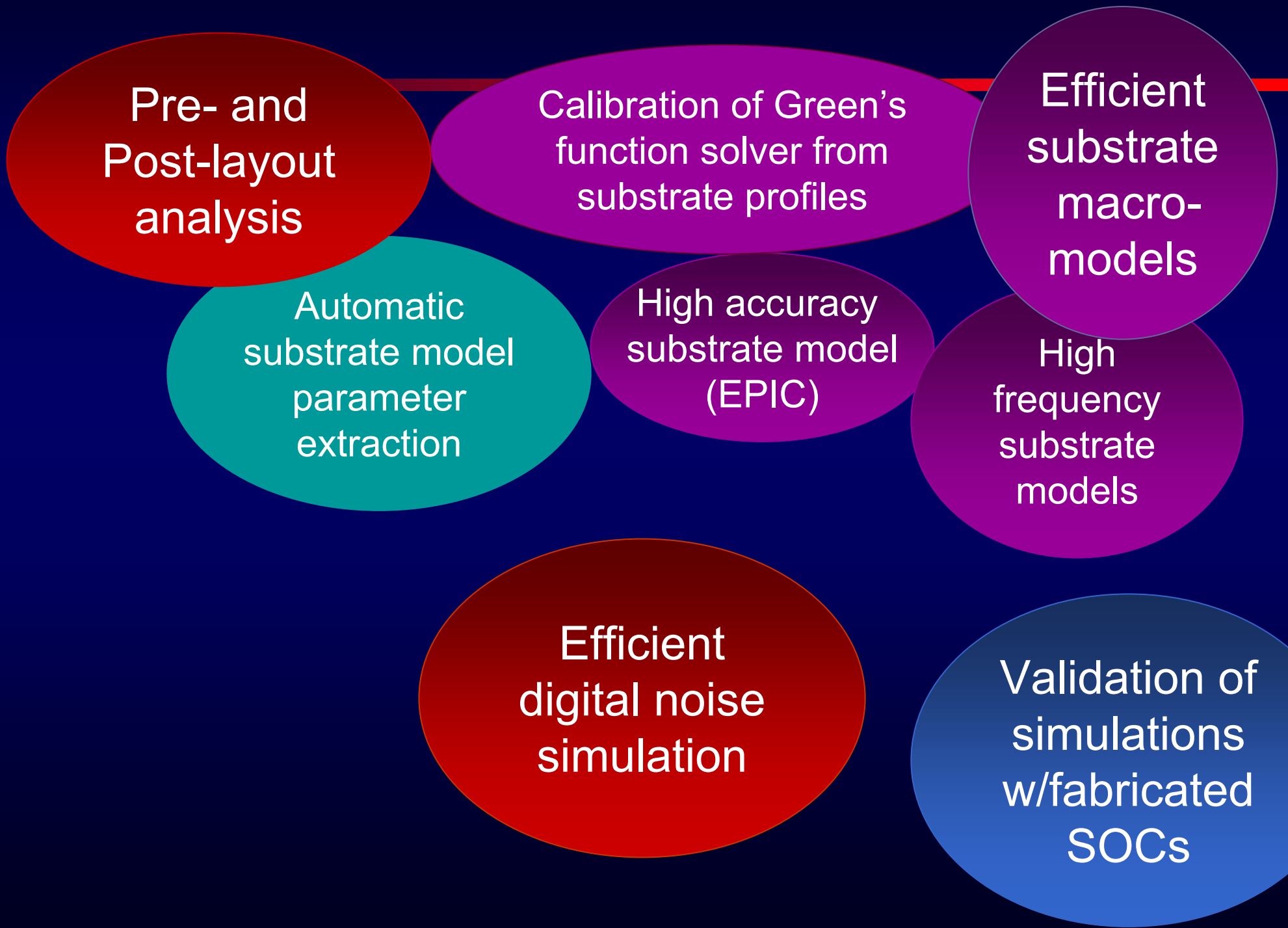


Noise Reduction

Designs



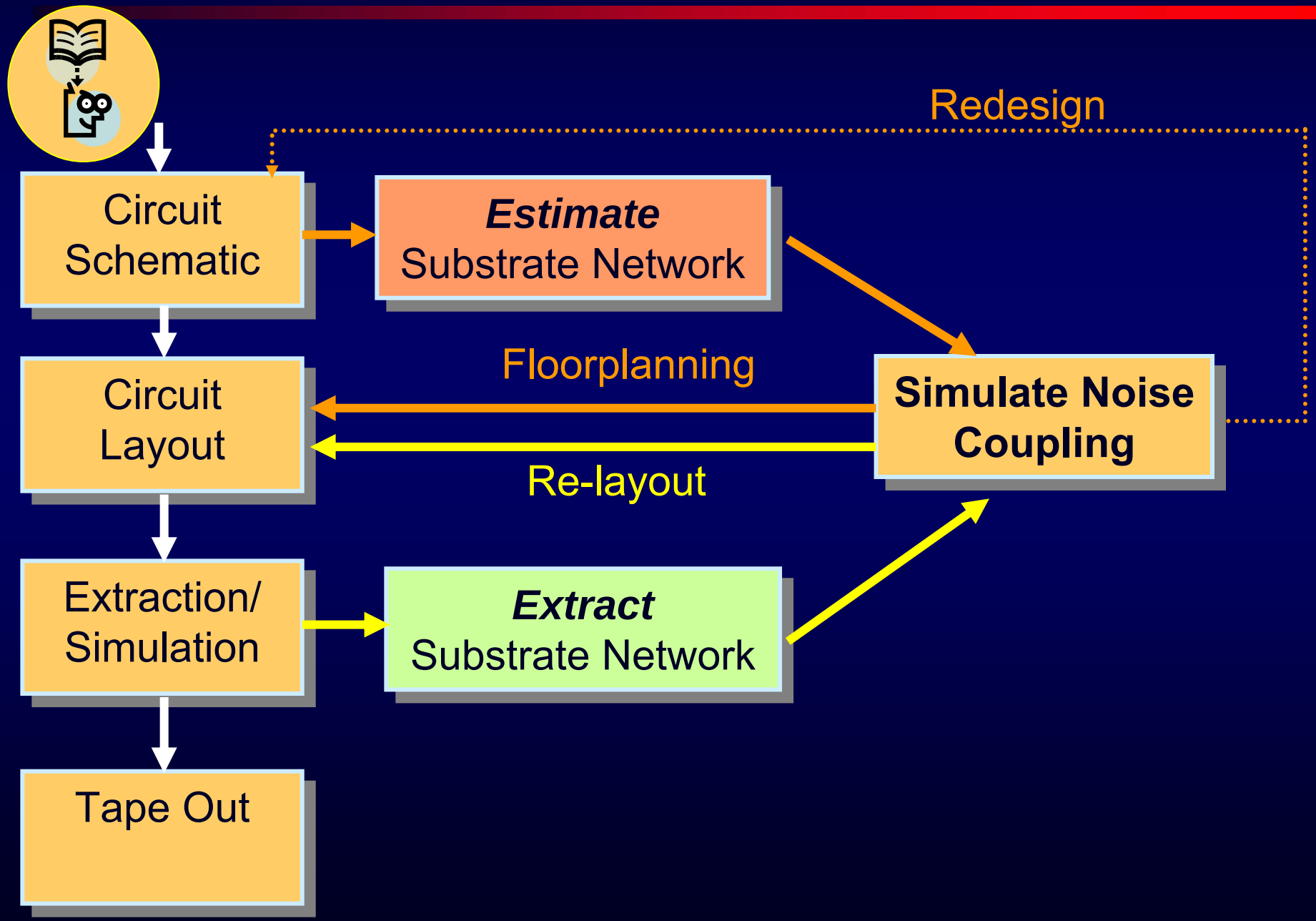
Components of Silencer!



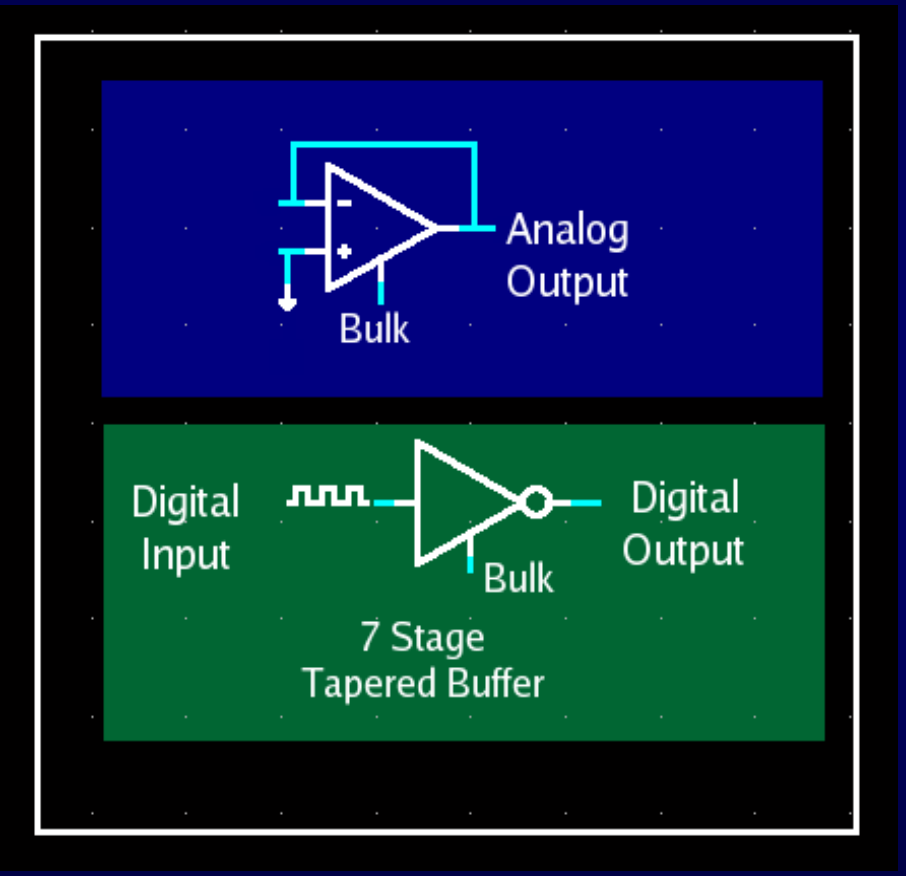
Silencer!
Substrate Noise Coupling Tool

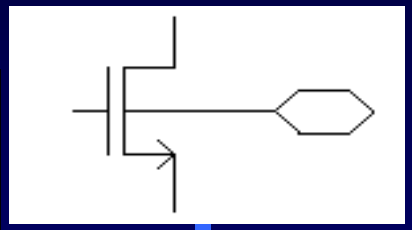
- **Post layout analysis**
- **Designer driven pre-layout floor planning**

Substrate Noise Coupling in Design Flow

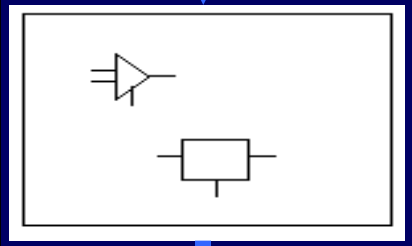


Using Schematic Symbols Silencer! Estimates Coupling



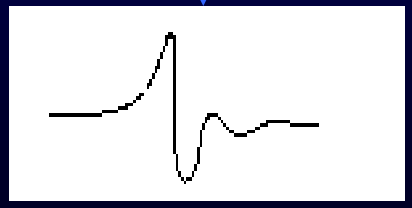


Connect transistor bulks to pin



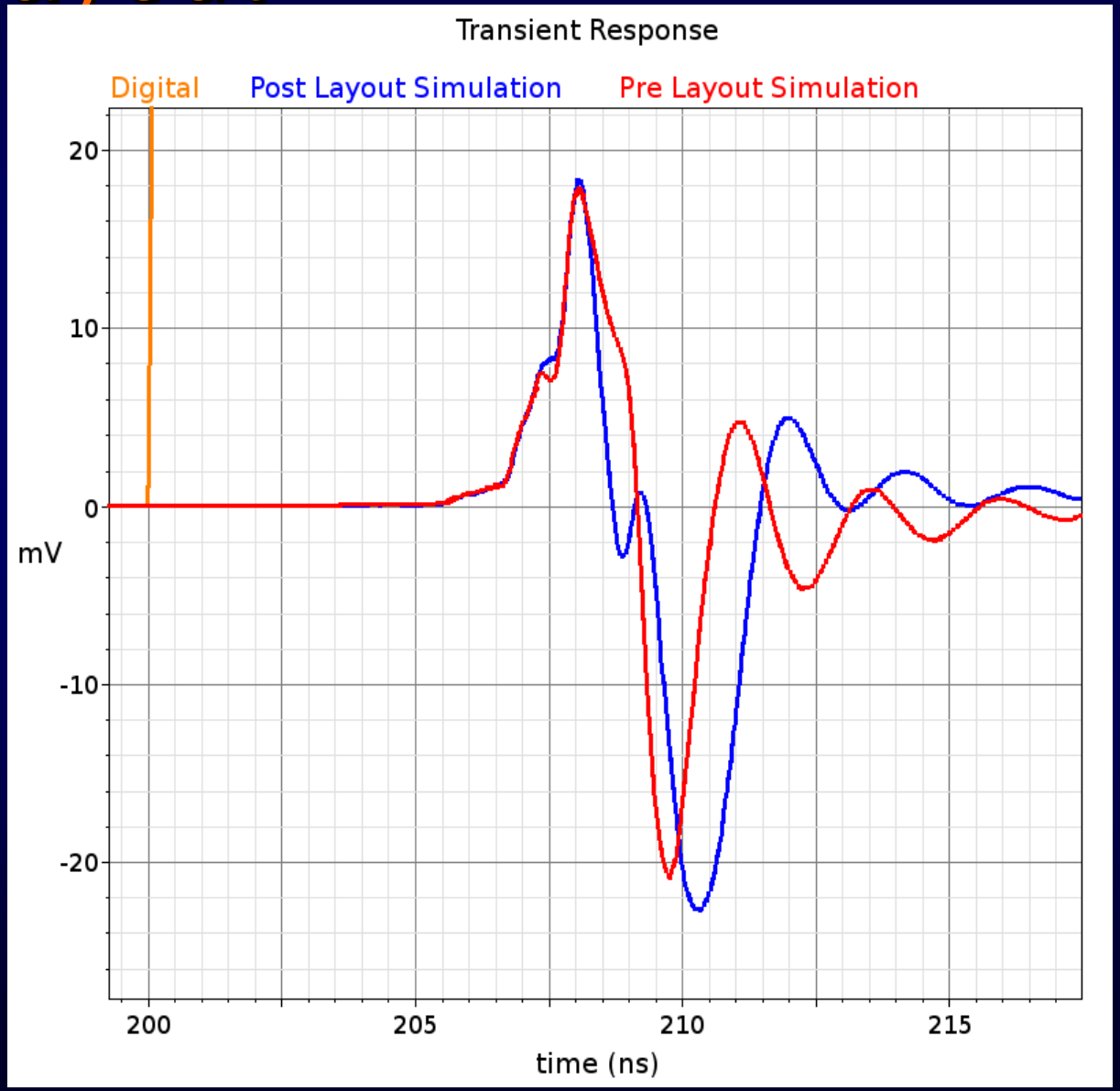
Position circuit symbols within “chip” symbol

Silencer! adds resistors to model substrate

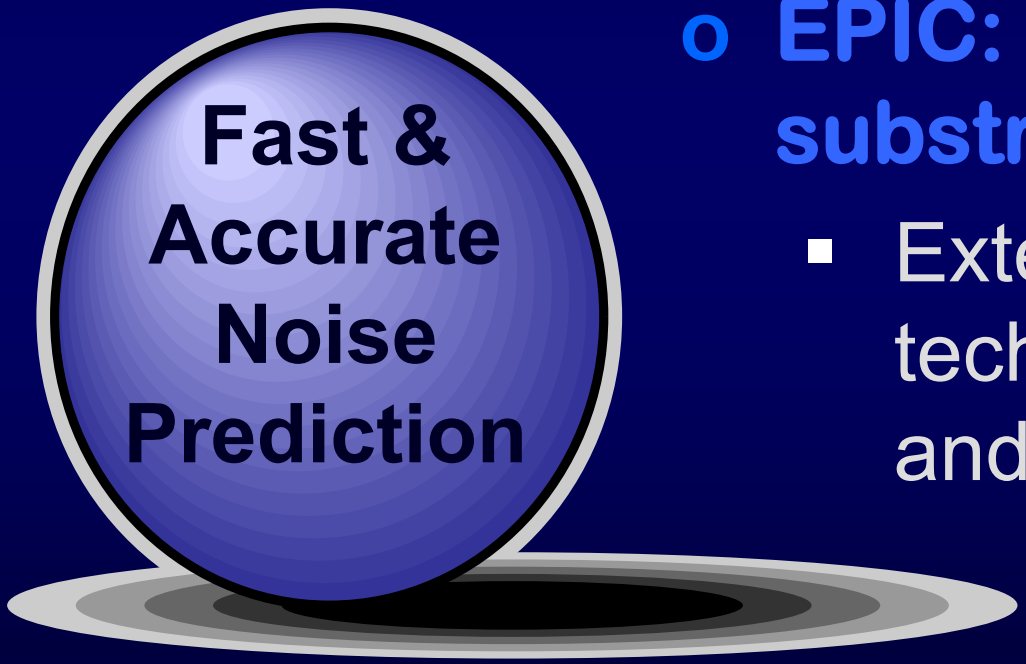


Simulate in Cadence

Schematic Simulation of Substrate Coupling runs 11X Full Layout



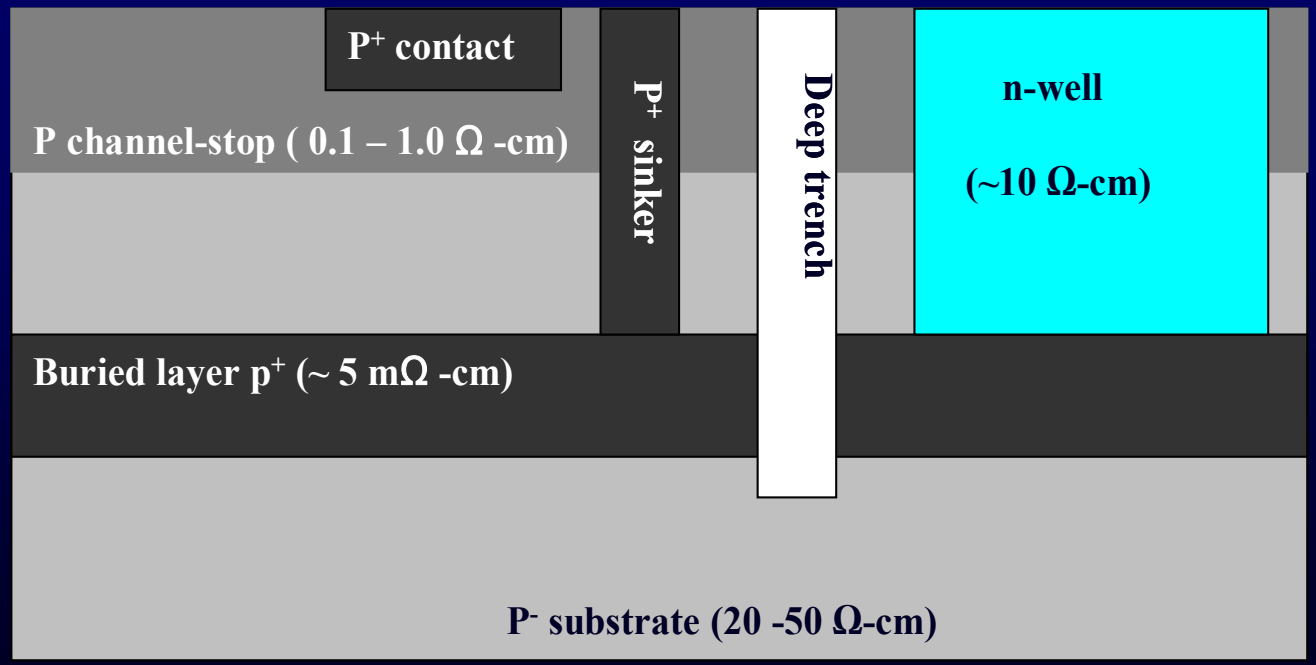
Models for Substrate Parasitics



- **EPIC: Green's function-based substrate parasitic extractor**
  - Extended inhomogeneous layer technique to high frequencies and n-wells

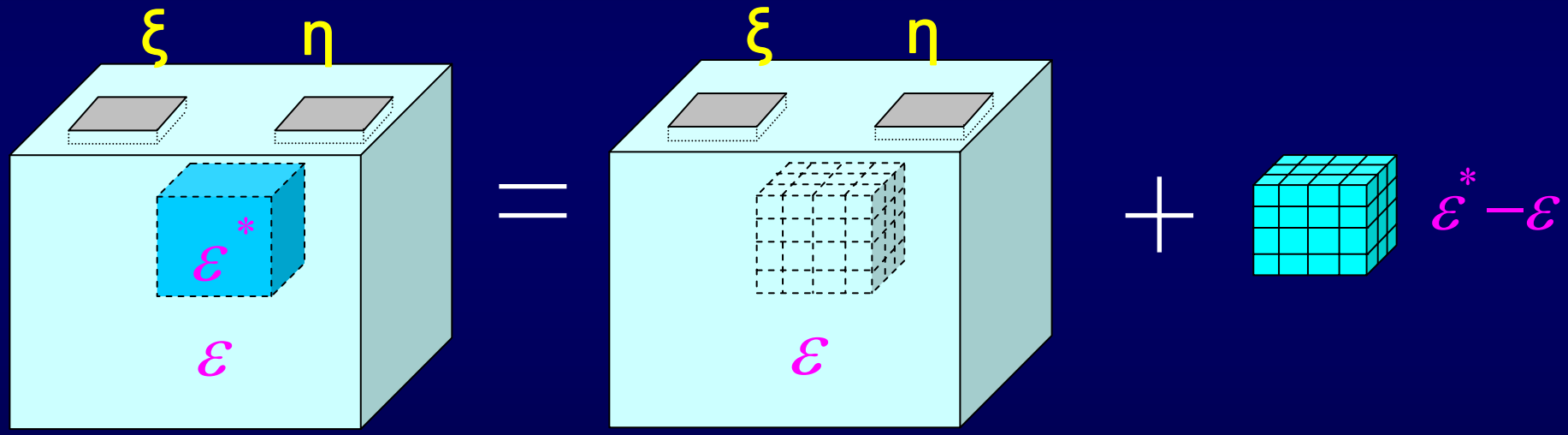
Inhomogeneous Substrate Layers Taken Into Account

- **Homogeneous approximation not valid for sinkers, wells, and trenches**
- **Enhancement of EPIC allows incorporation of modern deep submicron CMOS, BiCMOS, etc.**



Two-Problem Approach[+]

Two contacts in a substrate with one local inhomogeneous region



Original problem local region permittivity ε^*

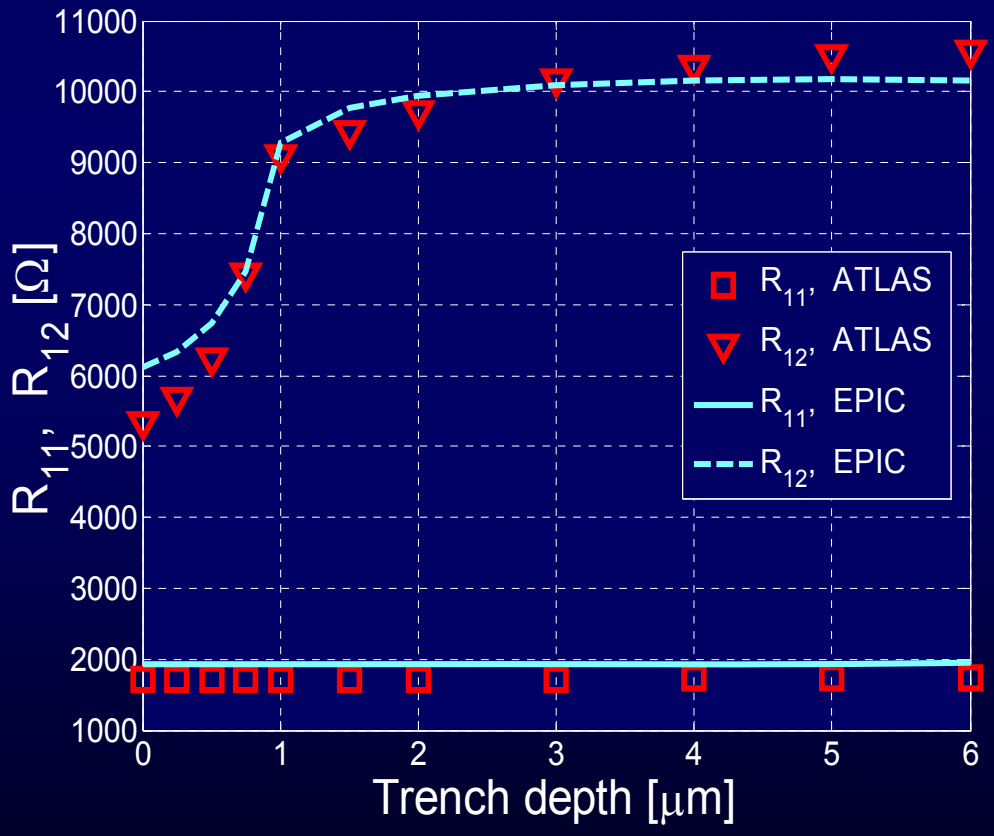
Homogenous substrate of permittivity ε

Companion region of permittivity $\varepsilon^* - \varepsilon$

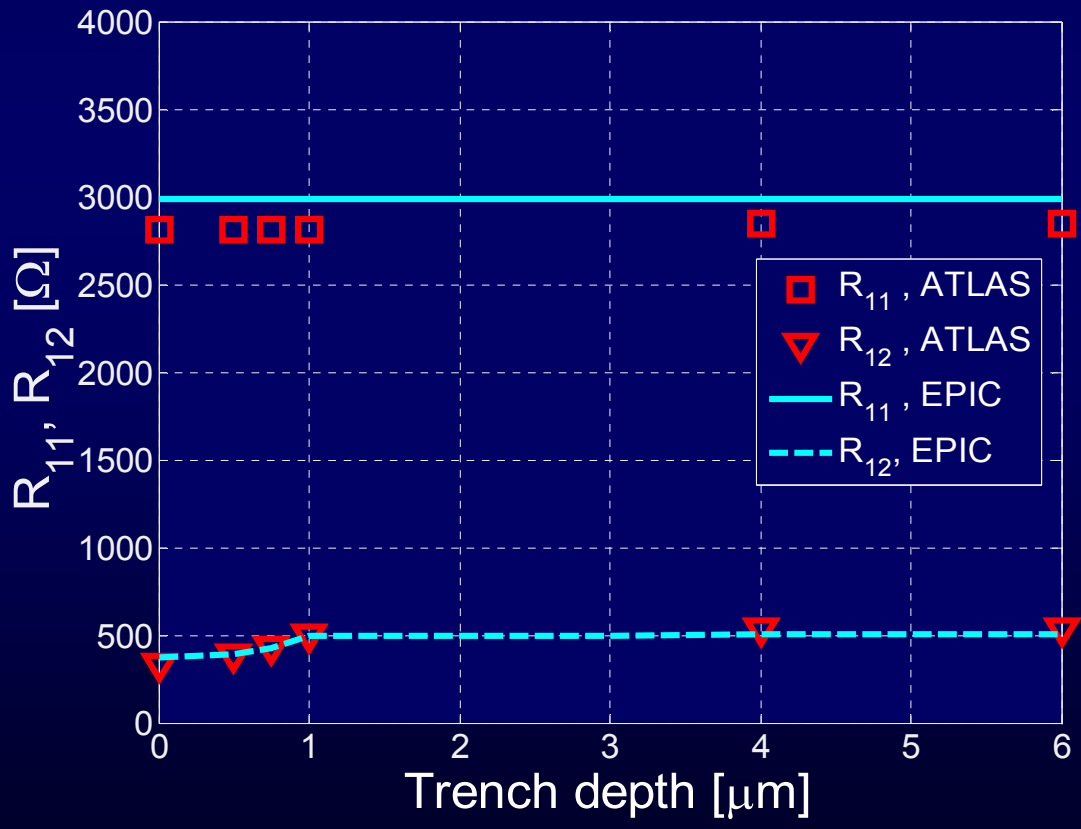
[+]R. Gharpurey, *Ph.D. Dissertation*, UC Berkeley, 1995

EPIC and ATLAS Comparisons

EPIC shows good agreement with ATLAS for both heavily and lightly substrates



Heavily Doped Substrate



Lightly Doped Substrate

Substrate Parasitic Extraction for High Frequency Applications

- **Static Green's function for purely resistive or capacitive substrates**
  - ✓ Resistive for $\sigma >> \omega\varepsilon$
  - ✓ Capacitive for $\sigma << \omega\varepsilon$
- **When σ and ωε comparable, quasi-static or full-wave simulations needed**
  - ✓ For typical heavily and lightly doped substrate, quasi-static analysis can be accurate up to 20GHz [1]
- **Quasi-static Green's function has the same form as static Green's function if complex permittivity is used [2]**

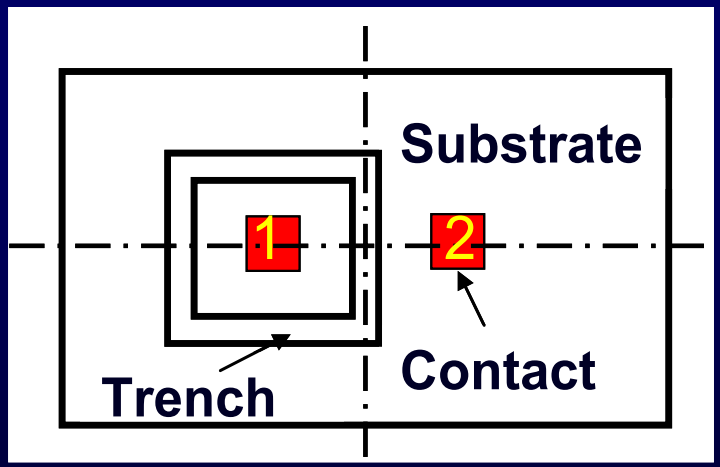
$$\varepsilon_c = \varepsilon - j\frac{\sigma}{\omega}$$

[1] G. Veronis, Y. Lu, and R. W. Dutton, *Proc. ISQED*, 2004

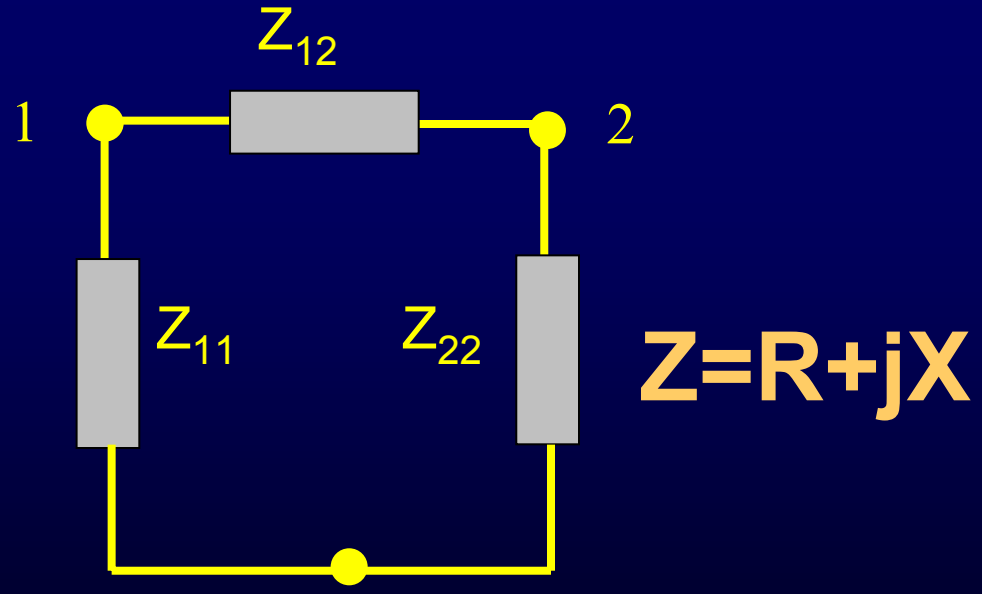
[2] R. Gharpurey and S. Hosur, *ICCAD*, 1997

Inclusion of Frequency Dependence

- **Two identical contacts with one surrounded by trench**
  - ✓ For zero trench depth: Z11 and Z12 as a function of frequency
  - ✓ Fixed frequency: Z11 and Z12 as a function of trench depth



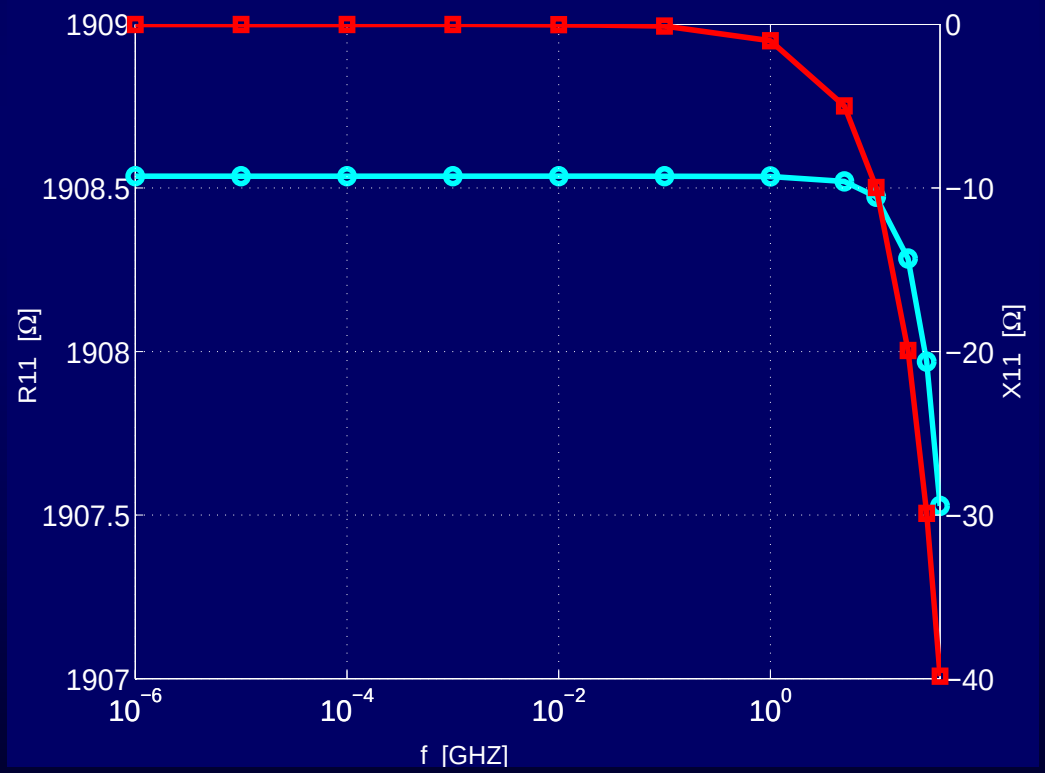
Two contacts and a trench

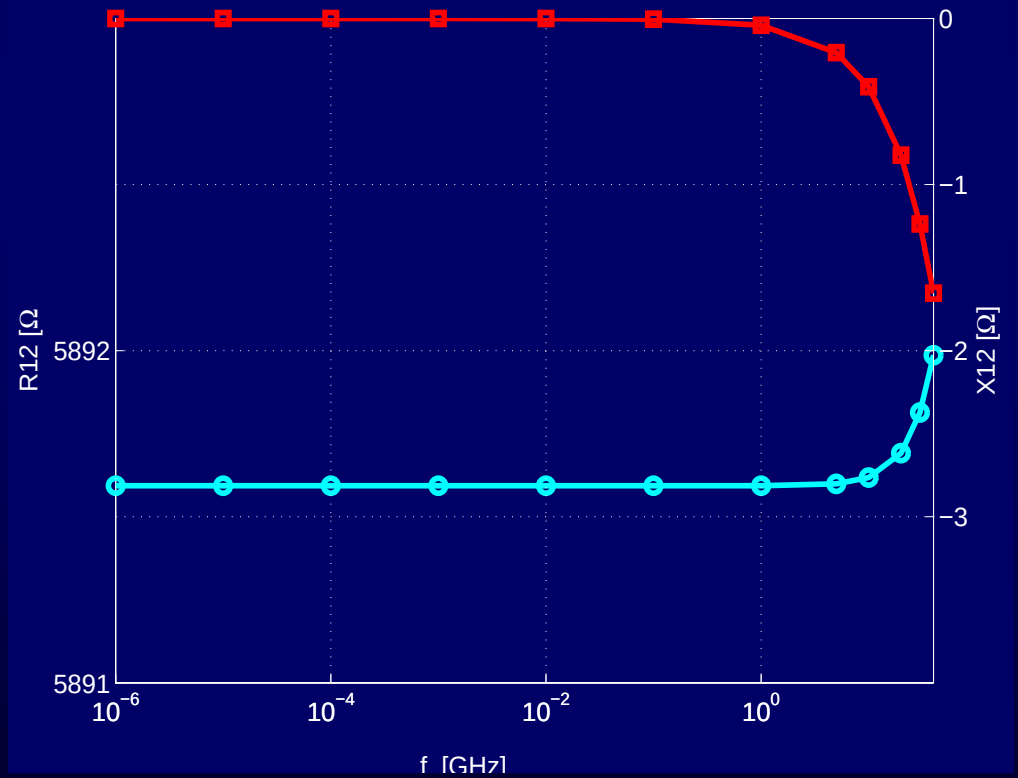


Equivalent circuit model

Frequency Dependence Without Trench

- **Z11 and Z22 identical because of symmetry**
- **Capacitive behavior observed for f > 10 GHz**



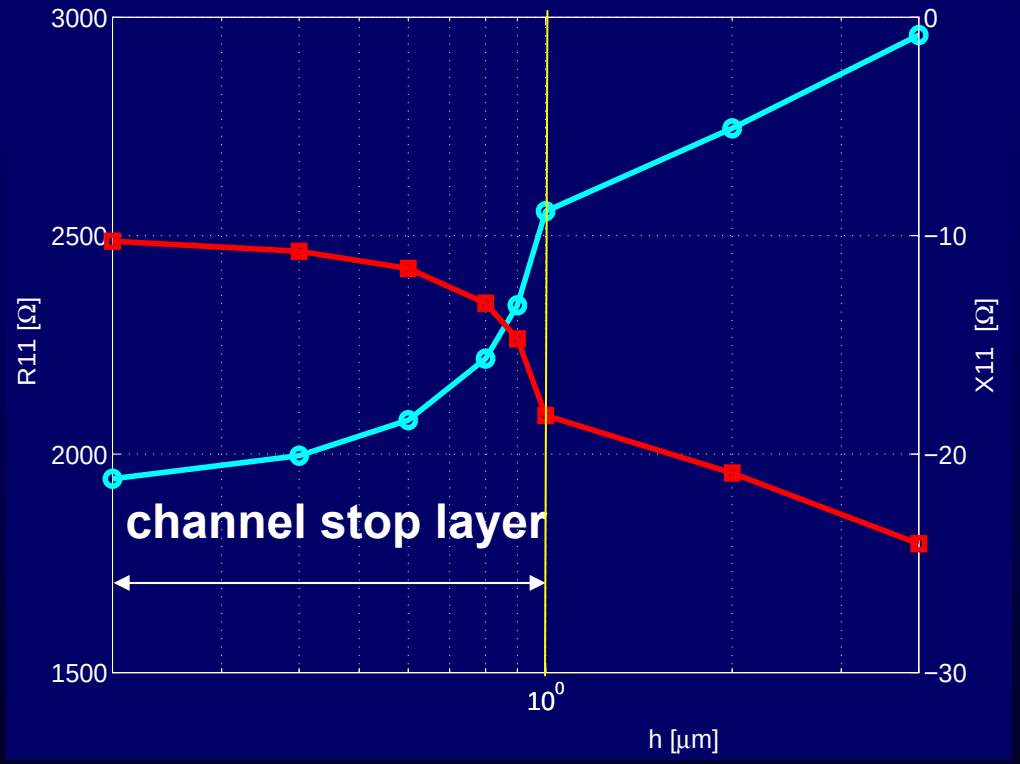


R11, X11

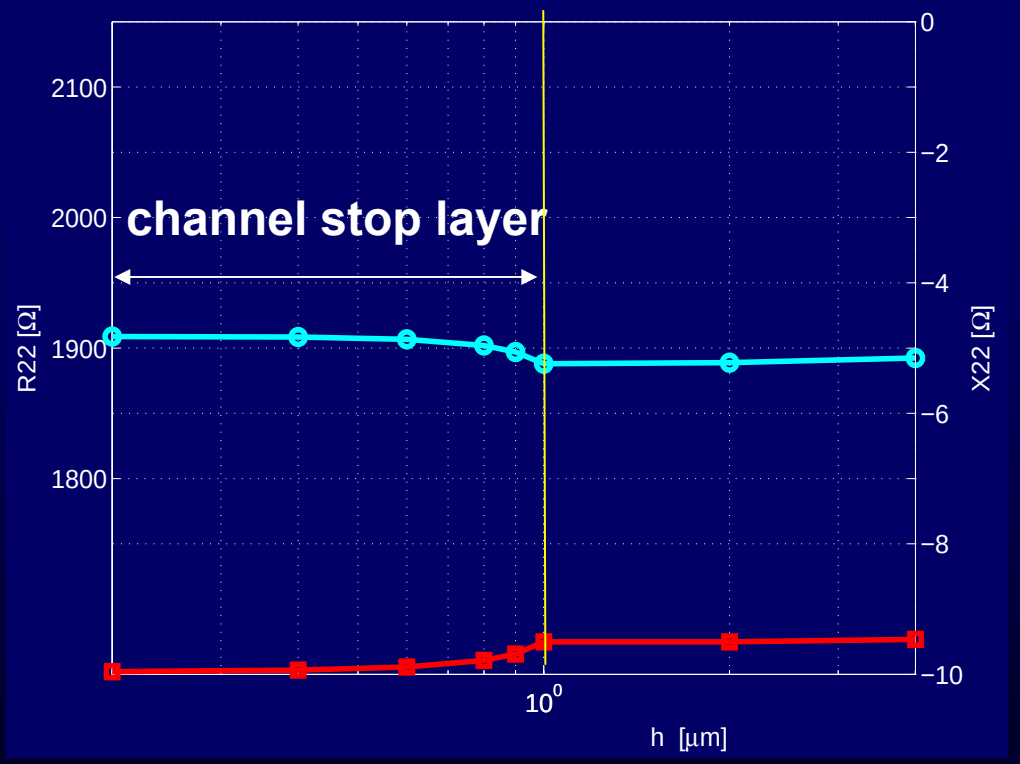
R12, X12

Self-coupling Impedance with Trench Depth

- **With an increase in trench depth (f = 10 GHz)**
  - ✓Z11 much more sensitive to trench depth change
  - ✓Z11 and Z22 change in opposite directions

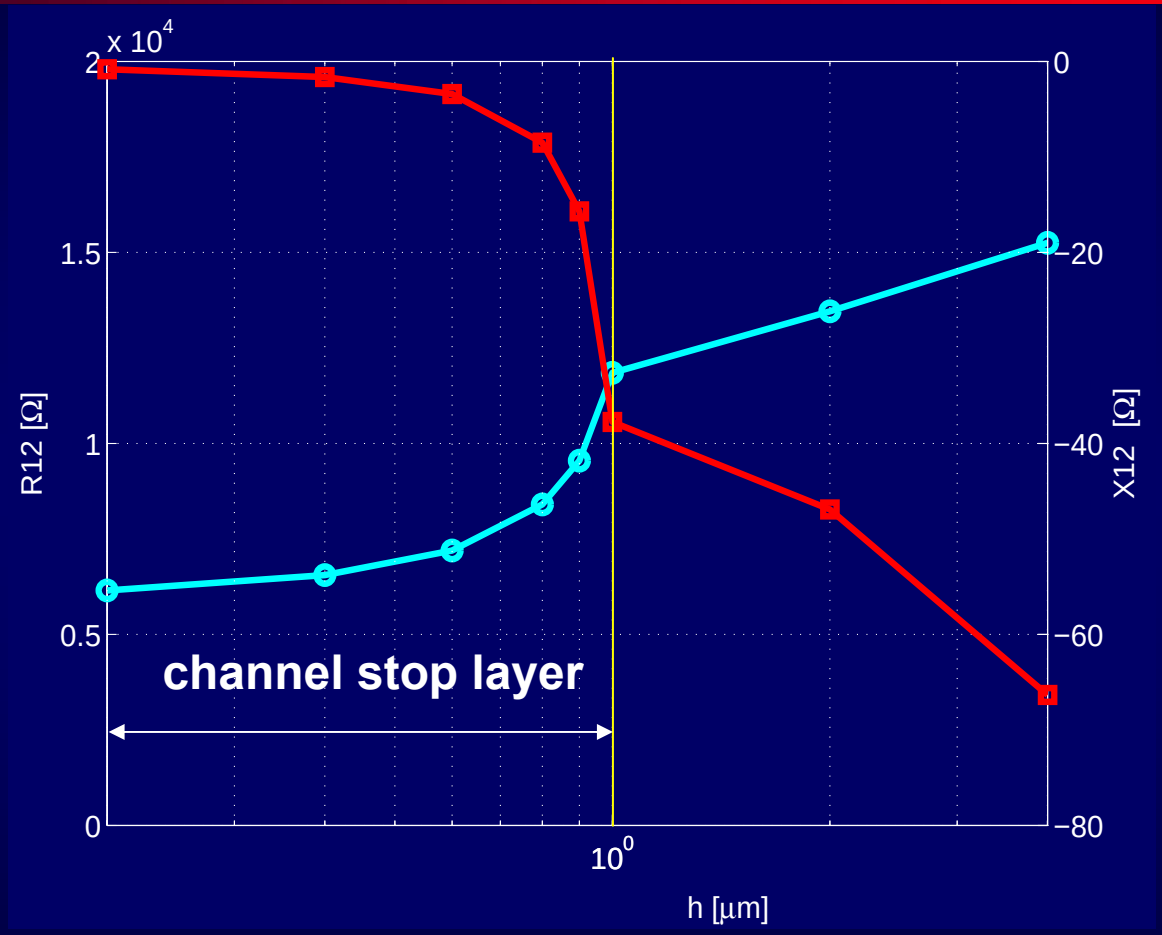


R11, X11



R22, X22

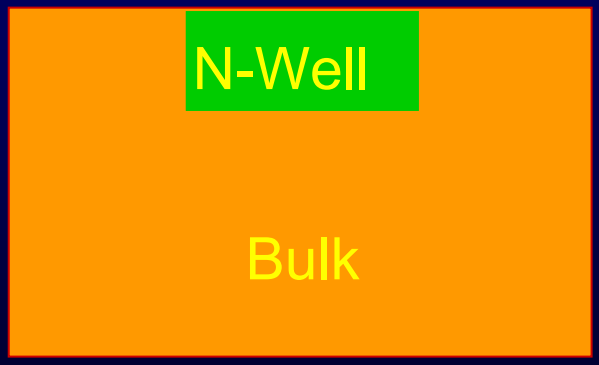
Cross-Coupling Impedance as a Function of Trench Depth



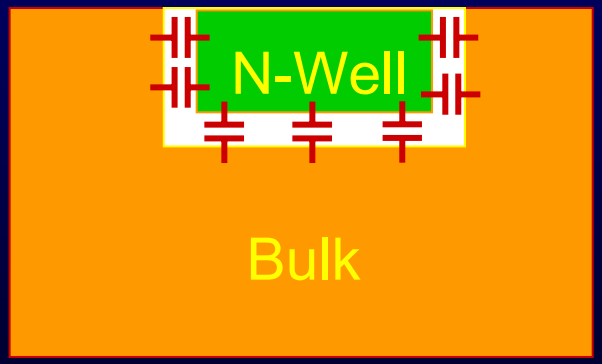
- **Both resistance and capacitance increase with trench depth**

Extensions for N-Well Modeling

- **Depletion region modeled as a trench with capacitances**
  - ✓ Trench eliminates DC coupling between well and bulk
  - ✓ AC coupling modeled by capacitors connecting well to bulk

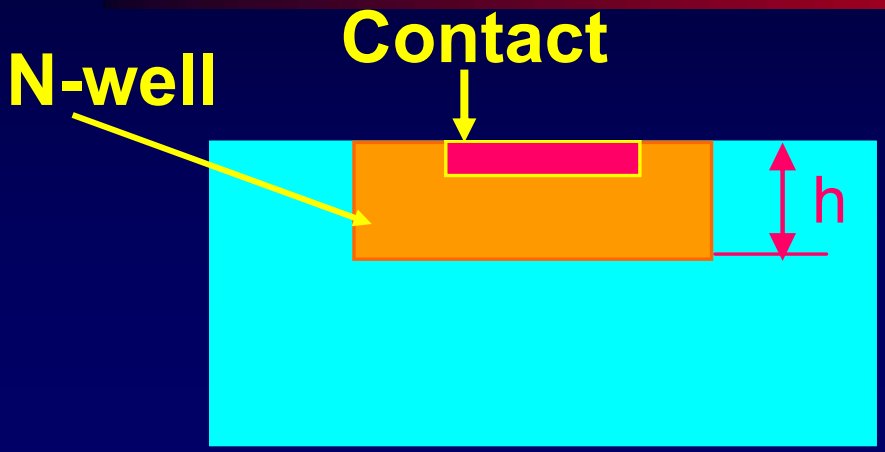


N-Well in a substrate

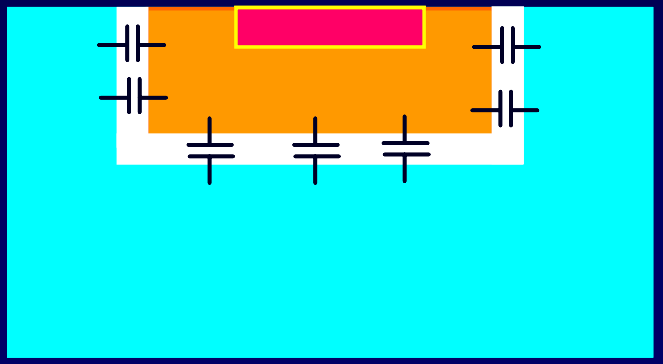


N-Well model

N-Well Modeling Expected Trends



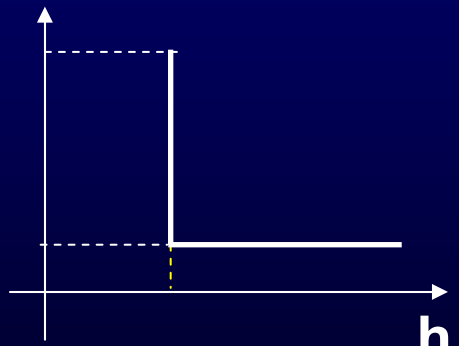
Contact in a well



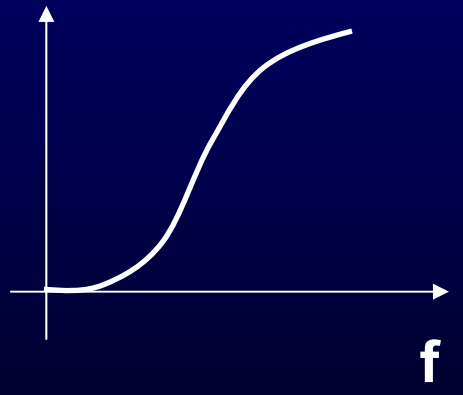
Numerical model

G11,h=0

G11,h>0 = 0



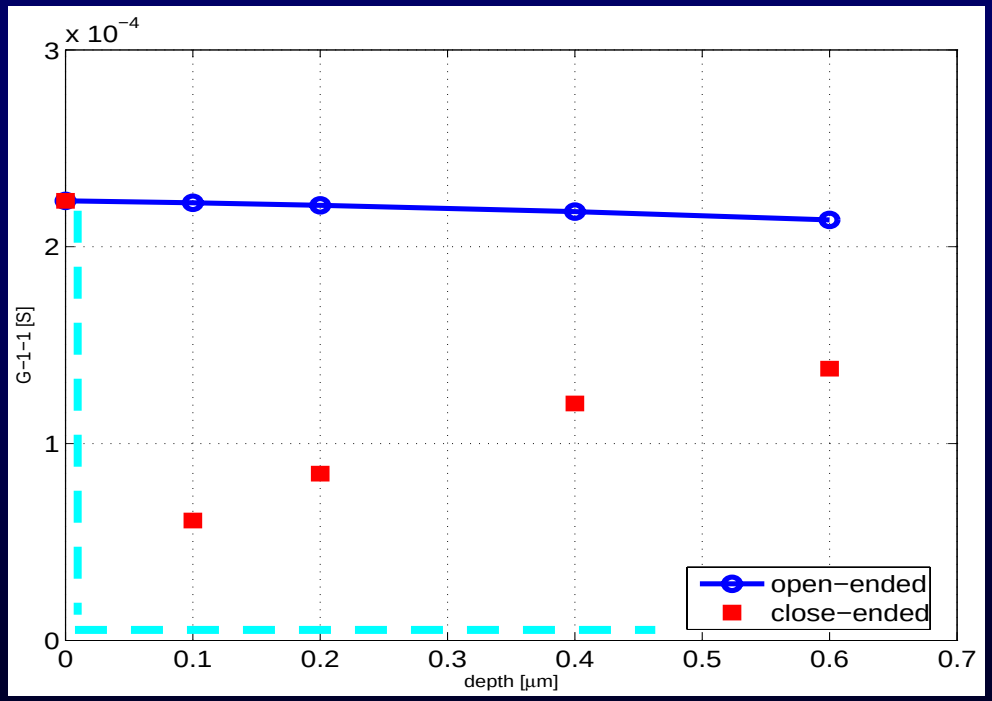
Low frequency behavior



High frequency behavior

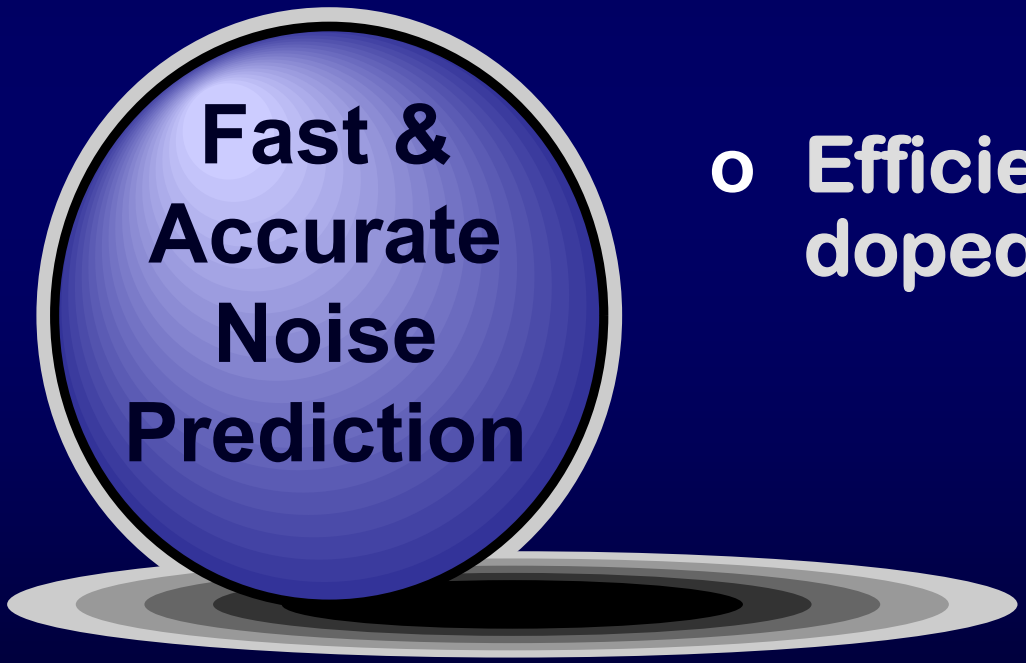
Calculated Low Frequency Behavior

- **Non-zero conductance at DC**
- **Dependence of conductance on well depth**
  - ✓ Numerics and code being debugged



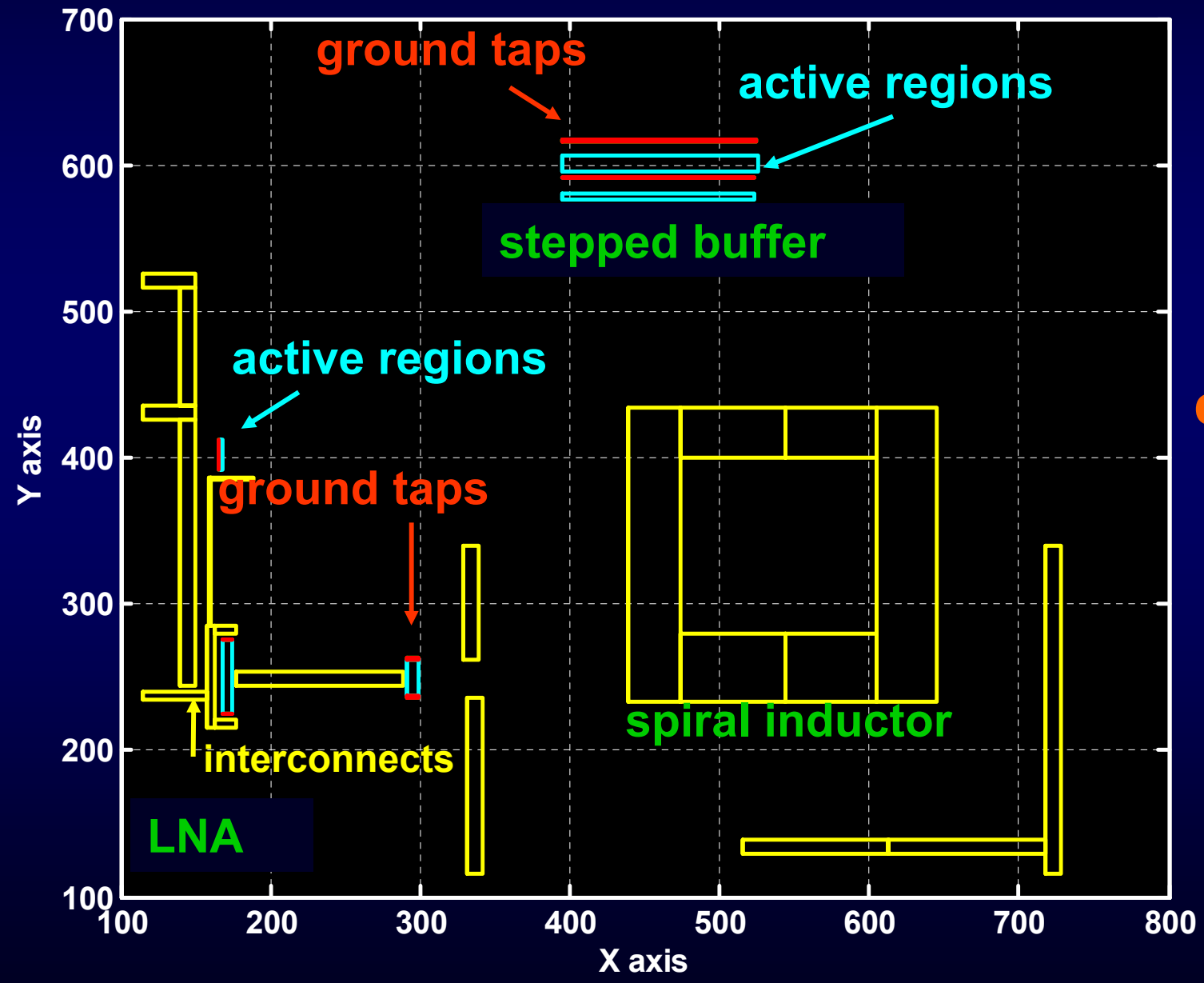
G11 as a function of well

Models for Substrate Parasitics



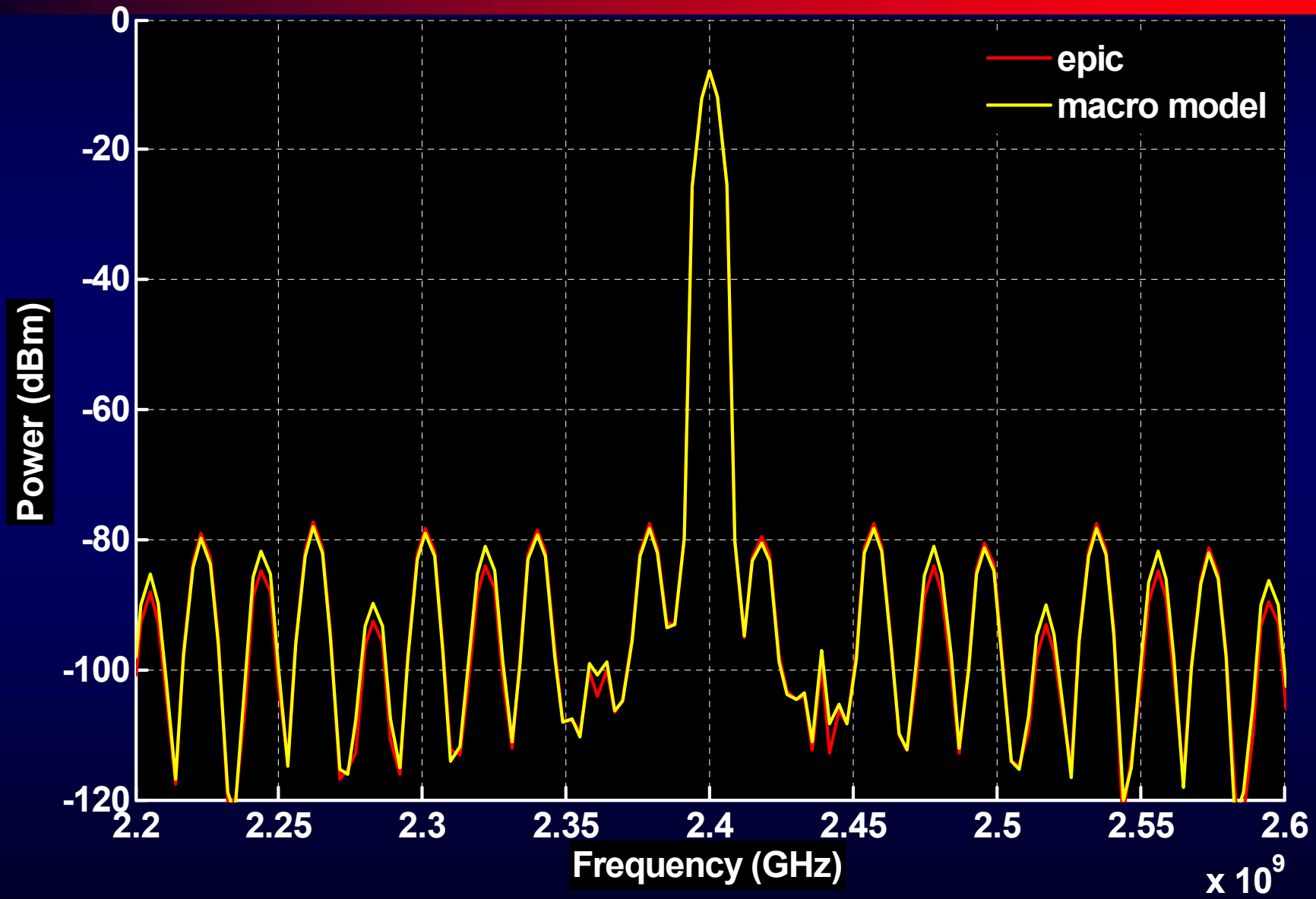
- Efficient macromodel for lightly doped processes

Application of Macro-model to RF LNA and Stepped Buffer Circuit

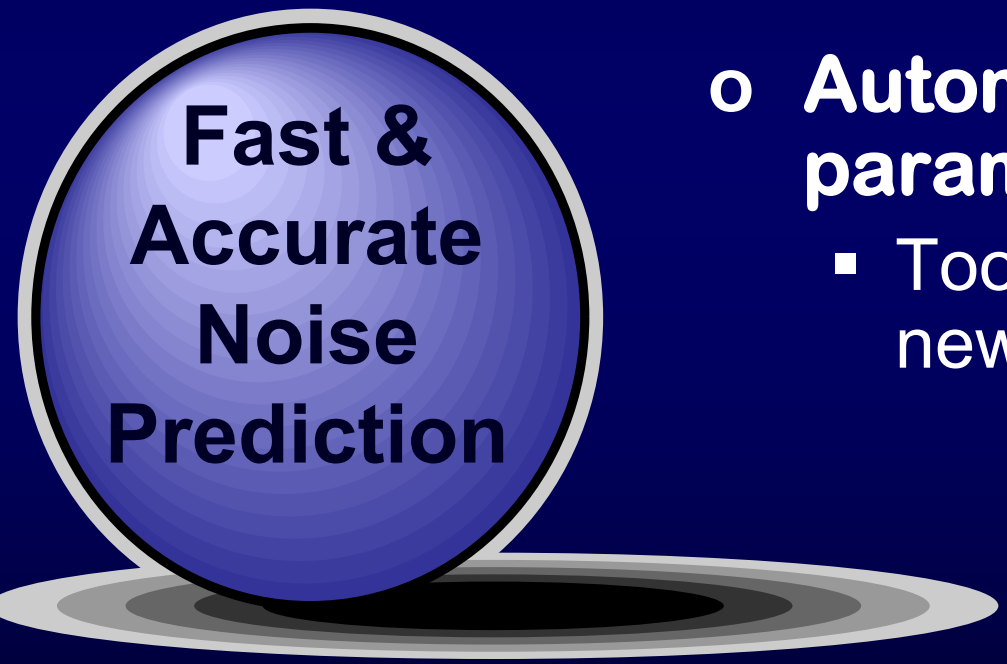


36 contacts

Macro-model Matches EPIC and Achieves *15x* Speedup for LNA Circuit

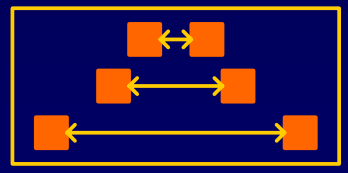


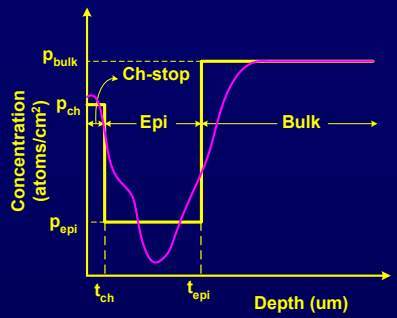
Models for Substrate Parasitics



- **Automated substrate model parameter generation**
  - Tool enables easy application to new processes

Incorporation of New Technology into Silencer!





$$Z_{12} = \alpha e^{-\beta x}$$

MEASURED Z11

DOPING PROFILE ESTIMATE

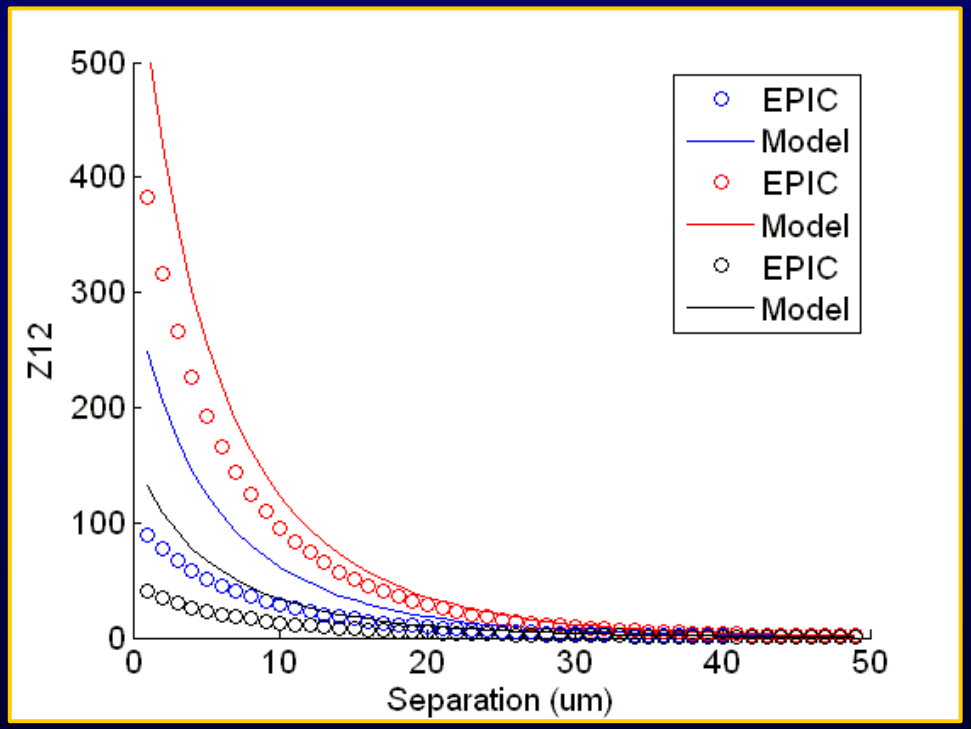
MACRO-MODEL EQUATION

AUTOMATED PARAMETER EXTRACTION

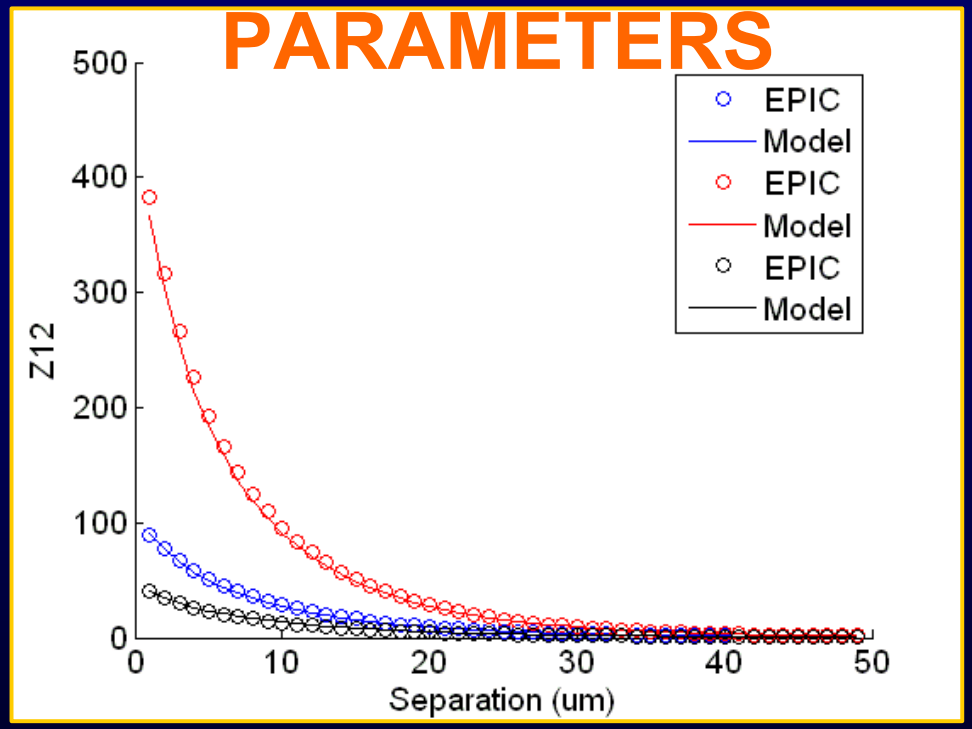
MODEL PARAMETERS

Automated Parameter Extraction Validation

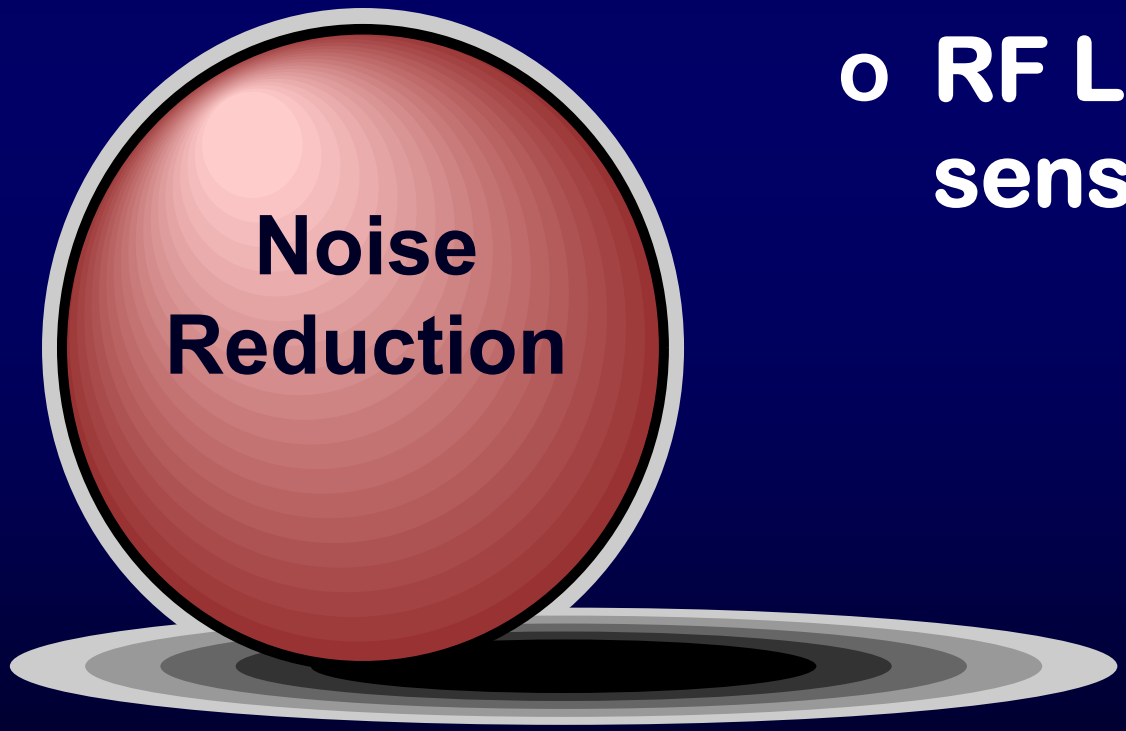
INITIAL GUESS



FINAL EXTRACTED PARAMETERS



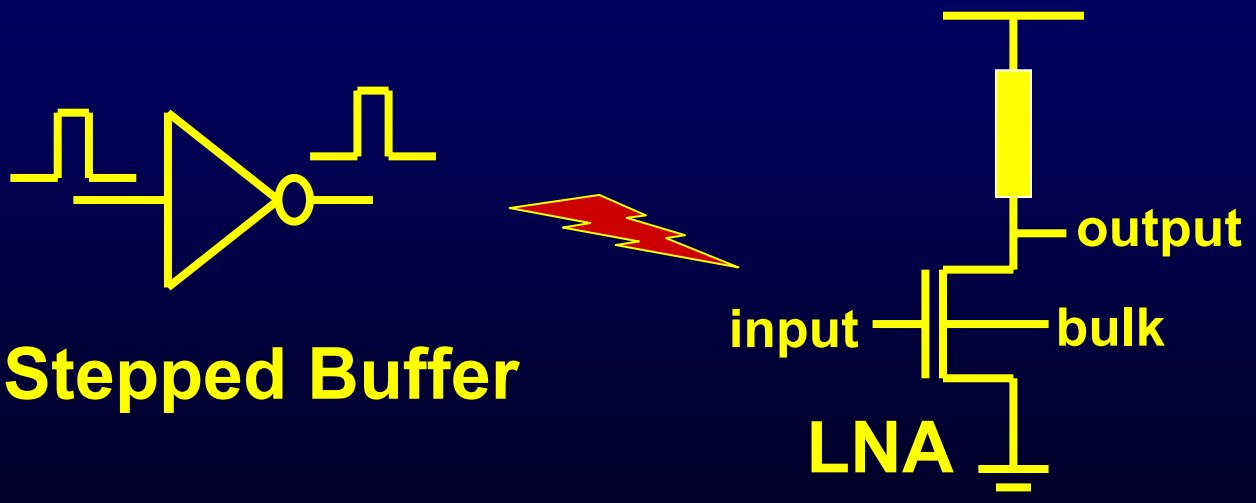
Design Approaches for Noise Mitigation



- **RF LNA substrate noise sensitivity**

Approach

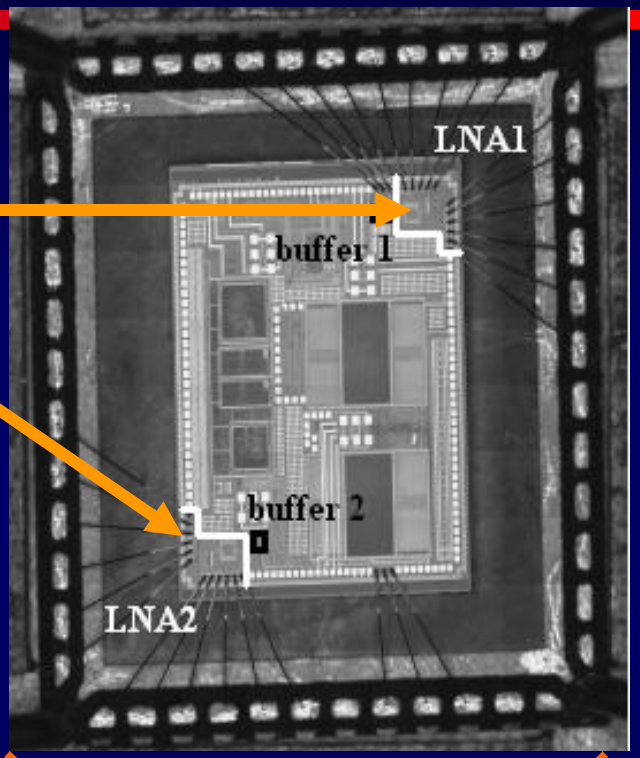
- **Evaluate noise coupling from stepped buffer to 1.5GHz LNA with simulations and measurements**
  - ✓ Substrate tap area
  - ✓ Location of substrate taps

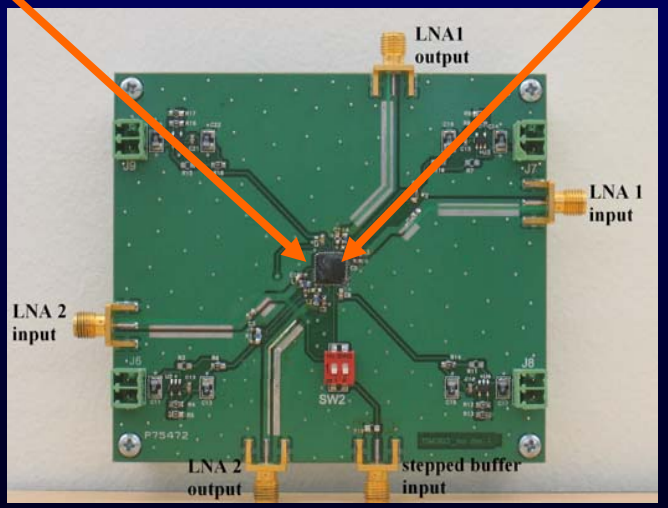


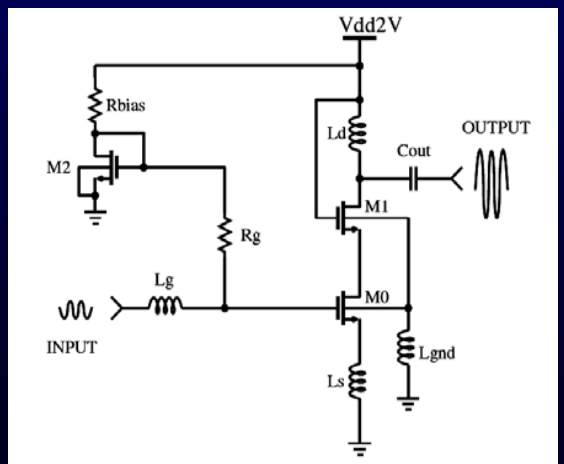
Experimental Setup and Die Photo

0.25μm CMOS Process

- **Two LNAs and stepped buffers on opposite corners**
- **Die assembled in 48-pin MLF plastic package**
- **Mounted on 2 layer FR4 test board with isolated supplies**



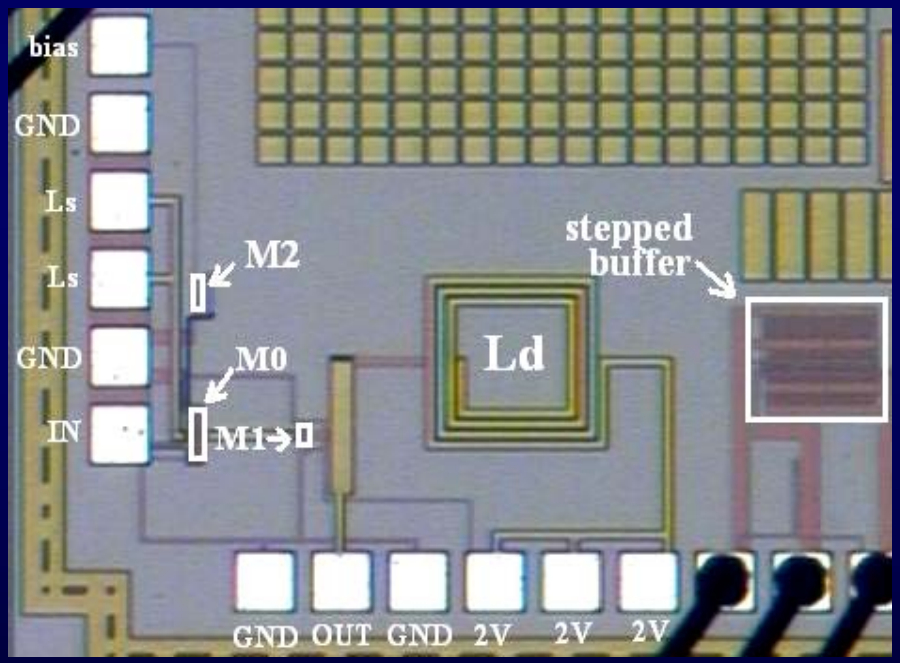




LNA Substrate Taps

LNA1: Few Taps

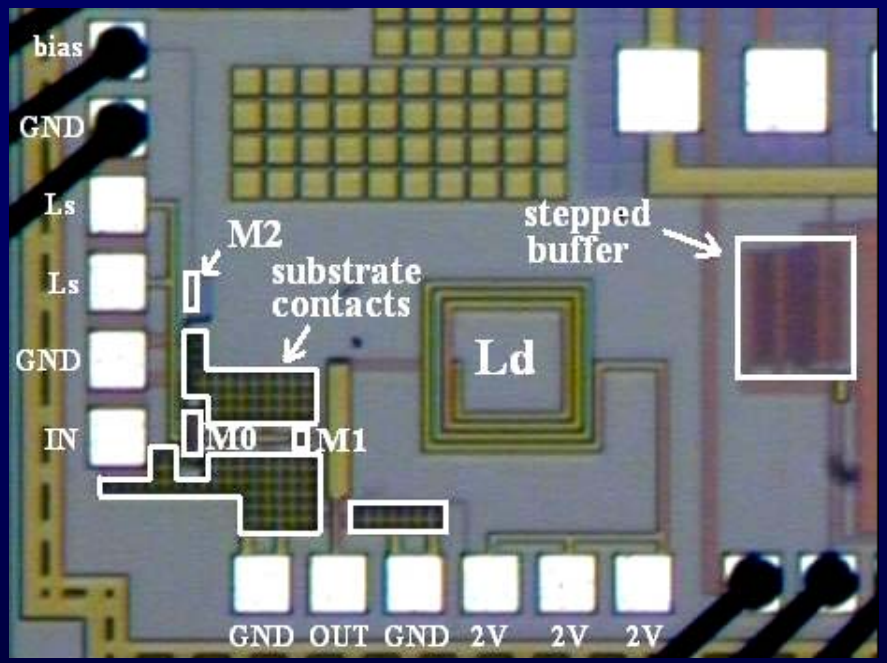
0.6 μm wide sections



Total tap area = 60 μm^2

LNA2: 400X Tap Area

Grounded grid



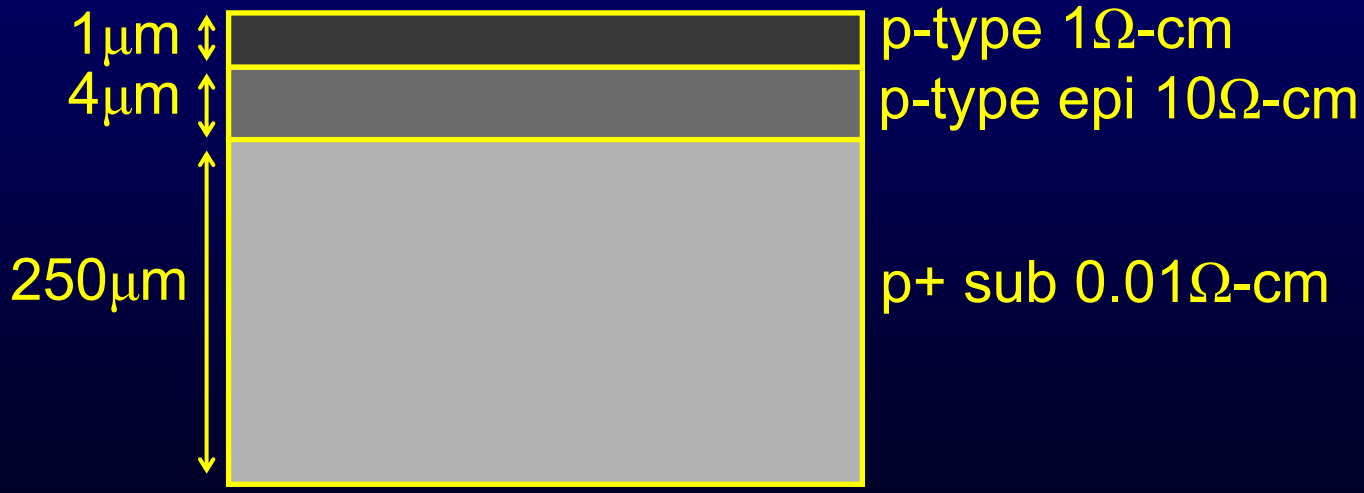
Total tap area = 24,000 μm^2

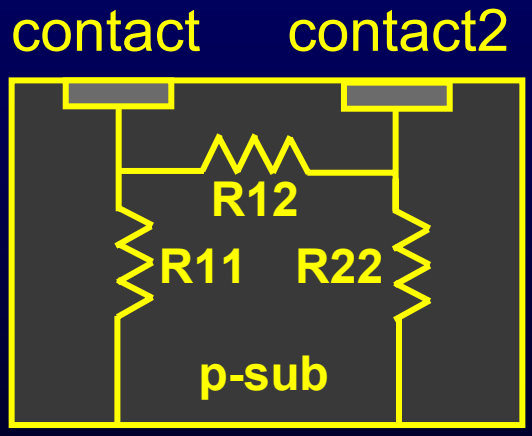
Circuit Simulation and Modeling

- Cadence Spectre RF simulator
- BSIM3v3 MOSFET TSMC transistor models
- On-chip interconnect and passive component models from TSMC and s-parameter simulations
- Package lead and bond wire models from EM simulations and package manufacturer data
- PCB trace models from simulations and component models from manufacturers

Heavily Doped Substrate Modeling

- Layered approximation for doping profile
- Green's function based solver for extracting resistive substrate network
- Resistive network connects NMOS active areas, substrate taps, and on-chip interconnects





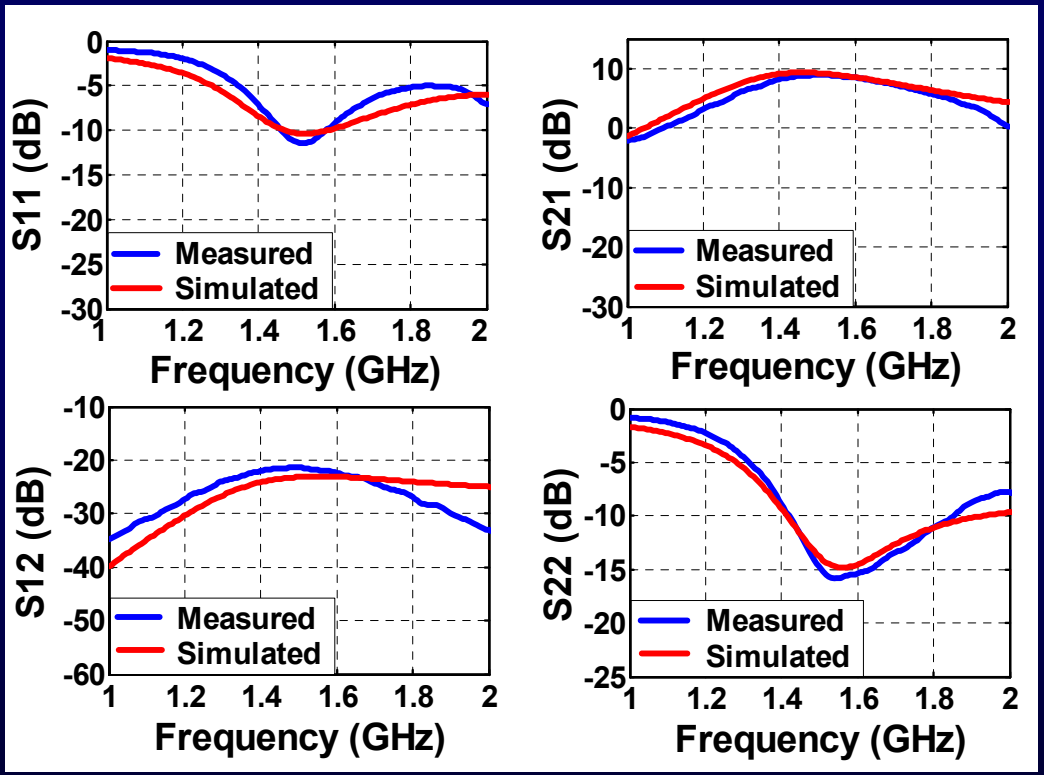
Measured LNA S-Parameters

At 1.5 GHz good agreement in measured performance

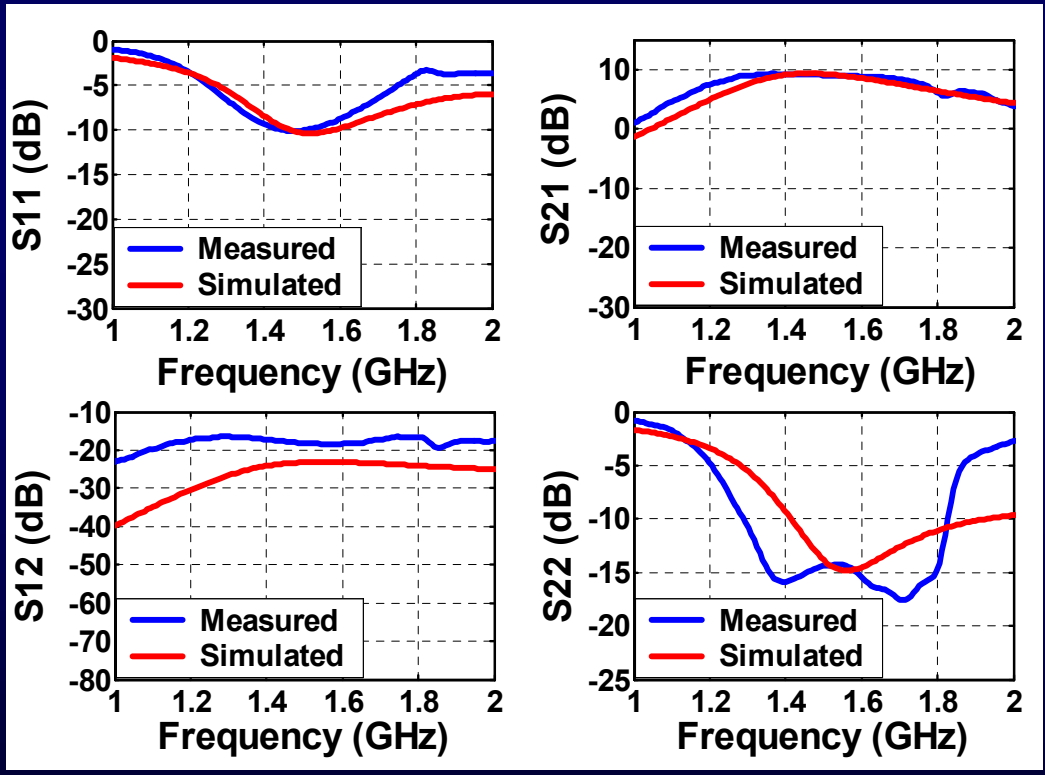
	LNA1	LNA2
S11(dB)	-11.3	-10.0
S21(dB)	8.9	9.0
S12(dB)	-21.3	-18.1
S22(dB)	-14.9	-14.4

Good Agreement between Simulated and Measured LNA S-Parameters

LNA1

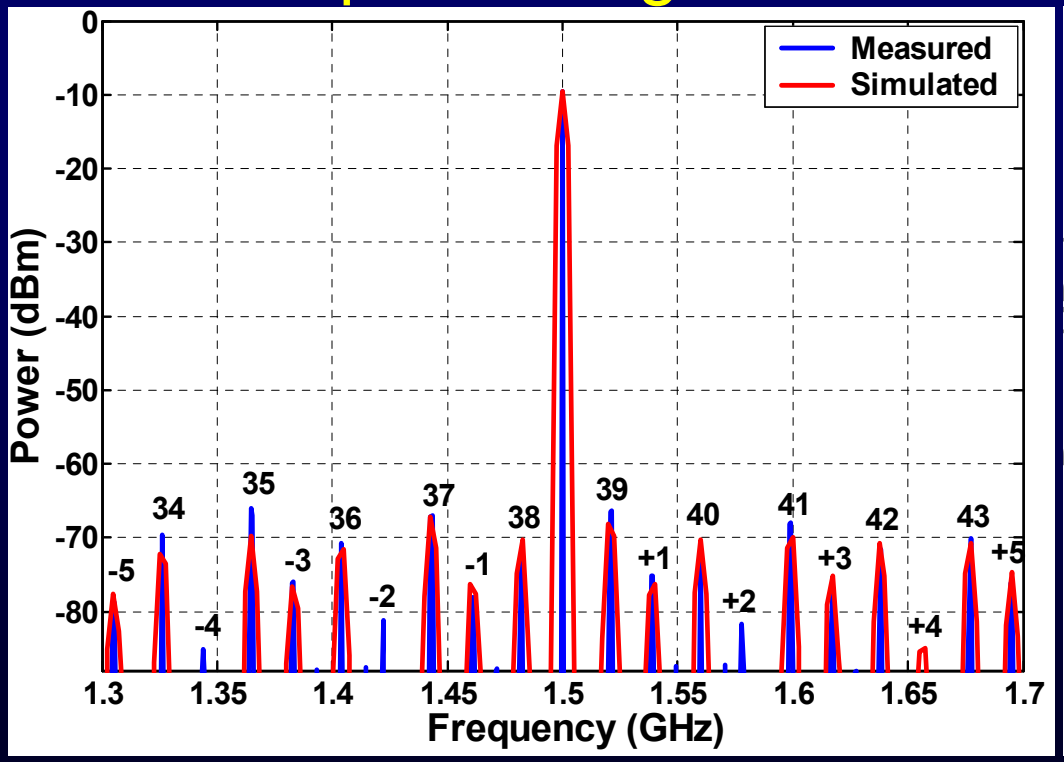


LNA2

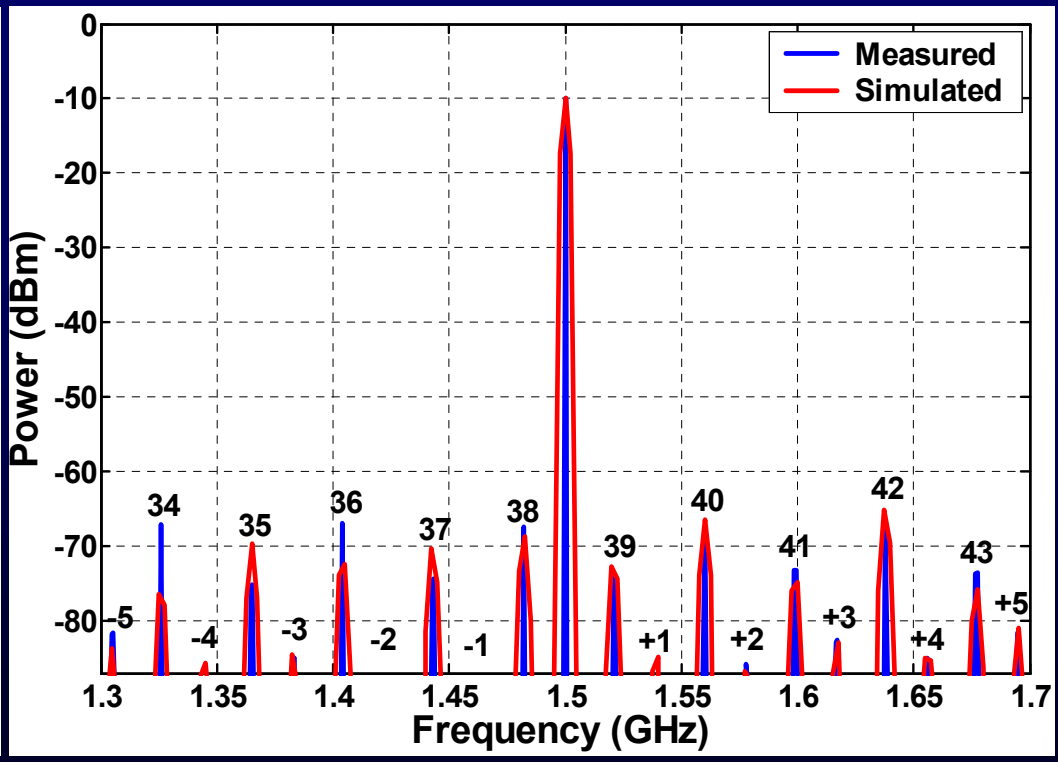


Measured and Simulated Substrate Noise at LNA Outputs

- **Clock harmonics and IM tones at LNA output**
  - ✓ Lower IM noise levels in LNA2 due to larger substrate taps
  - ✓ Harmonic noise differences due to buffer power and input routing



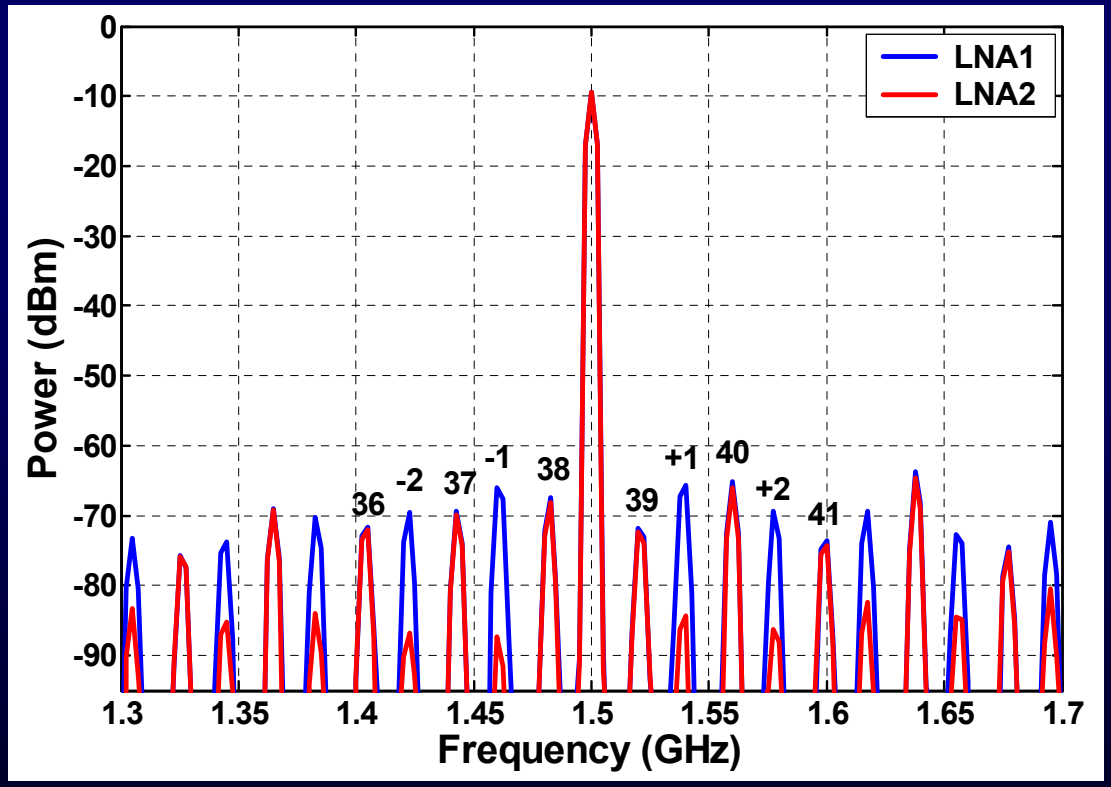
LNA1



LNA2

Simulations with Identical Noise Injection

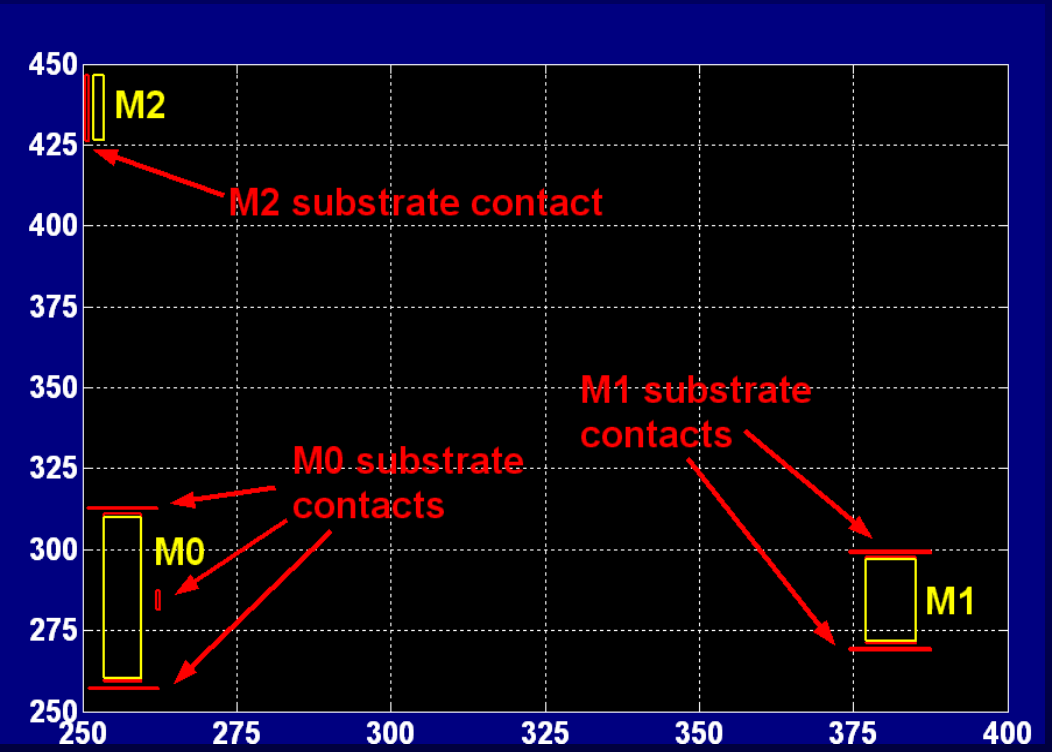
- **Differences in IM terms only**
- **95% of harmonic noise couples directly into LNA supply and output bond pads**

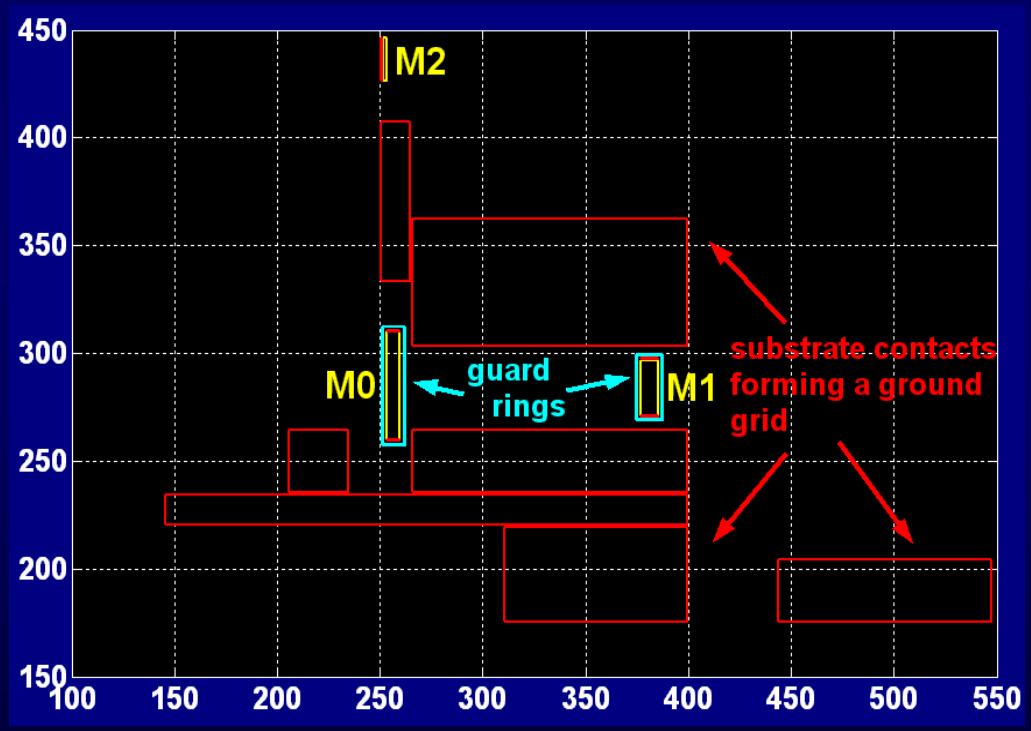


S. Hazenboom, *CICC, 2004*

Substrate Contact Area Scaling

Contact areas scaled from 1 to 400



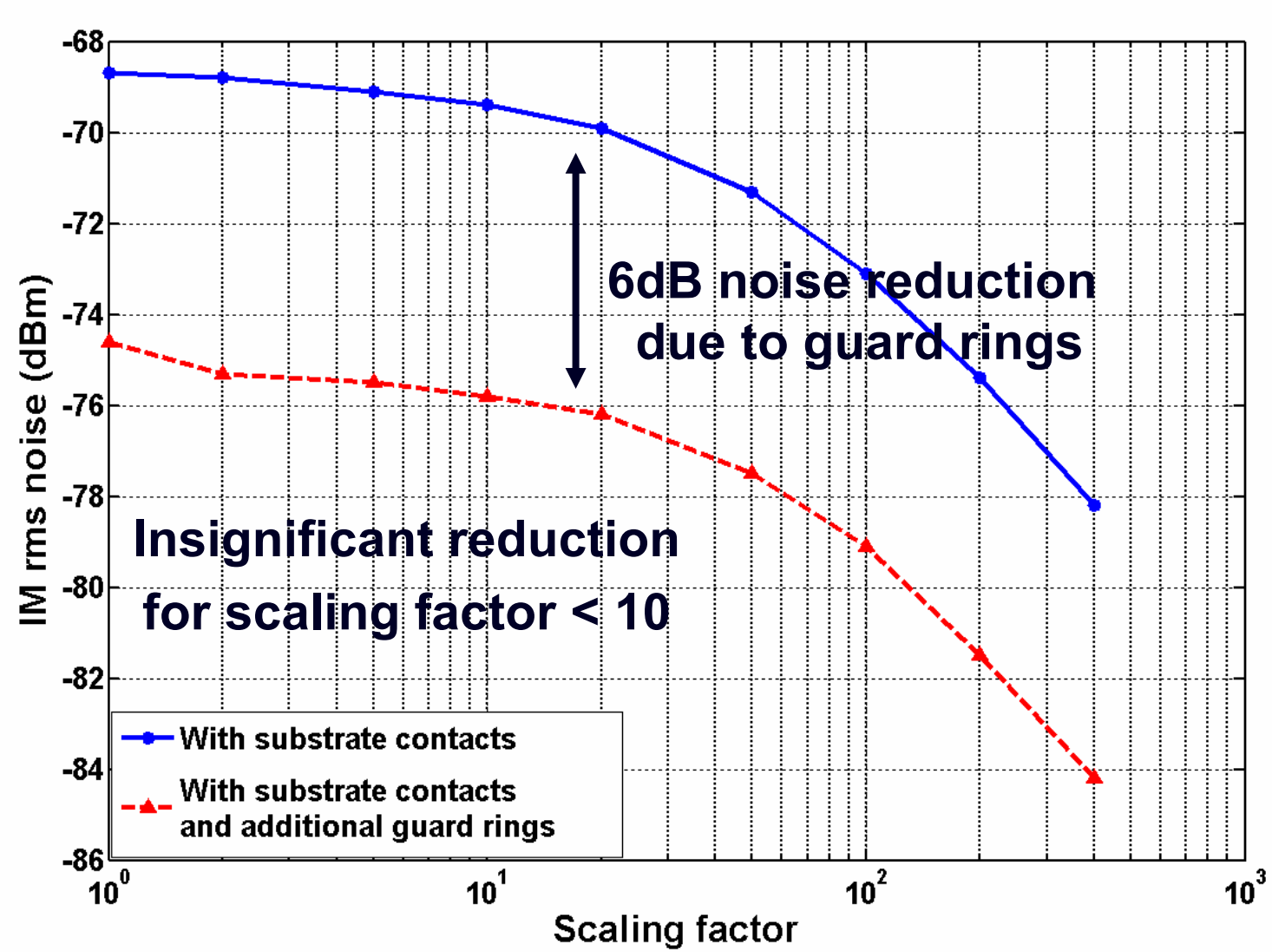


LNA1 : Area = 1X

LNA2 : Area = 400X

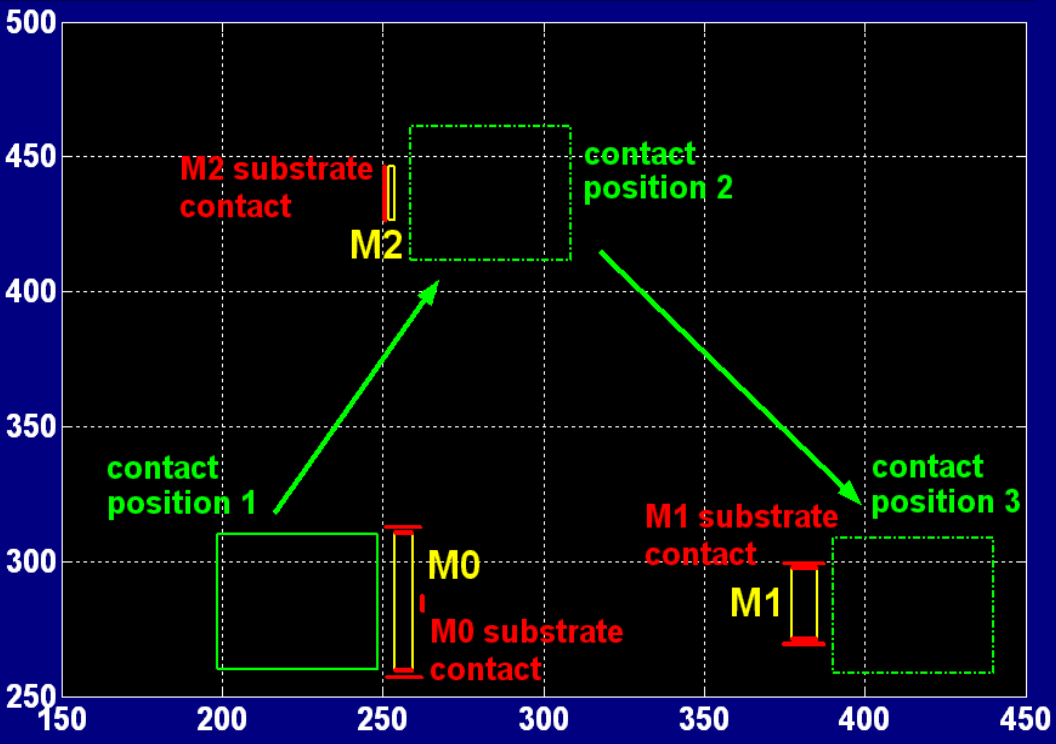
Simulated Results: Substrate Contact Area Scaling

Final size of 400X yields improvement of 9dB

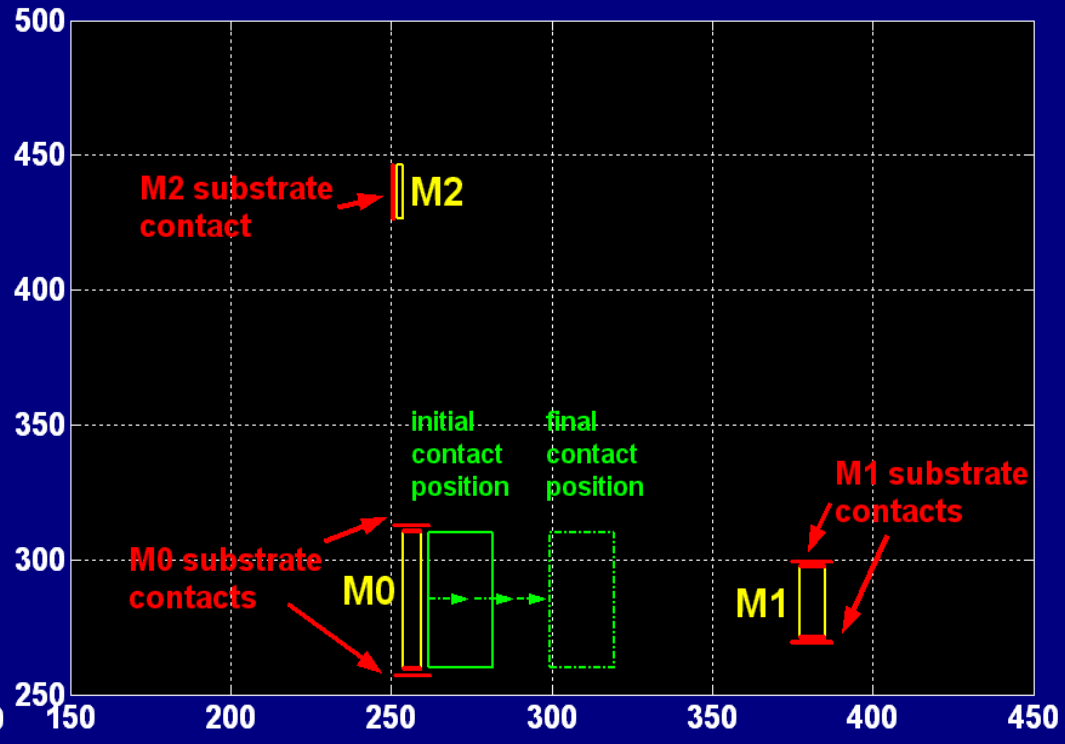


Substrate Contact Location

Identification of sensitive transistor



Proximity to sensitive transistor



Summary

- Extended Green's function based parasitic extraction to high frequencies with inhomogeneous substrate layers
- Developed new accurate low frequency macromodel for lightly doped substrate
- Developed tool for automatic extraction of model parameters
- Noise coupling in RF LNA shows scaling of substrate tap area by 400 improves isolation by 9dB

Comprehensive Approach to Substrate Noise Coupling