Sensitivity-based Modeling and Methodology For Full-Chip Substrate Noise Analysis

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Abstract

Substrate noise (SN) is an important problem in mixed-signal designs. With increasing design complexity, it is not possible to simulate for SN with a detailed SPICE model that uses an accurate model for each transistor. In this paper, we propose a sensitivity analysis- and static timing analysis-based methodology to derive a reduced model that computes the worst case substrate noise in the design. The reduced model contains only passive components, which are very few, and is very quick to simulate. The main feature of our methodology is that, unlike previous approaches, it is independent of input patterns and does not need to simulate for millions of clock cycles. This lets us apply it to a full-chip design in reasonable CPU time. We validate our reduced model on several benchmark circuits against a detailed and highly accurate reference model. On average, the reduced model is within 13% of the reference model and is up to 42 times faster. Finally, we apply our methodology to a mixed-signal switch chip design consisting of 8 million gates and show that it finishes in 17 minutes.

1 Introduction

Mixed-signal designs have become ubiquitous with the proliferation of deep sub-micron (DSM) system-on-chip (SOC) design methodologies. In such systems, maintaining signal integrity and reducing noise have become the most vexing issues. Switching noise due to large signal swings in the digital part can propagate through the common substrate and corrupt sensitive analog part (Figure 1). In technologies that have low resistivity substrates, noise generated in one region of the die may cause the rest of the chip to malfunction. Decreasing feature size lets more devices to be packed on a chip, generating higher overall noise. In addition, smaller device geometries translate to reduced threshold voltages resulting in higher sub-threshold leakage currents. Smaller devices are also more sensitive to noise because of reduced noise margins. The increasing switching rates and decreasing transition times are also responsible for more transients. Due to all these DSM effects, *substrate noise analysis* (SNA) has become a critical problem in most mixed-signal designs.

Traditionally, SPICE was the primary tool used by designers for noise analysis. However, it is not feasible to use SPICE on even a 100K-gate block. It is important to come up with high level models and methods to enable chip-level analysis. Due to iterative nature of the existing design flows, substrate noise analysis must be very fast.

Two important aspects of substrate noise are peak-to-peak noise and frequency-domain analysis. In this paper, we focus only on the peak-to-peak noise. The most important reason for doing this is that due to body effect, any fluctuation in substrate reference potential changes the threshold voltage of the devices, playing havoc with the noise margins. Analog devices are especially sensitive to substrate reference potential changes.

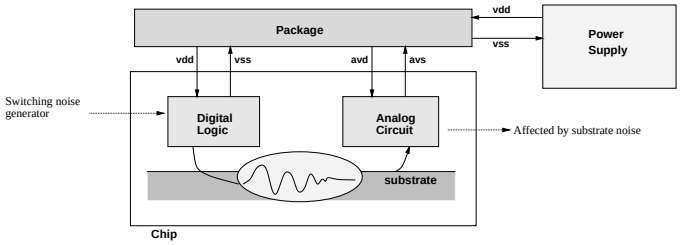

Figure 1: Substrate noise in mixed-signal system

In this paper we present a full-chip substrate noise analysis methodology based on static timing analysis and reduced passive substrate noise models. The main contributions of our work are as follows.

1. We present a new *pattern-independent methodology* (PIM) for SNA. It does not use any testbench or simulation and is much faster as compared to the pattern-dependent flows used in the previous approaches [4, 5]. Our methodology is naturally suited to full-chip designs.

2. Our reduced model is based on sensitivity analysis, where we model more accurately the factors that influence substrate noise the most. We believe this is the first paper to use such an analysis technique for analyzing substrate noise.

3. We propose a current waveform generation technique which is novel in the context of noise analysis. It uses static timing analysis, circuit topology and cell functionality to derive the waveform corresponding to the worst case behavior.

4. Package influences the substrate noise considerably. We include the effect of package in our noise model.

5. Our methodology considers the influence of capacitive load driven by a gate in the circuit. This is in contrast with all previous works.

The outline of the paper is as follows. In the next section, we present a summary of the previous SNA work. Our proposed methodology is described in Section 3. In Section 4, we present a reference model, which will be used to validate the reduced model we propose. In Section 5, we present details of our methodology: namely the reduced model, the sensitivity analysis used in deriving it, and the algorithm used for current waveform modeling. Section 6 presents experimental evidence of the accuracy of our proposed model and methodology. Section 7 describes how we apply the model to an industrial chip. Conclusions and directions for future work are presented in Section 8.

*The work was done when the author was an intern at Fujitsu Laboratories of America.

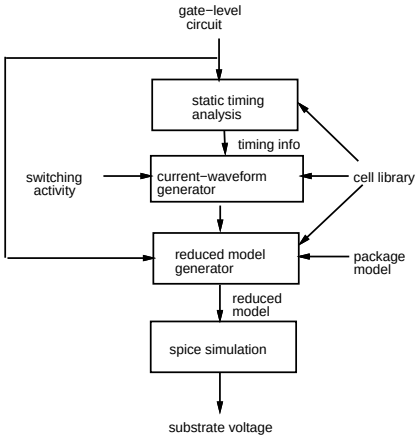

Figure 2: Pattern-independent methodology

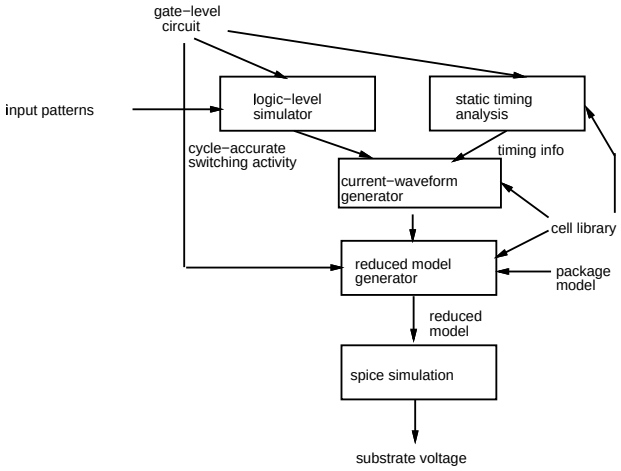

Figure 3: Pattern-dependent methodology

2 Previous Work

A lot of research work has been done on modeling the substrate noise during the design phase. [4, 13, 5, 6, 2] derive a passive network model that can be simulated with SPICE to yield substrate noise patterns for the entire design for the set of input vectors from a testbench. Each cell in the library is simulated with SPICE for all possible inputs and power supply current and substrate injection currents are extracted. This knowledge is used to do a full-chip analysis. One problem with [4, 13] is that they do not consider package inductance and the associated power supply noise, and hence are not very practical. [5, 6, 2] do not consider the dependency of noise on the load at each gate.

In [7] a time-series divided parasitic capacitance model is proposed for time-domain power supply current estimation. In [3] the authors give a comprehensive analysis of various device mechanics involved in the generation of substrate noise.

Note that all these approaches are input-pattern dependent, i.e., a separate model must be derived for each input pattern. Even for a moderately sized design, the number of models can become very large. This leads to exorbitant run-times, making these approaches impractical for a full chip analysis. Also, there is no guarantee that the maximum noise will be reported, since the worst-case input pattern may not be present in the testbench.

3 Proposed SNA Methodology

Our overall SNA methodology is shown in Figure 2. It is based on deriving a *reduced model* (RM) of the digital part of the design. First, a *static timing analysis* (STA) tool generates the timing information for each gate, such as the minimum and maximum rise/fall arrival and transition times. This, along with the switching activity information, is used by the *current waveform generation* (CWG) algorithm to construct the current waveform used in RM. The switching activities of various blocks in the design are expected to be provided by the designer; otherwise they may be deduced from a simulation testbench. The package model is also incorporated into RM. RM is simulated in SPICE to yield the substrate noise voltage.

Salient features of our methodology are as follows.

– RM consists of only passive components, and that too very few; so it can be simulated quickly. Also, RM does not include any explicit primary inputs and hence is input pattern-independent.

– The timing information of switching gates (such as signal arrival and transition times), which is an important determinant of noise, is derived by invoking STA. STA implicitly captures the best and worst circuit timing behavior over all input patterns. We use the information relevant to model the worst case SN – the one that maximizes the peak-to-peak SN (see Section 5.3). The use of STA obviates the need for simulating the design over a large set of representative input patterns, and contributes to significant run-time improvement.

– Our methodology can handle a hierarchical design by composing the reduced models of different hierarchical components. The details are provided in Section 7.

– A pattern-dependent methodology (PDM), where a sequence of input vectors is provided, can be easily incorporated. This methodology, although impractical for a full chip design, can be used for a block-level design and should be more accurate than PIM. The PDM flow is shown in Figure 3. The sequence of input patterns is fed to a logic simulator, which yields derive cycle-accurate switching activity, i.e., for each cycle, lists of gates making rising or falling transitions. This information is used by the CWG algorithm, in that CWG in a given cycle is performed only for those gates that are switching in that cycle. Additionally, the arrival window, load capacitance and transition time information obtained from STA are also used.

4 Reference Model

The reference model uses the transistor-level netlist for each cell in the design and augments it with a model for the substrate. The models for all cells are then composed to get the reference model for the design. This model serves as the standard with which we will compare our reduced models. Transistors are modelled in BSIM3. The substrate model is derived based on the following assumptions:

- The design is a standard cell CMOS design.
- The technology is NWELL with lightly doped P- epitaxial layer on top of a highly doped P+ substrate layer (BULK).
- The depth of the NWELL is assumed to be negligible compared to the thickness of the P+ epitaxial layer. Thus, the resistance of the NWELL is ignored.
- The BULK, due to its much lower resistivity compared to P- epi layer, is treated as one node for a given cell.

For simplicity, let us assume that the design consists of only one inverter. The corresponding reference model is shown in Figure 4. For a given cell, the model contains one substrate node referred to as $BULK$ or substrate node S. The PMOS transistor substrate node is connected to the $BULK$ node through a series connection of a capacitor C_{nw} and a resistor R_{epi2}. The capacitor C_{nw} represents the reverse-biased NWELL to P- epi layer junction diode and the resistor R_{epi2} represents the P- epi layer resistance under the NWELL area. For an NMOS transistor, its substrate node is connected to S through a resistor R_{epi1} (the P- epi layer

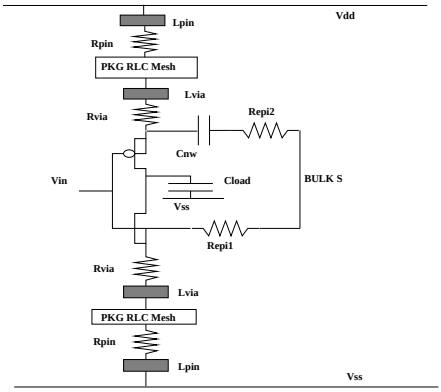

Figure 4: Reference model for an inverter

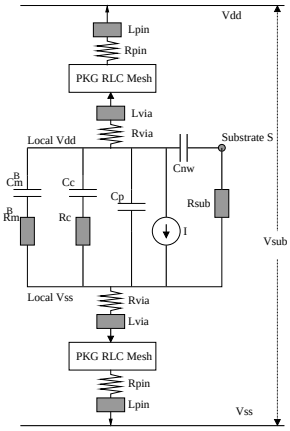

Figure 5: Reduced model

resistance under the transistor).

Each block has one VDD, one VSS and one *BULK* node. The VSS and VDD nodes are connected to a package model. The package modelling along with pin (Lpin, Rpin) and via (Lvia, Rvia) is described in more detail in Section 5.4. The substrate noise is measured at the *BULK* node point.

Previous work on reference substrate models includes [1, 14, 10, 11]. One drawback of these models is that they do not consider package model, which can be a big determinant in the noise.

5 Proposed Reduced Model

First, we present the basis of our reduced model in Section 5.1. For the model to be accurate and yet simple, we determine the minimum set of components that need to be modeled most accurately. We use sensitivity analysis (Section 5.2), which shows that current waveform and package model are the most important components, in that substrate noise is most sensitive to them. Their details are provided in Sections 5.3 and 5.4. In fact, modeling the current waveform is the core of our approach.

5.1 Original Reduced Model

Our reduced model for a digital block, as shown in Figure 5, is based on the model presented in [5]. It models switching activity and contains only passive circuit elements: a current source, internal capacitors and resistors. Capacitors and resistors model transistors, capacitance cells, and parasitics on the power/ground

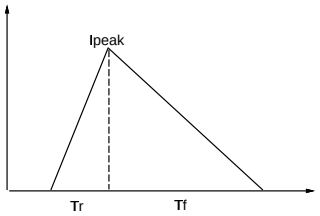

Figure 6: Current Waveform

nets. We have enhanced the model in [5] by introducing the package RLC mesh, L_{via} & R_{via}, and L_{pin} & R_{pin}. The presence of only passive elements and that too in a small number ensure that circuit simulation is fast.

R_m^B and C_m^B are the cumulative resistance and capacitance of transistors and wires in the block B. R_m^B is the average of pull-up and pull-down turn-on resistances of the transistors. C_m^B is the sum of all gate capacitances and wire loads in the block. For instance, for an inverter i, C_m^i is the load capacitance driven by i, which includes the gate capacitances of the fanout cells and the wire cap. If R_n and R_p are the ON resistances of the NMOS and PMOS transistors respectively, $R_m^i = (R_n + R_p)/2$. This assumes that the inverter is ON and OFF with equal probability, which is only an approximation. Also, R_n and R_p are functions of the operating point of the transistors. We approximate them by their average value in the linear region. As in [5], the equivalent single R_m^B (C_m^B) value for the entire block B containing several cells is computed by assuming that R_m^is (C_m^is) of all cells i in B are connected in parallel.

$$\frac{1}{R_m^B} = \sum_i \frac{1}{R_m^i}; \quad C_m^B = \sum_i C_m^i$$

C_c and R_c correspond to the decoupling capacitance cells placed in the vacant areas in the layout to guard against the voltage drop. They are computed from the SPICE netlists of these cells and the layout; the computation is similar to that of C_m and R_m. C_p is the parasitic capacitance on power or ground nets. R_{sub} is the p-well substrate resistance. C_{nw} is the junction capacitance between n-well and the substrate. R_{via} and L_{via} are the cumulative via resistance and inductance of the block.

The current source, I, is due to the total power consumption of the block, $P = VI_{avg}$. Since the current waveform is modeled as a triangle, as shown in Fig 6, $I_{avg} = \frac{1}{2} I_{peak} (T_r + T_f) f$, where f is the clock frequency.

5.2 Sensitivity Analysis

RM approximates the behavior of a digital circuit that is relevant for SNA. To improve the accuracy of RM, the components in RM should be modeled as accurately as possible. As we use more accurate and hence complex models, the overall flow becomes slower and even intractable for large designs. Clearly, there is a trade-off between model accuracy and its scalability. Our approach is to determine the minimum set of parameters which have significant impact on substrate noise, and model them more accurately. For this purpose, we performed several sensitivity analysis experiments on both accurate and reduced models.

5.2.1 Package Mesh

The package mesh is a two-dimensional mesh of RLC network representing the connection to off-chip pin. Table 1 shows the effect of 2D package mesh on the substrate noise for the reference model. As can be seen in this table, the noise is attenuated by the package mesh by a factor of 3. So it is important to model the package mesh accurately.

block	SN with mesh (mV)	SN w/o mesh (mV)
A	26.4	88.2
B	40.2	132.9

Table 1: Effect of package mesh

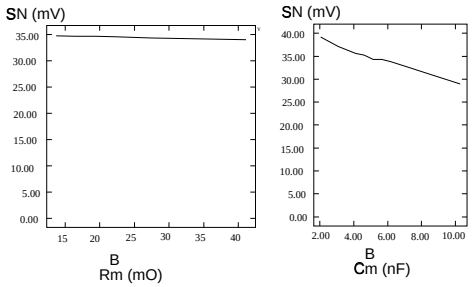

Figure 7: Variation of substrate noise with R_m & C_m

5.2.2 Block Resistance and Capacitance

We performed several experiments on the effect of block resistance, R_m, and capacitance, C_m, on the substrate noise. Figure 7 shows the dependence of substrate noise on R_m and C_m variations. We can see that the effect of R_m variation on substrate noise is negligible. Varying R_m from 15 mΩ to 40 mΩ (i.e., by a factor of 2.7) changes the peak-to-peak noise from 34.8 mV to 34.0 mV (i.e., by a factor of 0.98). This result works to our advantage, since our R_m computation method is not very accurate (as mentioned in Section 5.1). Even if our R_m value is within a factor of 2.5 from the actual value, it should not affect SN.

The C_m variation has a somewhat larger impact on the noise, although still not very significant. Varying C_m from 2 nF to 10.2 nF (i.e., by a factor of 5) changes the noise almost linearly from 39.2 mV to 29.0 mV (a factor of 0.74).

5.2.3 Current Waveform

In the original reduced model, the current waveform is assumed to have a triangular shape [5]. We performed two kinds of analyses. In the first, we changed the value of the peak current but kept $T_r + T_f$ constant (Figure 8 A). In the second, we changed both peak current and $(T_r + T_f)$, but kept $\frac{dI}{dt}$ constant (Figure 8 B). In both cases, the substrate noise is very sensitive to both the peak value and the shape of the current waveform.

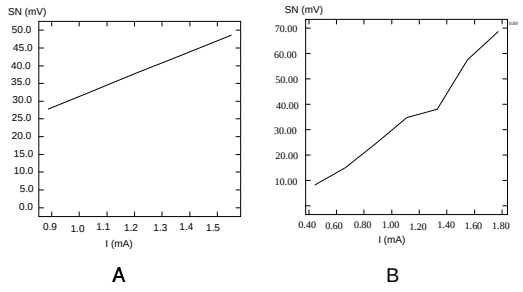

Figure 8: Variation of substrate noise with I: (A) $T_r + T_f$ constant (B) $\frac{dI}{dt}$ constant

5.2.4 Conclusion

Based on the results of sensitivity analysis, we can conclude that substrate noise is not sensitive to R_m and only slightly sensitive to C_m. So, we need not model these two components too accurately. However, the noise is very sensitive to the package model and the current waveform. So, these two parameters must be modeled accurately. We describe their modeling schemes next.

5.3 Current Waveform Modeling

In the presented model, only the switching current is considered, i.e. the leakage and sub-threshod current of transistors are ignored. The switching current is due to the charge and discharge of parasitic capacitances in the digital part of the circuit, when the transistors are making transitions. In this model, the switching current of a gate during the transition time is modeled as $I(t) = \partial C(t) V_C(t)/\partial t$. If we assume that the capacitance is constant during the transition time and $V_C(t)$ is a ramp function from 0 to V_{DD} (V_{DD} to 0) for a rise (fall) transition, which are fair approximations, the current of a gate through its load capacitance is a pulse function with a peak value of $I = CV_{DD}/\Delta T$ where ΔT is the transition time. The pulse width is also ΔT.

The overall current waveform is a superposition of the current pulses for all the gates in the digital part of the circuit.

In the presented approach, no logic simulation is performed. In other words, unlike the previous work in which there is a reduced model for each input pattern in the testbench [8, 6, 7, 13, 2, 9, 4], our model is independent of input patterns. As a result our pattern-independent model is several times faster than pattern-dependent methods. Our model is built by extracting information from STA and developing a reduced model that captures the worst case substrate noise over all possible input patterns.

The information obtained from STA for each gate g is as follows: 1. the arrival window: minimum arrival time T^g_{begin}, and maximum arrival time T^g_{end}, 2. the minimum transition time ΔT^g_{min}, and 3. the maximum transition time ΔT^g_{max}

It is assumed that the *transition start time*, T^g_{tran}, lies anywhere in the arrival window. The main idea of our proposed approach is to assign a valid transition start time for each gate g (i.e., $T^g_{begin} \leq T^g_{tran} \leq T^g_{end}$), such that the peak current and, as a result the substrate noise, are maximized.

Since no logic simulation is performed in the presented methodology to precisely determine which gates are making transition in each direction (rising or falling), switching activity and the relative number of gates making rising and falling transitions are assumed to be known. This information can be obtained either directly from the designer or from the logic simulation dump generated during design validation.

Figure 9 shows the pseudo code for the *overlapping* algorithm which finds the worst-case maximum possible peak current based on the arrival window, transition time, and load capacitance for each gate obtained from static timing analysis. This algorithm not only finds the maximum peak current, but also constructs the entire current waveform. In each iteration (lines 5-16), the maximum peak current that is possible from the remaining unselected gates (i.e., in list L) is computed. This is done as follows. For each gate g_i, I^i_{peak}, the maximum current that can be drawn at the start point of its arrival window, $T^{g_i}_{begin}$, is computed (lines 6-11). This is done by adding up the currents due to all gates g_j whose arrival windows overlap with the arrival window of g_i. Then, the gate g_k with maximum current is determined (lines 12-13). The transition start times for all the gates contributing to this maximum current (i.e., those in the list L_k) are set to the start point in the arrival window of g_k. These gates are removed from the list L (lines 14-16). The above iteration is performed until the list L becomes empty, i.e. the entire current waveform is constructed.

The above procedure is invoked once for the gates making rising transition and once for those making falling transition. In actual implementation of this algorithm, the list is sorted based on the start point of the arrival windows of the gates. The search for the

1.$L \leftarrow$ list of all switching gates
2.**for** each gate $g_i \in L$ **do**
3. $I^{g_i} \leftarrow C_{g_i} V_{DD} / \Delta T^{g_i}$
4.**repeat**
5. **for** each gate $g_i \in L$ **do**
6. $I^i_{peak} \leftarrow I^{g_i}$
7. $L_i \leftarrow \{g_i\}$
8. **for** each gate $g_j \in L (j \neq i)$ **do**
9. **if** $T^{g_i}_{begin} \leq T^{g_j}_{begin} \leq T^{g_i}_{end}$ **then**
10. $I^i_{peak} \leftarrow I^i_{peak} + I^{g_j}$
11. $L_i \leftarrow L_i \cup \{g_j\}$
12. $I_{peak} \leftarrow \max_i \{I^i_{peak}\}$
13. $k \leftarrow \arg\max_i \{I^i_{peak}\}$
14. **for** each gate $g_i \in L_k$ **do**
15. $T^{g_i}_{tran} \leftarrow T^{g_k}_{begin}$
16. $L \leftarrow L - L_k$
17.**until** $L = \Phi$

Figure 9: The overlapping algorithm for generating maximum peak current

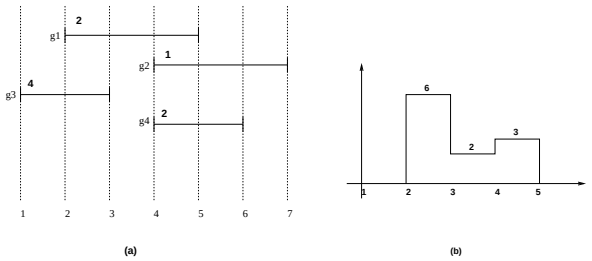

Figure 10: Example: (a) arrival time windows of gates g_1 to g_4; (b) current waveform using CWG algorithm

gates which are overlapping with a given gate is stopped if the difference in start points is more than the largest arrival window in the circuit. Using these optimizations, the overall complexity of this algorithm is $O(n^2 \log n)$, where n is the total number of gates in the design.

We illustrate the algorithm with the help of an example. Figure 10.a shows the arrival time windows of gates g_i, $i = 1$ to 4, along with the current values I^{g_i}. For instance, $T^{g_1}_{begin} = 2, T^{g_1}_{end} = 5, I^{g_1} = 2$. The maximum current at time 1, start point for g_3, is 4 units; at time 2, start point for g_1, is 6 units; and at time 4, start point for g_2 and g_4, is 5 units. Hence, the maximum current is 6 units, and the transition start time for g_1 and g_3 is set to time 2. g_1 and g_3 are removed from the list. The next maximum happens at time 4 for g_2 and g_4. Note that the overall current waveform is obtained by superimposing current pulses for all the gates. The duration of current pulse for a gate is equal to the minimum transition time of that gate; this takes care of the worst-case condition. Assume that the minimum transition time for g_1 is 2 units and for g_2, g_3 and g_4 1 unit each. The overall current waveform for this example is shown in Figure 10 b.

5.4 Package Model

Package model is an abstraction of power and ground planes in the package. It has a large impact on the power supply noise, because package inductance directly affects the $L\frac{di}{dt}$ noise [12]. We model the package as an RLC mesh (Figure 11). The inductance L, sheet resistance R, and capacitance C are computed from layer information. The package model is connected to VDD/VSS through L_{pin} & R_{pin} and to the digital part through L_{via} & R_{via}.

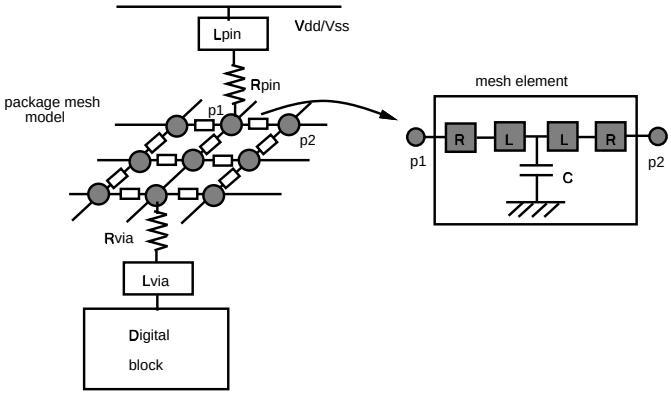

Figure 11: Mesh model of the package

6 Reduced Model Validation

The reduced model presented above was validated against the reference model. Since reference models for large circuits cannot be simulated due to exorbitant CPU-times, the reduced model can only be validated for relatively small circuits. Several circuits were generated with sizes varying from 50 to 650 gates. In these experiments, the technology is 0.11-μ, with VDD = 1.2V.

The results for the PIM flow are presented below. The current waveform and the reduced model were generated based on the timing windows obtained from a static timing analysis tool, as described in Section 5. The switching ratios used to generate the reduced model were calculated from the testbench that was used with the reference model. The reduced model was simulated and substrate noise voltage measured.

Table 2 shows results of the peak-to-peak (P2P) substrate noise comparisons. The noise measured by the PIM flow is close to the noise measured by reference model. There is a dramatic improvement in the CPU time. On average, the P2P noise in the reduced model is 13% different from that in the reference model, and the reduced model simualtion is 21 times faster. Note that the CPU time increases linearly with the number of cycles. The reference model was simulated for less than 10 cycles in our experiments. For larger designs, CPU times for reference model simulation increases exponentially, since bigger designs need exponentially more cycles. However, for the PIM flow, the time grows linearly with size, since model generation takes time linear in the design size.

7 Chip-level SNA

7.1 Chip-level Analysis Flow

For a chip-level design, it is not possible to measure the the substrate noise by a detailed SPICE model. We use the following methodology to handle the chip complexity. It exploits the hierarchical nature of the design. It takes three inputs: design information, cell libraries and technology parameters. Design information consists of gate netlist, chip floorplan, package size and parameters. Cell libraries include timing libraries and SPICE models. Technology parameters include process information such as sheet resistances of metal layers, capacitance, etc. The output is the substrate noise level for each hierarchical block.

The main steps of the methodology are as follows. First, the reduced model M_i of each block B_i is derived, as described in

ckt	gate	Noise (mV)			CPU Times (secs)		
	cnt	ref	red	%err	ref	red	X
c1	67	11.2	13.9	24.1	390	85	4
c2	281	31.6	25.5	-19.3	1760	92	19
c3	641	40.5	35.5	-12.4	4341	103	42
c4	56	6.0	5.5	-8.3	331	79	4
c5	422	10.7	11.4	6.5	3035	75	40
c6	97	8.9	9.4	5.6	521	89	5
c7	464	26.0	30.0	15.4	3641	107	34
avg				13			21

ref: SN for reference model; red: SN for reduced model
err = (red – ref)/ref; X: CPU time speed-up

Table 2: Substrate noise results

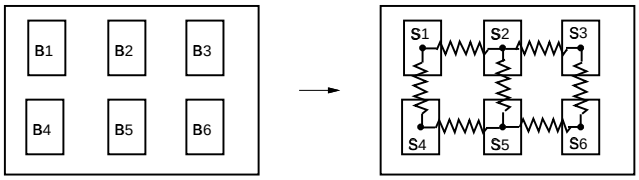

Figure 12: Floorplan-driven, hierarchical SN model

Section 5. Let the substrate in each block B_i be S_i (Figure 12). The reduced block models are then composed to generate a single chip-level model M with power structure representation. The relative placement of the blocks in the floorplan is used to derive M. If blocks B_i and B_j are physically adjacent in the floorplan, their corresponding substrate nodes S_i and S_j are connected through a resistor R_{ij}. The value of R_{ij} is computed using the sizes of the blocks and sheet resistance of the bulk. After combining the composed model with the package model, SPICE simulation is performed and SN is measured for each block.

7.2 Application to A Chip-level Design

We applied our methodology to a mixed-signal, switch chip. The analog components of this chip are the high-speed I/O macros. The gate count is 8 million. The chip has 34 top-level blocks, each block consisting of hundreds of thousands of gates. In our modeling, we were only concerned about P2P SN. The designers provided us with the switching activity for each block. The results were as follows. The complete simulation finished in 17 minutes. The maximum value of P2P SN over all S_i nodes was 40.7mV, the average being 34.5mV. The designers had specified a threshold of 60mV, which was met.

8 Conclusions

We presented a methodology for measuring peak-to-peak substrate noise of a mixed-signal design. The key idea is to derive a reduced model consisting only of passive components. Based on sensitivity analysis, we determined that the noise is most sensitive to the current waveform. We modeled this based on a pattern-independent methodology. Unlike the previous work in which a pattern-dependent reduced model is derived and evaluated for each input pattern, the proposed reduced model is generated and evaluated only once. The proposed model is validated on several benchmark circuits with the accurate reference model. The reduced model is within 13% of the reference model with respect to P2P SN and up to 42 times faster. Finally, a technique for measuring substrate noise of a hierarchical full-chip design was proposed and results for a real chip were presented.

The future work is in the following directions. To obtain a more accurate current waveform, circuit topology and logic implications are currently being integrated in the CWG algorithm. We need better modeling of the current waveform in the presence of inductance. Finally, in this paper, we focused only on P2P SN, since the analog part of the chip we targeted consisted only of I/O macros. For a design that uses frequency-sensitive analog components, our model should be extended to handle frequency analysis.

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