Variation Experimental Reports

January 2, 2006

1 Experimental Setup

Testcase:

cascade inverters to drive a 100x cout

Metric:

Delay and power

Freedoms:

(1) stage ratio and stage number (2) P/N ratio (3) voltage scaling: 1.1 V and 0.7 V

Variation settings:

Types of variation (1) Temp (-20% - 100% of nominal temperature variation) (2) Vth (+/- 20%) (3) Tox (+/- 20%)

2 Experimental Results

2.1 Optimized design under 0.7v and 1.1v

As suggested by Changbo, I enumerated all designs with stage ratio between 3.5 and 6.5 with 0.5 as the step and P/N ratio between 2.0 and 6.0 with 0.5 as the step to find the optimal design under 0.7v and 1.1v, respectively.

Two kinds of objective functions are used: A) optimal delay, B) minimal power with 120% optimal delay (i.e. 20% slack allowed). Table 1 shows the optimal settings under the two objective functions, respectively. "0.7v_delay_opt" and "1.1v_delay_opt" are optimal settings under Vdd=0.7v and Vdd=1.1v, respectively, for optimal delay (objective A). "0.7v_power_opt" and "1.1v_power_opt" are optimal settings under Vdd=0.7v and Vdd=1.1v, respectively, for optimal power (objective B). Table 2 shows the delay and power of optimized designs (in Table 1) under Vdd=0.7v and 1.1v, respectively.

Table 1: Optimal settings

Design	P/N ratio	Stage ratio	Stage number
0.7v_delay_opt	4.5	5.0	3
1.1v_delay_opt	5.0	5.0	3
0.7v_power_opt	3.5	6.0	3
1.1v_power_opt	3.5	5.5	3

2.2 Optimized designs under process variation

I conducted two groups of experiments for objective A and B, respectively. For the two delay optimal designs "0.7v_delay_opt" and "1.1v_delay_opt", Figure 1 and Figure 2 shows the delay and power with the process variation when they work under Vdd=0.7v and Vdd=1.1v, respectively. For the two power optimal designs "0.7v_power_opt" and "1.1v_power_opt", Figure 3 and Figure 4 shows the delay and power with the process variation when they work under Vdd=0.7v and Vdd=1.1v, respectively.

Table 2: Delay and Power of optimized designs under Vdd=0.7v and 1.1v

Design	Vdd(v)	Delay(s)	Power(W)
0.7v_delay_opt	0.7	3.736e-10	1.82e-05
0.7v_delay_opt	1.1	2.622e-10	4.534e-05
1.1v_delay_opt	0.7	3.881e-10	1.86e-05
1.1v_delay_opt	1.1	2.609e-10	4.713e-05
0.7v_power_opt	0.7	4.401e-10	1.587e-05
0.7v_power_opt	1.1	3.219e-10	4.023e-05
1.1v_power_opt	0.7	4.089e-10	1.627e-05
1.1v_power_opt	1.1	2.952e-10	4.129e-05

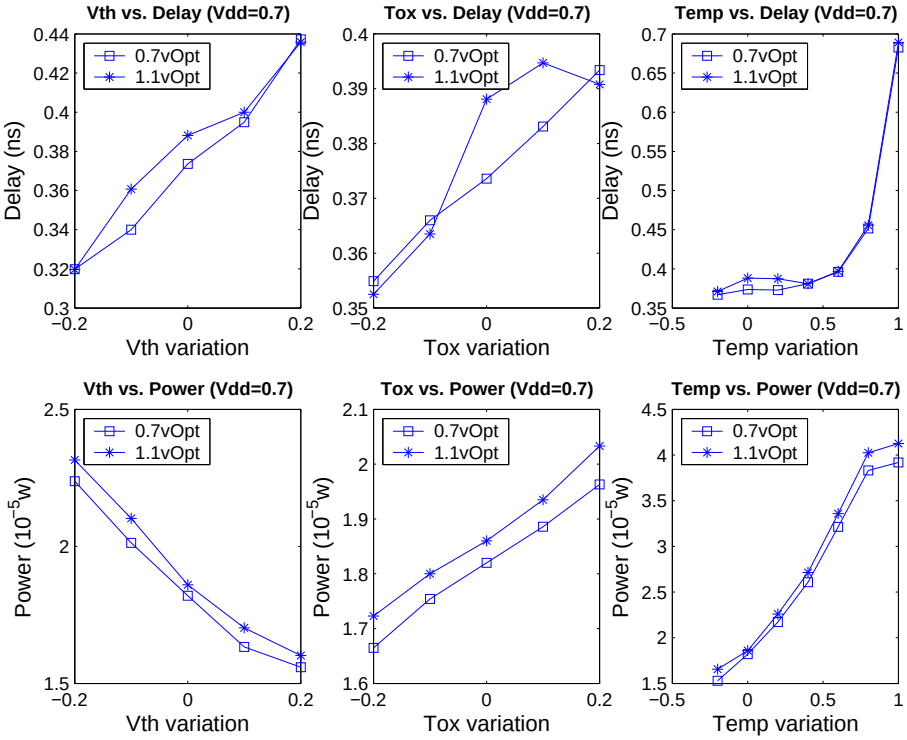

Figure 1: 0.7v_delay_opt and 1.1v_delay_opt with Vdd=0.7v

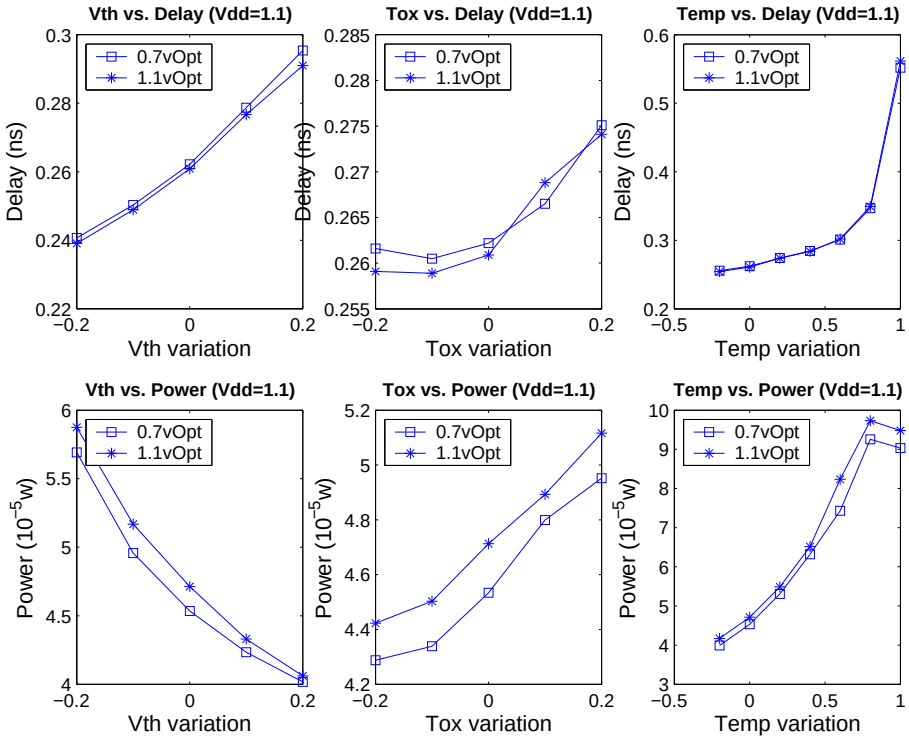

Figure 2: 0.7v_delay_opt and 1.1v_delay_opt with Vdd=1.1v

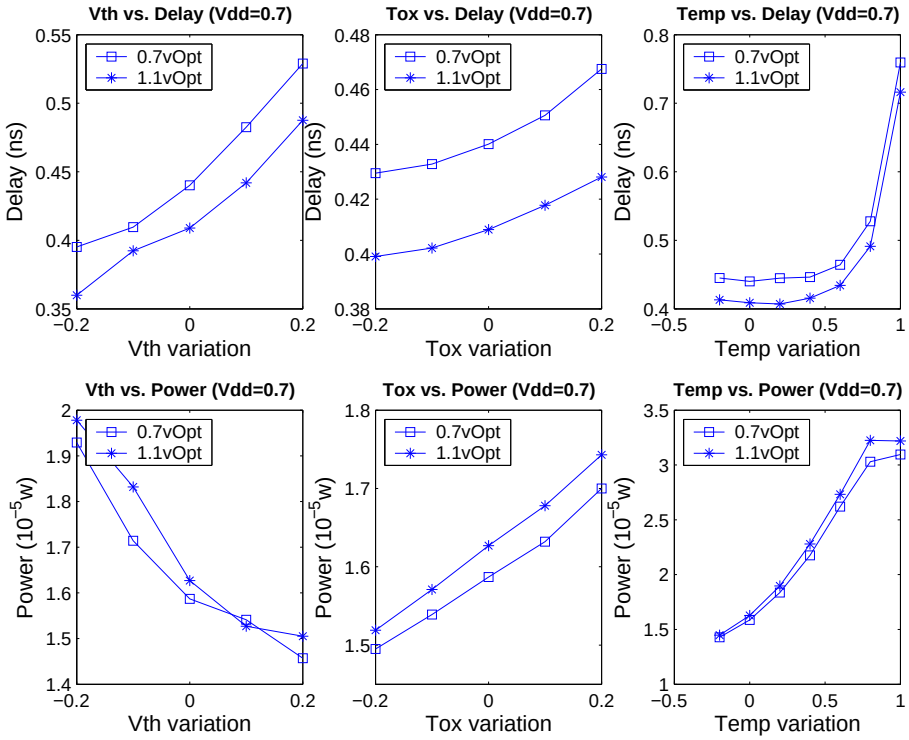

Figure 3: 0.7v_power_opt and 1.1v_power_opt with Vdd=0.7v

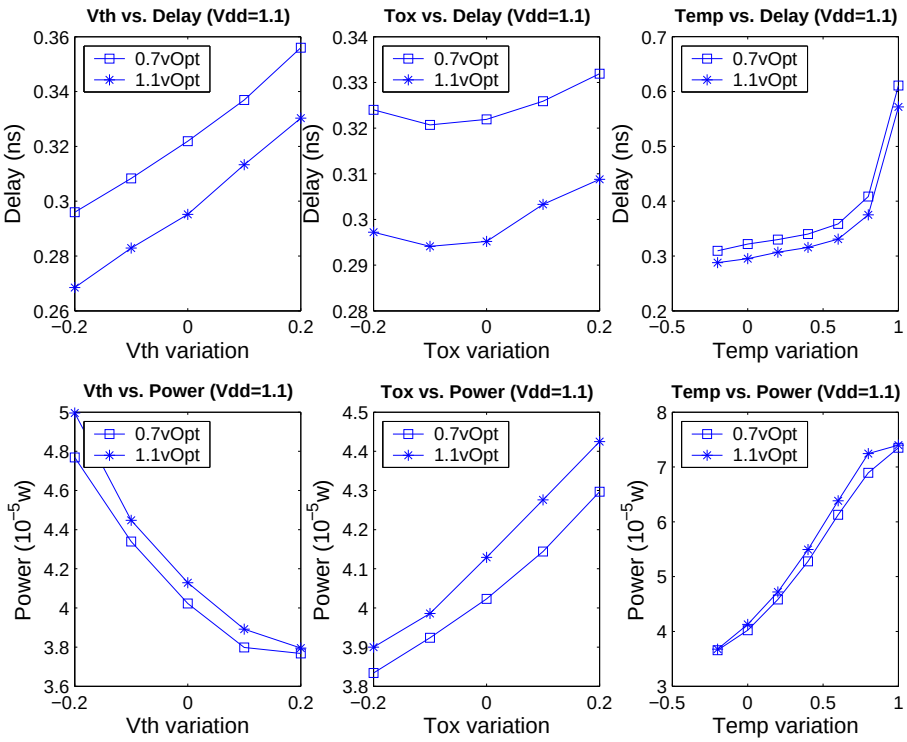

Figure 4: 0.7v_power_opt and 1.1v_power_opt with Vdd=1.1v