Weekly Report for Yu Hu's work from Aug. 22 to Aug. 28

August 28, 2005

1. **Review Jinjun's process variation buffer insertion work by both paper and code.** For extend my speedup techniques to consider process variation in buffer insertion, I reviewed Jinjun's ICCAD'05 submission and checked out his "vBuf" package from cvs. As there is no instructions for how to run the code and neither input benchmarks included in the package, I asked Jinjun to send these stuffs to me but no replies yet. I need these so that I can firstly integrate the "vBuf" into BIC_package and then add the speedup part in. As an initial thought of speedup "vBuf", we can try to prove whether "Pre-Slack buffer pruning" is still hold and do some experiments if it is. The "vBuf" considers only timing issue, which make the increase of options not so quickly as power-optimal problem, therefore, sampling techniques will be not effective for runtime. I wonder whether we need to extend this work for power optimization in future.

2. **Prepare my presentation in the next group meeting.** I've finished prepared the slides for my presentation in the next group meeting, though it has been cancelled because of Prof. He's visiting to Sun in the next Tuesday. The main purpose of my presentation is to introduce my work on dual vdd buffering speedup.

3. **Dual Vdd buffer insertion journal paper writing.** The first version draft of the journal paper has been checked into cvs under directory "dvdd_jrnl". This version is abased on the newly updated outline with four sections "introduction, level converter free dual vdd formulation, speedup techniques, conclusions". The experimental results are combined right after the description of the responding subsections. The proof for the optimality of the level converter free formulation is not accomplished yet. The comparison cases in King Ho's DAC'05 paper is not a solid proof for the journal paper, it should be proved by comparing both line (2-pin net) and tree (multi-pin net) cases. The difficulty becomes from there exist several combinations of vdd level for branches in the tree case. I'll try to figure out it in the next week.

4. **Preparing slides for Prof. He's talk in Sun.** The talk is mainly focused on "Interconnect Design for Low Power and Process Variation Tolerance", which is divided into 2 parts: Part I C 1) Dual Vdd Interconnect Dual Vdd Buffering. 2) Chip level time slack allocation 3) How to decide vdd levels for interconnects and Part II - Variation tolerant interconnects. I compiled King Ho's DAC'05 work, ISLPED'05 work and my ICCAD'05 work together to get the part I slides and Jinjun takes care of Part II.

5. **Escape routing paper reading.** To extend our studies on escape and package routing, I searched several papers and read two typical ones (C. K. Cheng's recent escape routing paper pointed by Prof. He can not be found as the conference seems not in IEEE Xplore or ACM portal).

   "Horiuchi, M.; Yoda, E.; Takeuchi, Y., Escape routing design to reduce the number of layers in area array packaging, IEEE Transaction on Advanced Packaging, Volume 23, Issue 4, Nov. 2000 Page(s):686 - 691". Focused on the escape routing design within one die, this paper studies on the effect of the escape routing style on the layer number reduction. The authors compare the conventional escape routing (escape from the outer row to inner row) and the hybrid channel routing (based on preferential routing along the vertical rows) and different settings of the hybrid channel are discussed. The main conclusion is, the layer counts can be decreased for a given identical area array pad matrix depending on a routing design and nothing change in the manufacturing process, such as reduce the wire width, is required with this procedure.

   "Simultaneous escape routing and layer assignment for dense PCBs Ozdal, M.M.; Wong, M.D.F.; Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on 7-11 Nov. 2004 Page(s):822 - 829". This paper mainly discussed package routing for the pins between two dies (e.g. PCB). The objective of this problem is to minimize the number of crossings between wires connecting pins in both dies, in the same time no conflicts can occur in the escape routing in the individual die. The authors formulate this problem as a longest path with forbidden pairs (LPFP) problem, which is an NP-Hard problem.

Two algorithms, an exact one and a random based approximate but faster one, are proposed to handle LPFP problem.

For the existing papers for escape routing, the routability-driven escape routing has been well studied, but there are few works focusing on performance driven routing, i.e. no timing and power issues are added into consideration. We can add these stuffs into escape routing and set up our new formulations and algorithms. The key point is to find out what performance issues are more important in escape and package routing.